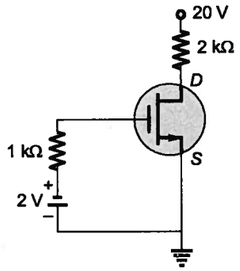
6 FET Biasing

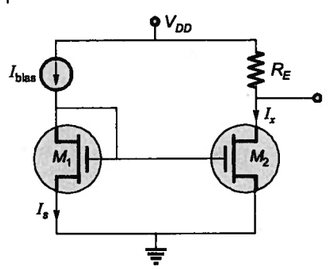
Multiple Choice Questions

Q.1 The value of V_{GS} and V_G for the circuit shown in figure is



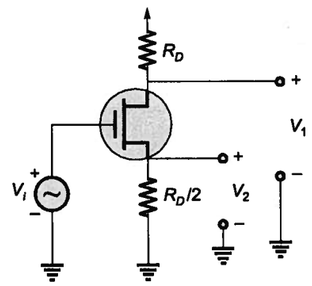
(a) –2 V, –2 V (b) 2 V, –2 V
(c) 2 V, –2 V (d) –2 V, 2 V

Q.2 For the circuit shown in the following figure, transistors M_1 and M_2 are identical NMOS transistors. Assume that M_2 is in saturation and output is unloaded.



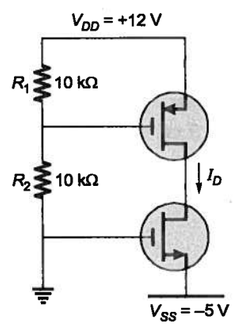
(a) $I_x = I_{bias} + I_s$
(b) $I_x = I_{bias}$
(c) $I_x = I_{bias} - I_s$
(d) $I_x = I_{bias} - \left(V_{DD} - \frac{V_{out}}{R_E}\right)$

Q.3 In the MOSFET amplifier of figure, the signal output V_1 and V_2 obey the relationship



(a) $V_1 = \frac{V_2}{2}$ (b) $V_1 = -\frac{V_2}{2}$
(c) $V_1 = 2\ V_2$ (d) $V_1 = -2\ V_2$

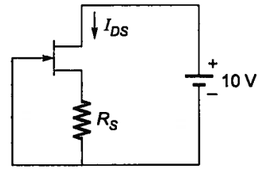
Q.4 For the MOSFET shown in the figure, the threshold voltage $|V_t| = 2$ V and $K = \frac{1}{2}\mu C\left(\frac{W}{L}\right) = 0.1\text{mA/V}^2$. The value of I_D (in mA) is _____.



(a) 0.9 mA (b) 0.5 mA
(c) 1.5 mA (d) 1.15 mA

[GATE-2014]

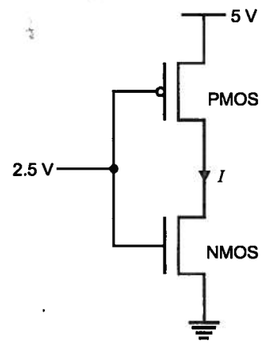
Q.5 The JFET in the circuit shown in figure has an I_{DSS} = 10 mA and $V_P = -5$ V. The value of the resistance R_S for a drain current I_{DS} = 6.4 mA is (Select the nearest value)



(a) 150 ohms (b) 470 ohms
(c) 560 ohms (d) 1 kilo ohm

[GATE-1992]

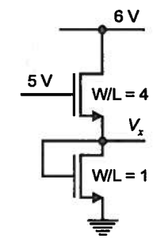
Q.6 In the CMOS inverter circuit shown, if the transconductance parameters of the NMOS and PMOS transistors are $K_n = K_p = \mu_n C_{ox}\frac{W_n}{L_n} = \mu_p C_{ox}\frac{W_P}{L_P} = 40\ \mu\text{A/V}^2$ and their threshold voltages are $V_{THn} = |V_{THp}| = 1$ V, the current I is



(a) 0 A (b) 25 μA
(c) 45 μA (d) 90 μA

[GATE-2007]

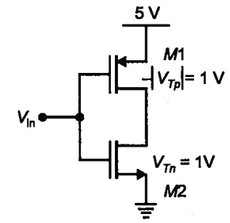
Q.7 In the circuit shown below, for the MOS transistors, $\mu_n C_{ox} = 100\ \mu\text{A/V}^2$ and the threshold voltage $V_T = 1$ V. The voltage V_x at the source of the upper transistor is



(a) 1 V (b) 2 V
(c) 3 V (d) 3.67 V

[GATE-2011]

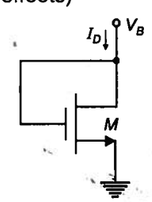
Q.8 In the CMOS circuit shown, electron and hole mobilities are equal, and $M1$ and $M2$ are equally sized. The device $M1$ is in the linear region if



(a) $V_{in} < 1.875$ V
(b) $1.875\ \text{V} < V_{in} < 3.125$ V
(c) $V_{in} > 3.125$ V
(d) $0 < V_{in} < 5$ V

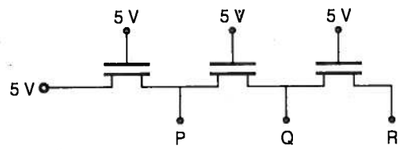
[GATE-2012]

Q.9 The small-signal resistance (i.e., dV_B/dI_D) in kΩ offered by the n-channel MOSFET M shown in the figure below, at a bias point of $V_B = 2$ V is (device data for M: device transconductance parameter $k_N = \mu_n C'_{OX}(W/L) = 40\ \mu\text{A/V}$, threshold voltage $V_{TN} = 1$ V, and neglect body effect and channel length modulation effects)



(a) 12.5 (b) 25
(c) 50 (d) 100 **[GATE-2013]**

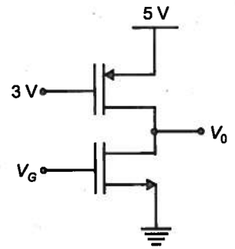
Q.10 In the following circuit employing pass transistor logic, all NMOS transistors are identical with a threshold voltage of 1 V. Ignoring the body-effect, the output voltages at P, Q and R are,



(a) 4 V, 3 V, 2 V (b) 5 V, 5 V, 5 V
(c) 4 V, 4 V, 4 V (d) 5 V, 4 V, 3 V

[GATE-2014]

Q.11 Consider the CMOS circuit shown, where the gate voltage V_G of the n-MOSFET is increased from zero, while the gate voltage of the p-MOSFET is kept constant at 3 V. Assume that, for both transistors, the magnitude of the threshold voltage is 1 V and the product of the transconductance parameter and the (W/L) ratio, i.e. the quantity $\mu C_{ox}(W/L)$, is 1 mA V^{-2}.



(i) For small increase in V_G beyond 1 V, which of the following gives the correct description of the region of operation of each MOSFET?
(a) Both the MOSFETs are in saturation region
(b) Both the MOSFETs are in triode region
(c) n-MOSFET is in triode and p-MOSFET is in saturation region
(d) n-MOSFET is in saturation and p-MOSFET is in triode region

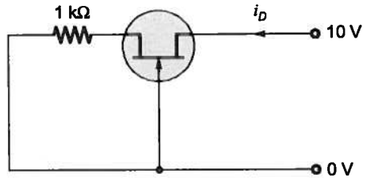
[GATE-2009]

(ii) Estimate the output voltage V_0 for V_G =1.5 V. [Hints: Use the appropriate current-voltage equation for each MOSFET, based on the answer to part (i)]

(a) $4-\frac{1}{\sqrt{2}}$ V (b) $4+\frac{1}{\sqrt{2}}$ V
(c) $4-\frac{\sqrt{3}}{2}$ V (d) $4+\frac{\sqrt{3}}{2}$ V

[GATE-2009]

Q.12 Consider the JFET circuit shown below:



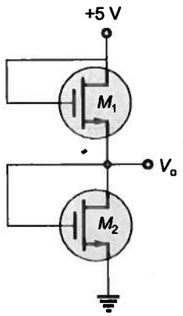
Current i_D is given by

(Assume $i_D = 12\left(1+\frac{V_{GS}}{4}\right)^2$

(a) 2.26 mA (b) 3.39 mA
(c) 1.48 mA (d) 2.78 mA

Numerical Data Type Questions

Q.13 Consider the circuit shown below.



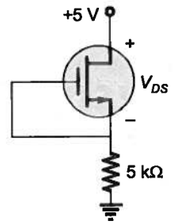
Both transistors have parameter as follows:

$V_{TN} = 0.8$ V, $k_n' = 30\ \mu A/V^2$

If the width-to-length ratios of M_1 and M_2 are $\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = 40$, the output V_o is ____ volts.

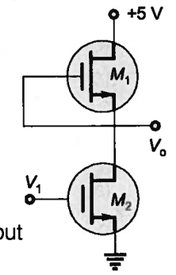
Q.14 Consider the circuit shown below. The transistor parameters are as follows.

$K_n = 0.1$ mA/V^2
$V_{TN} = -2$ V



What is the value of drain to source voltage V_{DS} (in volts)?

Q.15 Consider the circuit shown below. The transistor parameters are as follows:



For M_2 $V_{TN2} = 1$ V
$K_{n2} = 50\ \mu A/V^2$
For M_1 $V_{TN1} = -2$ V
$K_{n1} = 10\ \mu A/V^2$

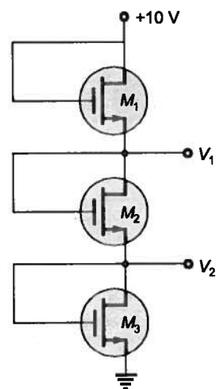
If V_1 = 5 V, then value of output voltage (V_o) is _____ volts.

Q.16 A MOSFET in saturation has a drain current of 1 mA for V_{DS} = 0.5 V. If the channel length modulation coefficient is 0.05 V^{-1}, the output resistance (in kΩ) of the MOSFET is _____.

[GATE-2015]

Try Yourself

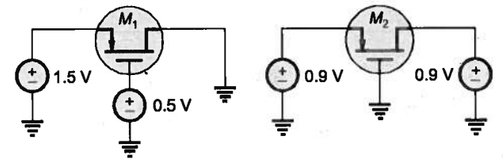
T1. In the circuit shown below, the transistor parameters are $V_{TN} = 1$ V and $k_n' = 36\ \mu A/V^2$.



If I_D = 0.5 mA, V_1 = 5 V and V_2 = 2 V then the width-to-length ratio required in each transistor are

	$\left(\frac{W}{L}\right)_1$	$\left(\frac{W}{L}\right)_2$	$\left(\frac{W}{L}\right)_3$
(a)	1.75	6.94	27.8
(b)	4.93	10.56	50.43
(c)	35.5	22.4	5.53
(d)	56.4	38.21	12.56

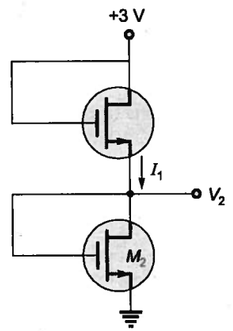
T2. In the given circuit of figure, transistors M_1 and M_2 are operating in (V_{TH} = 0.4 V)



(a) M_1 is in linear region, M_2 is OFF
(b) both M_1 and M_2 are OFF
(c) M_1 is in saturation, M_2 is in linear region
(d) both M_1 and M_2 are in saturation region

T3. For the circuit shown below, both transistors are identical and has following parameters:

$\mu_n C_{ox} = 20\ \mu A/V^2$, $V_{Th} = 1$ V, $\frac{W}{L} = 3$



Current I_1 and voltage V_2 are respectively,
(a) 15 μA, 3 V (b) 7.5 μA, 1.5 V
(c) 15 μA, 1.5 V (d) 7.5 μA, 3 V