Chapter 7

Operational Amplifiers

LEARNING OBJECTIVES

After reading this chapter, you will be able to understand:

- Operational Amplifiers
- Single–ended operation
- CMRR (common mode rejection ratio)
- Level–shifter
- 2 electrical parameters of op-Am
- Open loop op-Amp configurations
- The non-inverting amplifier
- Closed loop op-Amp configurations
- Filters
- Oscillators
- Theory of sinusoidal oscillators
- Waveform generators and wave shaping circuits
- Square wave generation from sinusoid
- Monostable multivibrator
- Power supplies

Operational Amplifiers

An operational amplifier is a direct, coupled, high gain amplifier consisting of one or more differential amplifiers, usually followed by a level translator and an output stage. The output stage is generally a push-pull or push-pull complementary-symmetry pair

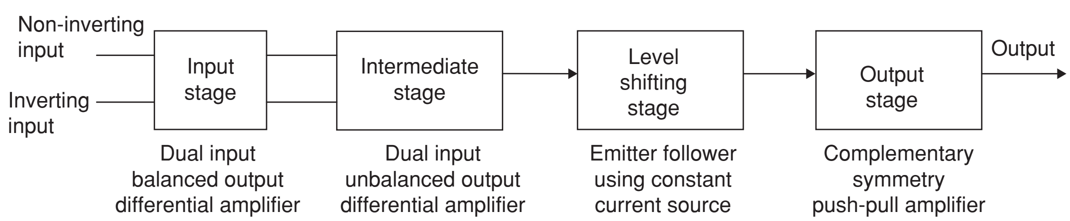
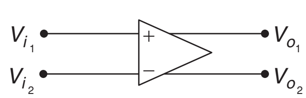


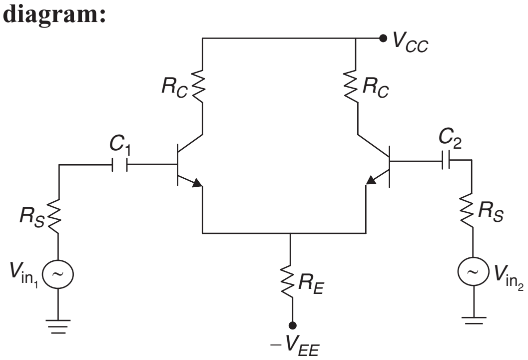
Figure 1 Block diagram of a typical op-amp

Differential Amplifier

Symbol:



Circuit diagram:



Modes of operation:

(i) Single-ended: Either of the input is grounded

(ii) Double-ended: Opposite polarity signals are applied at two inputs.

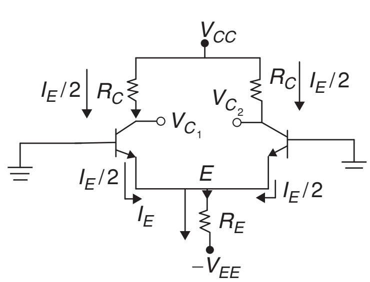
(iii) Common mode: Two similar input signals are applied at both inputs.

DC analysis:

(i) Make the AC sources ground

(ii) Replace the coupling capacitors open

Equivalent Circuit:



KVL at input side gives

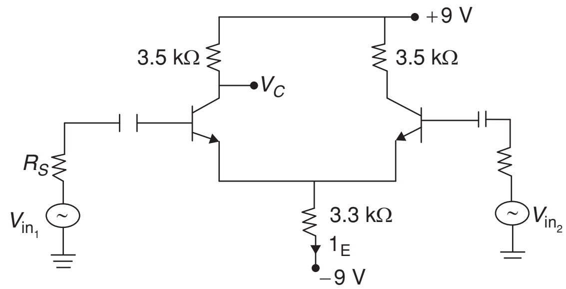
$0 - V_{BE} - V_E = 0$

$V_E = -0.7$ V

$V_E - I_E R_E + V_{EE} = 0$

$$I_E = \frac{V_{EE} - 0.7}{R_E}$$

Example 1: Determine I_E and V_C for the given circuit



(A) 4.1 V and 5 mA
(B) 5 V and 2.5 mA
(C) 5 V and 5 mA
(D) 4.6 V and 2.5 mA

Solution: (D)

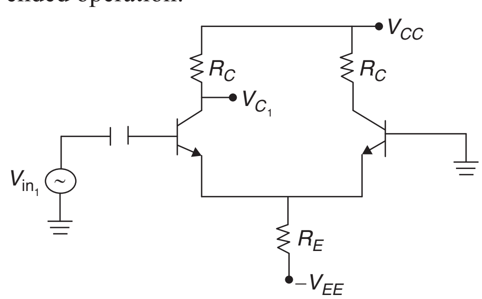
$$I_E = \frac{V_{EE} - 0.7}{R_E}$$

$$I_E = \frac{9 - 0.7}{3.3\text{ k}} = 2.5\text{ mA}$$

$$V_C = V_{CC} - \frac{I_E}{2} R_C$$

$V_C = 4.6$ V.

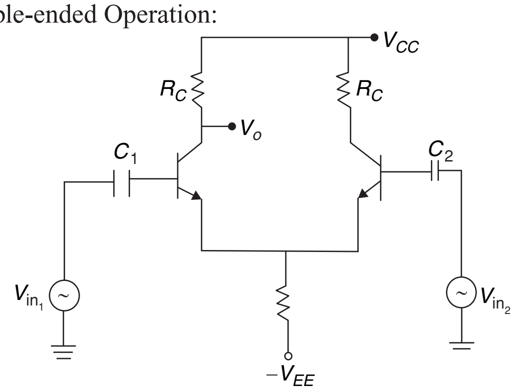
Single-ended operation:



Voltage gain $A_V = \dfrac{R_C}{2r_e} = \dfrac{V_{C_1}}{V_{in_1}}$

Input impedance $Z_i = 2\beta r_e$

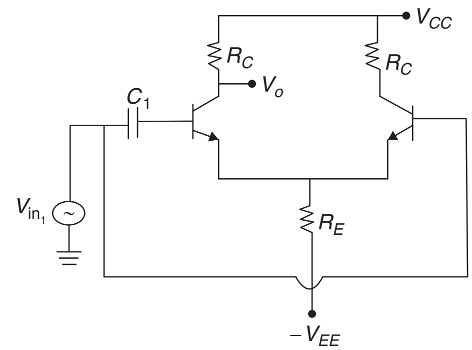
Double-ended Operation:



$$V_d = V_{in_1} - V_{in_2}$$

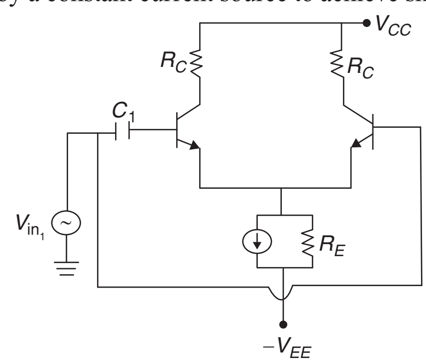
$$A_V = \frac{V_0}{V_d} = \frac{R_c}{2r_e}$$

Common-mode Operation:



$$A_C = \frac{V_0}{V_{in}} = \frac{\beta R_c}{\beta r_e + 2(\beta + 1)R_E}$$

In all IC design application, 'A_c' (common-mode gain) must be as small as possible. Hence R_E has to be so larger. So R_E is replaced by a constant current source to achieve smaller 'A_c'.



CMRR (Common-mode rejection ratio):

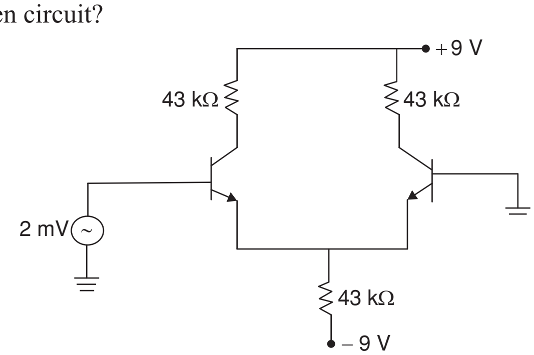
$$\text{CMRR} = \frac{A_d}{A_c}$$

$$\text{CMRR in dB} = 20\log\left(\frac{A_d}{A_c}\right)$$

Where, A_d = Differential gain
A_c = common mode gain

In all practical applications, CMRR should be as high as possible. Ideal value of CMRR = ∞

Example 2: Calculate the single-ended voltage gain for the given circuit?



(A) 100 (B) 91.2
(C) 87.4 (D) 83

Solution: (C)

$$A_v = \frac{R_c}{2r_e}$$

$$r_e = \frac{26}{I_{E_1}}\text{ mV} = \frac{26}{I_{C_1}}\text{ mV}$$

$$I_E = \frac{V_{EE} - 0.7\text{ V}}{R_E} = 193\ \mu\text{A}$$

$$I_{C1} = \frac{I_E}{2} = 96.5\ \mu\text{A}$$

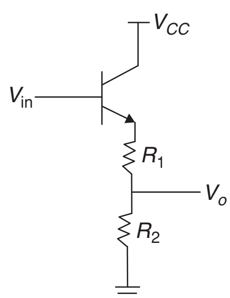
$$\therefore\quad r_e = \frac{26\text{ mv}}{96.5\ \mu\text{A}} = 269\ \Omega$$

$$A_v = \frac{R_C}{2r_e} = 87.4$$

Level-Shifter

The purpose of the coupling capacitor in any amplifier is to block DC and allows AC. In the absence of a capacitor, level-shifter circuit is used to block DC

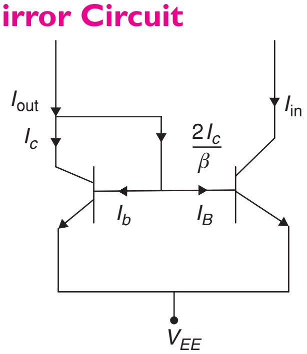
Simple Level Shifter:



$$V_0 = V_{\text{in}}\frac{R_2}{R_1 + R_2}$$

Resistor R_2 not only level-shifts DC by an amount $\frac{R_2}{R_1 + R_2}$ but also attenuates the AC signal. Remedy is to replace R_2 with current mirror circuit.

Current-mirror Circuit



If both the transistors are assumed to be symmetrical,

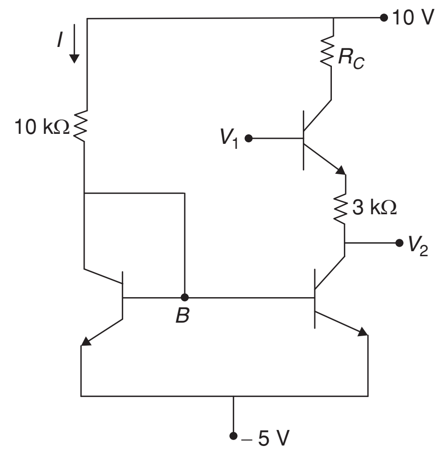
$$I_{\text{out}} = I_C + \frac{2I_c}{\beta}$$
$$= I_C[1 + 2/\beta]$$

If 'β' is designed to be so large, then

$$I_{\text{out}} \approx I_C \approx I_{\text{in}}$$

Advantage: I_C depends only on base current but not on the collector–emitter voltage.

Example 3: Find V_1–V_2 level shift in the given circuit if V_{BE} = 0.7 V and β is assumed to be so large?



(A) 4.52 (B) 5.23
(C) 4.99 (D) 6.25

Solution: (C)

$V_B - 0.7 + 5 = 0$

$V_B = -4.3$ V

$$I = \frac{10 - V_B}{10\text{ K}} = 1.43\text{ mA}$$

$\therefore$ Current through 3 kΩ resistor is 1.43 mA

$V_1 - V_2 = 0.7 + I(3\text{ k}\Omega)$

$V_1 - V_2 = 4.99$

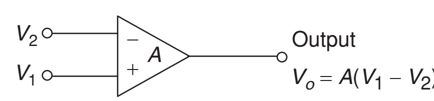
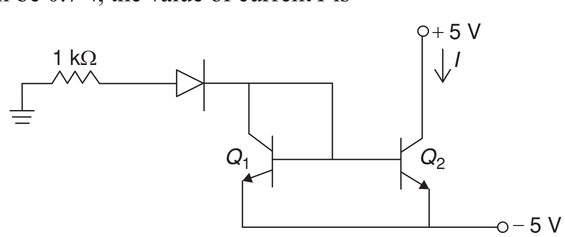


Figure 2 Schematic symbol for op-amp

Example 4: Two perfectly matched silicon transistors are connected as shown in the figure. Assuming β of the transistors to be very high and forward voltage drop in diode will be 0.7 V, the value of current I is



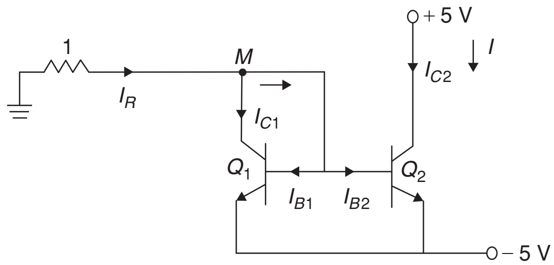
(A) 0 mA (B) 3.6 mA
(C) 4.3 mA (D) 5.7 mA

Solution: (B)

Since both are perfectly matched

$$V_{BE_1} = V_{BE_2}$$

$$\frac{I_{C_1}}{I_{C_2}} = \exp^{\left[\frac{V_{BE_1} - V_{BE_2}}{V_t}\right]} = e^0 = 1$$



Since β is the same for both transistors, $I_{B_1} = I_{B_2} = I_B$

By KVL in loop at Q_1, $I_R = \dfrac{0 - 0.7 - 0.7(-5)}{1\text{ k}\Omega} = 3.6$ mA

KCL at point M,

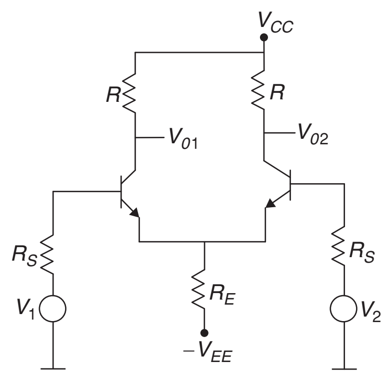
$$I_R = I_{C_1} + 2I_B = I_{C_1} + 2\frac{I_{C_1}}{\beta}$$

$$I_{C_1} = \frac{\beta}{\beta + 2} \cdot I_R$$

for large β

$$I_{C_1} \approx I_R = 3.6 \text{ mA}$$

Common Data for Questions 5 to 7: The differential amplifier, of shown in the figure has element values R_C = 50 kΩ, r_π = 1 MΩ, R_s = 2 kΩ, R_E = 200 kΩ, $\beta_0 = 2 \times 10^3$



Example 5: Differential mode voltage gain is

(A) –300 (B) –200

(C) –100 (D) 50

Solution: (C)

$$h_{fe} = \beta = 2 \times 10^3,\ r_\pi = 1\text{ M}\Omega$$

$$R_C = R_L = 50\text{ k}\Omega,\ R_E = 200\text{ k}\Omega,\ R_S = 2\text{ k}\Omega$$

$$A_{DM} = -\frac{h_{fe}R_L}{r_\pi} = -\frac{2 \times 10^3 \times 50 \times 10^3}{1 \times 10^6} = -100$$

Example 6: Common mode voltage gain is

(A) –0.5 (B) –0.25

(C) –0.125 (D) 0

Solution: (C)

$$A_{CM} = -\frac{R_L}{2R_E} \text{ when } r_\pi > R_S$$

$$= -\frac{50\text{ k}\Omega}{2 \times 200\text{ k}\Omega} = -\frac{1}{8} = -0.125$$

Example 7: The value of CMRR in dB is

(A) 800 (B) 60

(C) 58 (D) ∞

Solution: (C)

$$\text{CMRR} = \frac{A_{DM}}{A_{CM}} = \frac{100}{0.125} = 800$$

CMRR in dB = 20 log (800) = 58 dB

Electrical Parameters of Op-amp

Input offset voltage is the voltage that must be applied between the two input terminals of an op-amp to null the output.

The algebraic difference between the currents into the inverting and non-inverting terminals is referred to as input offset current $I_{io} = |I_{B_1} - I_{B_2}|$

Input bias current I_B is the average of the currents that flow into the inverting and non-inverting terminals of op-amp

$$I_B = \frac{I_{B_1} + I_{B_2}}{2}$$

Common mode rejection ratio is the ratio of differential voltage gain A_d, to the common mode voltage gain A_{CM}

$$\text{CMRR} = \frac{A_d}{A_{CM}}$$

The higher the value of CMRR, the better is the matching between the input terminals.

The change in an op-amp input offset voltage V_{io} caused by variations in supply voltages is called the supply voltage rejection ratio (SVRR), PSRR.

Slew rate is defined as the maximum rate of change of output voltage per unit of time and is expressed in volt per microseconds

$$\text{SR} = \left.\frac{dV_0}{dt}\right|_{\text{maximum}} \text{V/}\mu\text{s}$$

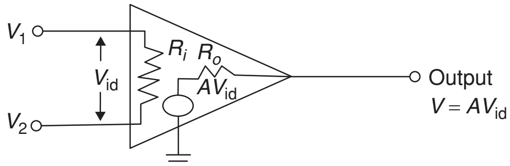
Slew rate indicates how rapidly the output of an op-amp can change in response to the changes in the input frequency, slew rate changes with change in voltage gain, and is normally specified at (+1) unity gain

The ideal op-amp characteristics:

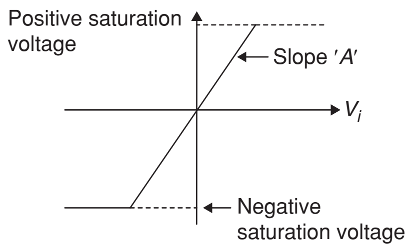
1. Infinite voltage gain (A)
2. Infinite input resistance (R_i)

3. Zero output resistance (R_0)
4. Zero output voltage when input voltage is zero
5. Infinite bandwidth
6. Infinite CMRR
7. Infinite slew rate

Equivalent Circuit of an Op-Amp

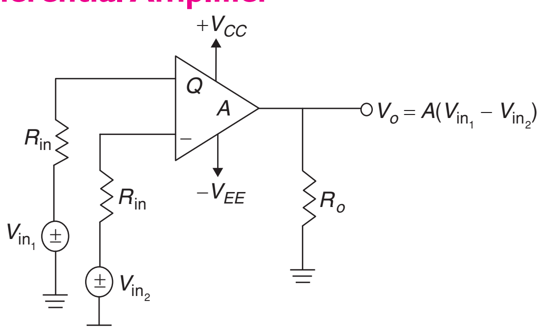


$$V_0 = AV_{id} = A(V_1 - V_2)$$

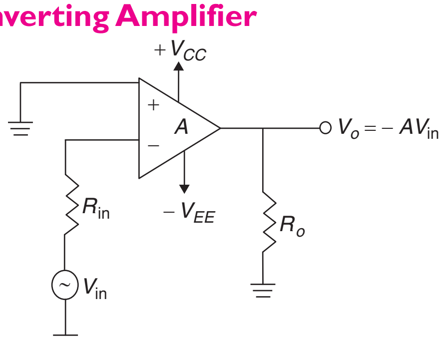


Open Loop op-amp Configurations

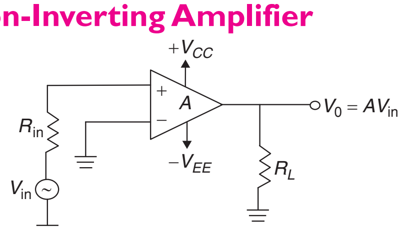
Differential Amplifier



The Inverting Amplifier



The Non-Inverting Amplifier

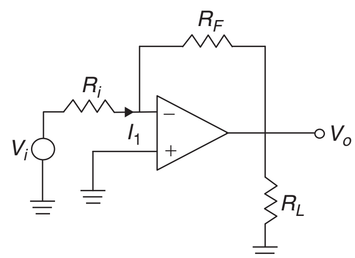


Very small values of input voltages can drive the open op-amp into saturation, as gain is very high, this prevents the use of open loop configurations of op-amps in linear applications.

Very high gain of open loop op-amp as well as its variation with temperature, power supply, and production yield makes the open loop op-amp configuration, unsuitable for linear applications.

Closed Loop Op-amp Configurations

Inverting Amplifier

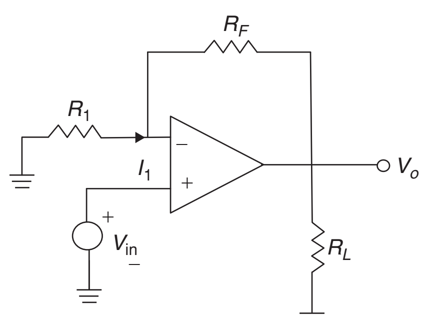


$$I_1 = \frac{V_i}{R_i}, V_0 = -I_1 R_f = \frac{-R_f}{R_1} V_i$$

$$A_v = \frac{-R_f}{R_i}$$

This is voltage shunt feedback circuit

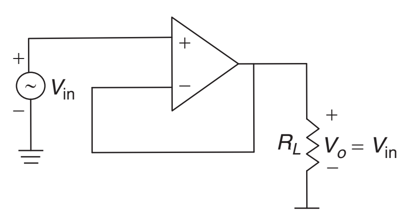
Non-inverting Amplifier



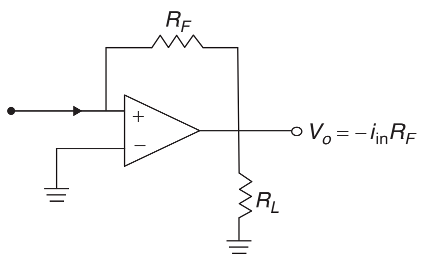
$$A_v = 1 + \frac{R_f}{R_i}$$

This is voltage series negative feedback configuration

Voltage follower



Current to Voltage Converter



The introduction of negative feedback stabilizes the gain; however, it is also smaller than the open loop gain. On the contrary, positive feedback is necessary in oscillator circuits.

The use of negative feedback in a non-inverting amplifier increases the input impedance, and bandwidth, and decreases output resistance, total output offset voltage.

The input resistance of the inverting amplifier is relatively smaller because it depends on the resistance connected in series with the input signal source.

A special case of non-inverting amplifier is voltage follower, while the current to voltage converter is the special case of inverting amplifier. The voltage converter produces output voltage proportional to input current.

Differential Amplifiers

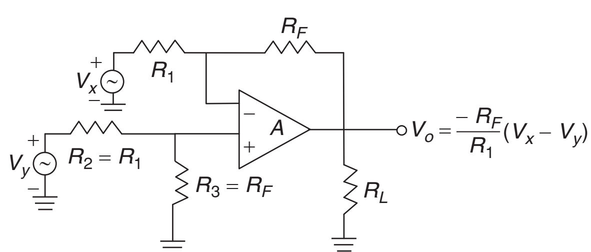


Figure 3 Differential amplifier with one op-amp

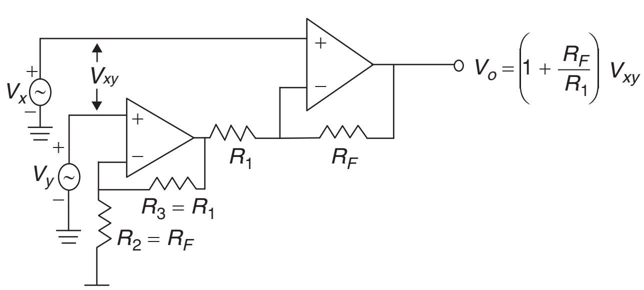
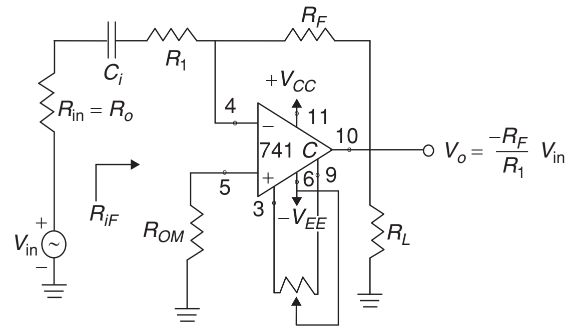


Figure 4 Differential amplifier with two op-amps

Negative feedback is also used in differential amplifier. The differential amplifier with one op-amp has the same characteristics as inverting amplifier, while the amplifier with two op-amps has the same characteristics as the non-inverting amplifier.

AC Amplifier–Inverting Amplifier



The coupling capacitor not only blocks the DC voltage but also sets the low frequency cutoff limit

$$f_L = \frac{1}{2\pi C_i(R_{iF} + R_o)}$$

The high frequency cutoff f_H or high end of the bandwidth depends on the closed loop gain of the amplifier

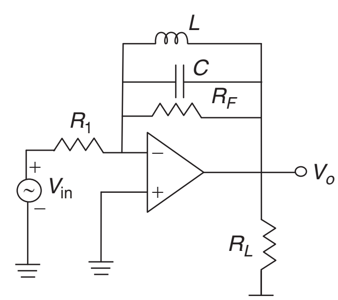
$$f_F = \frac{\text{(unity gain bandwidth)}}{A_F} \times k$$

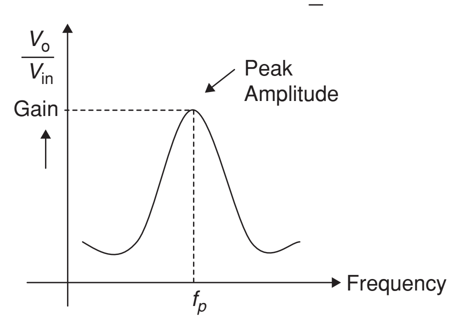
and $k = \dfrac{R_F}{R_1 + R_F}$,

$$A_F = \frac{-R_F}{R_i} \text{ (inverting amplifier)}$$

$$= 1 + \frac{R_F}{R_i} \text{ (non inverting amplifier)}$$

The Peaking Amplifier





The peaking response, that is the frequency response that peaks at a certain frequency, can be obtained by using a parallel LC network with the op-amp

$$f_P = \frac{1}{2\pi\sqrt{LC}}, \text{ if } Q_{\text{coil}} \geq 10$$

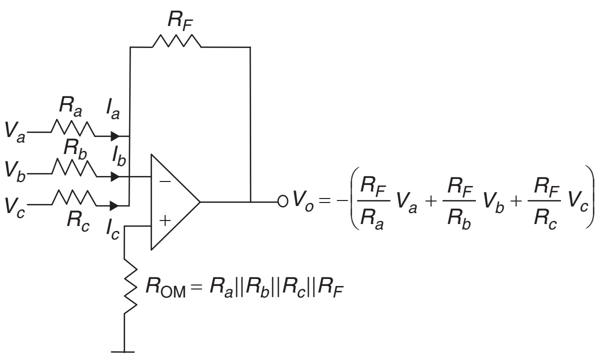
The gain of amplifier at resonance is maximum and is given by $A_F = \dfrac{-R_F \parallel R_P}{R_1}$

R_P = equivalent resistance of the tank current = $Q^2_{\text{coil}} R$,

R = internal resistance of the coil

$$BW = \frac{f_p}{Q_p},\ Q_p = R_F \parallel \frac{R_p}{X_L}$$

Weighted Amplifier

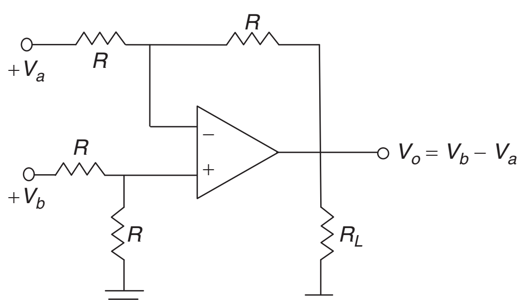


Summing amplifier:

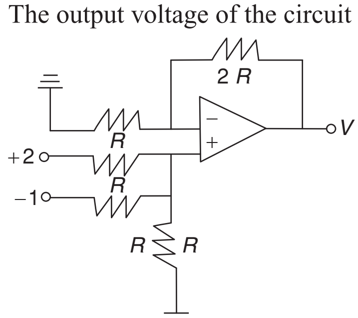
$$R_a = R_b = R_c = R,\ \text{then } V_0 = \frac{-R_F}{R}(V_a + V_b + V_c)$$

Averaging Amplifier: If $\dfrac{R_F}{R} = \dfrac{1}{n}$ for n inputs, then output is average of input voltages

Subtractor:



Example 8: The output voltage of the circuit



(A) 1.0 V
(B) 1.5 V
(C) 2.0 V
(D) 3 V

Solution: (B)

$$V_o = \left(1 + \frac{2R}{R}\right)\left[\frac{R}{R+R}\times 2 + \frac{R}{R+R}\times(-1)\right]$$

$$= 3\left[\frac{1}{2}\times 2 - \frac{1}{2}\right] = 1.5 \text{ V}$$

Example 9: An op-amp has a differential gain of 10^3 and a CMRR of 100, the ouptut voltage of the op-amp with inputs 120 µV and 80 µV will be

(A) 26 mV (B) 41 mV
(C) 100 mV (D) 200 mV

Solution: (B)

$$\text{CMRR} = \left(\frac{A_d}{A_c}\right) = 100 \quad \Rightarrow \quad A_c = \frac{A_d}{100} = 10$$

$$V_d = V_1 - V_2 = 40\ \mu\text{V}$$

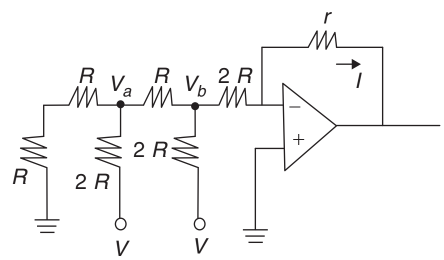
$$V_c = \frac{V_1 + V_2}{2} = 100\ \mu\text{V}$$

$V_o = A_d \cdot V_d + A_c \cdot V_c$

$= 10^3 \times 40 \times 10^{-6} + 10 \times 100 \times 10^{-6}$

$= 41$ mV

Example 10: The current I through resistance r in the circuit is



(A) $\dfrac{-V}{4R}$ (B) $\dfrac{V}{6R}$

(C) $\dfrac{V}{12R}$ (D) $\dfrac{V}{3R}$

Solution: (C)

$$\frac{-V_a}{2R} = \frac{V_a - V}{2R} + \frac{V_a - V_b}{R}$$

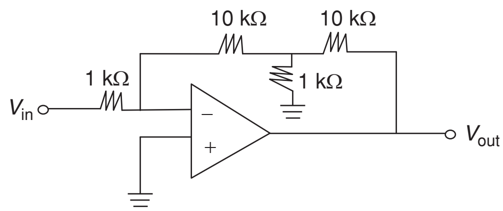
$$4V_a = 2V_b + V \tag{1}$$

$$\frac{V_b - V_a}{R} + \frac{V_b - V}{2R} + \frac{V_b}{2R} = 0 \tag{2}$$

So we get $-V_a = V_b = \dfrac{V}{6}$

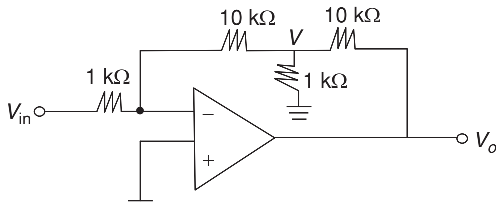
$$I = \frac{V}{12R}.$$

Example 11: Assuming the op-amp to be ideal, the gain $V_{\text{out}}/V_{\text{in}}$ for the circuit shown is?



(A) –1 (B) –20
(C) –100 (D) –120

Solution: (D)
Nodal equation at 'V'



$$\frac{V-0}{10}+\frac{V}{1}+\frac{V-V_{out}}{10}=0$$

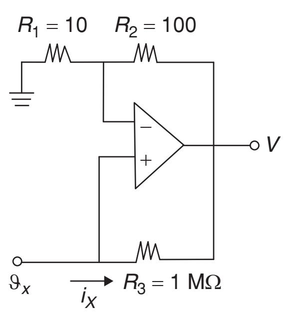
$$12\text{ V}=V_{out}$$

Nodal equation at inverting node, we get

$$\frac{V_{in}-0}{1}=\frac{0-V}{10} \Rightarrow V_{in}=\frac{-V}{10}$$

$$\frac{V_{out}}{V_{in}}=\frac{12}{-1/10}=-120$$

Example 12: Input Resistance $R_{in} = (\vartheta_x/i_x)$ of the circuit is



(A) +100 kΩ (B) –100 kΩ
(C) +1 MΩ (D) –1 MΩ

Solution: (B)
Using KCL at inverting terminal, we have

$$\frac{v_x-V}{R_2}+\frac{V_x-0}{R_1}=0$$

$$\frac{v_x}{V}=\frac{R_1}{R_1+R_2}$$

Using same at Non-inverting terminal

$$i_x=\frac{v_x-V}{R_3}=\frac{v_x-v_x\left(\frac{R_1+R_2}{R_1}\right)}{R_3}$$

$$i_x=\frac{-v_xR_2}{R_1R_3}$$

$$R_{in}=\frac{v_x}{i_x}=\frac{-R_1R_3}{R_2}=-100\text{ k}\Omega.$$

The Integrator

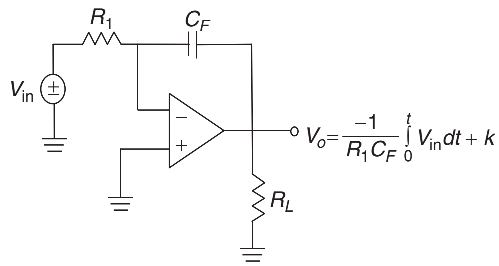


Figure 5 Basic Integrator

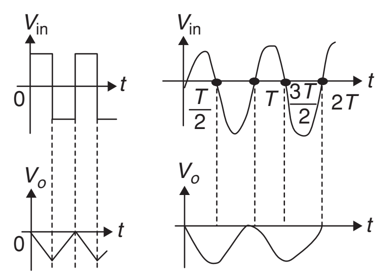
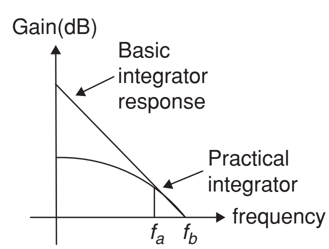
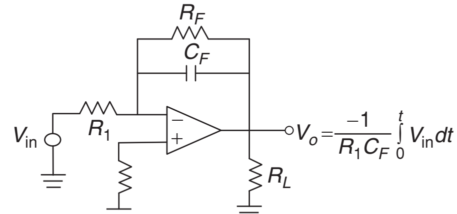


Figure 6 Input–Output wave forms



$$f_b=\frac{1}{2\pi R_1C_F}$$

The stability and low frequency roll-off problem can be corrected by the addition of a resistor R_F as shown in the practical integrator



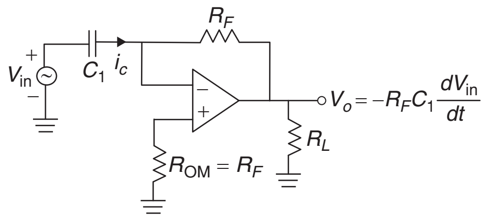
The gain limiting frequency $f_a=\dfrac{1}{2\pi R_FC_F}\cdot R_FC_F$ and R_1C_F values should be selected such that $f_a < f_b$.

The input signal will be integrated properly if the time period 'T' of the signal is larger than or equal to R_FC_F

$$T \geq R_F C_F$$

where, $R_F C_F = \dfrac{1}{2\pi f_a}$

The Differentiator



The output V_o is equal to $R_F C_1$ times the negative instantaneous rate of change of input voltage V_{in} with time

Differentiator performs the reverse of the integrator's function, a cosine wave input will produce a sine wave output, or a triangular input will produce a square wave output.

The frequency at which gain is zero is

$$f_a = \frac{1}{2\pi R_F C_1}$$

The gain $\dfrac{R_F}{X_{C_1}}$ of the circuit increases with increase in frequency at a rate of 20 dB/decade. This makes the circuit unstable, also the input impedance X_{C_1} decreases with increases in frequencies.

Both the stability and the high frequency noise problems can be corrected by the addition of two components R_1 and C_F

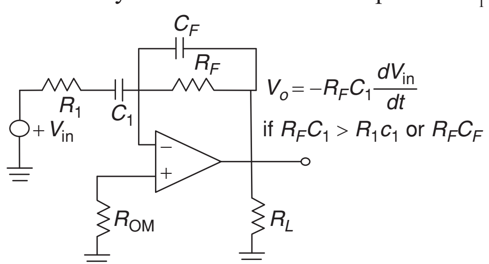


Figure 7 Practical Differentiator

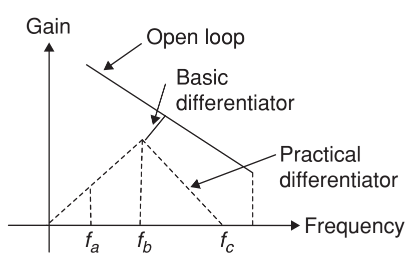


Figure 8 Frequency response

The gain limiting frequency f_b is given by

$$f_b = \frac{1}{2\pi R_1 C_1}$$

Generally the values of f_a, f_b, f_c are

$$f_a = \frac{1}{2\pi R_F C_1},\ f_b = \frac{1}{2\pi R_1 C_1},\ f_c$$

$$f_c = \frac{1}{2\pi R_F C_F}$$

f_c = unity gain bandwidth

The input signal will be differentiated properly if time period (T) of input signal $T \geq R_F C_1$

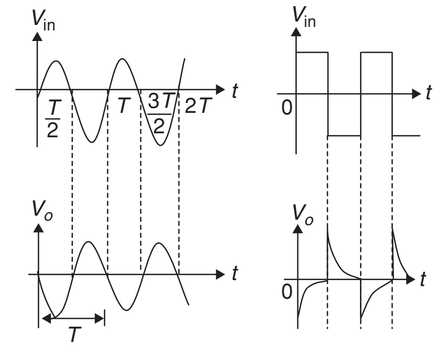
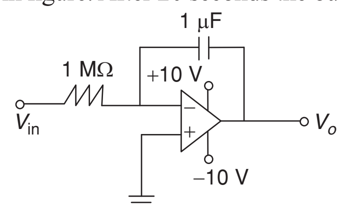


Figure 9 Input–output wave forms

Example 13: A unit positive step is applied at the input of the circuit shown in figure. After 20 seconds the output V_o will be



(A) +20 V (B) + 10 V
(C) –10 V (D) –20 V

Solution: (C)

$$V_o \frac{-1}{sCR} V_i = \frac{-1}{sCR} \cdot \frac{1}{s} (V_i \text{ is unit step})$$

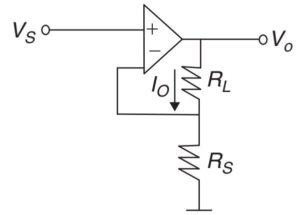
$$= \left[\frac{-1}{s^2 RC}\right]$$

$$V_o = \frac{-1}{RC} t \text{ after 20 seconds}$$

$$V_o = \frac{-1}{1 \times 1} \times 20 = -20 \text{ V}$$

But $\pm V_{sat} = \pm 10$ V so output is –10 V.

Example 14: The current I_o is

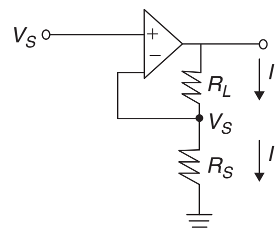


(A) $V_S \cdot \dfrac{R_L}{R_S(R_L + R_S)}$ (B) $\dfrac{V_S}{R_S}$

(C) $\dfrac{V_S}{R_L}$ (D) $V_S\left(\dfrac{1}{R_S} + \dfrac{1}{R_L}\right)$

Solution: (B)

No current flows into input $I_o = \dfrac{V_S}{R_S}$.



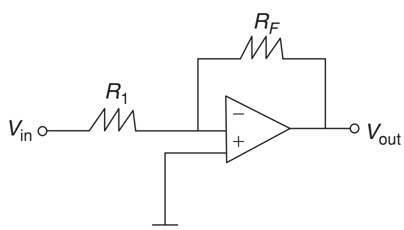
Example 15: The open loop voltage gain of an operational amplifier is 240. The noise level in the output without feedback is 100 mV; if negative feedback with $\beta = \dfrac{1}{60}$ is used, the noise level in the output will be

(A) 1.66 mV (B) 2.4 mV
(C) 4.0 mV (D) 20 mV

Solution: (D)

$$N_f = \frac{N}{1+\beta A} = \frac{100}{1+\frac{1}{60}\times 240} = \frac{100\text{ mV}}{5} = 20\text{ mV}$$

Example 16: For the operational amplifier circuit shown in the figure. What is the maximum possible value of R_1 if the voltage gain required is between –10 and –25? Upper limit of $R_F = 1$ MΩ.



(A) ∞ (B) 1 MΩ
(C) 100 kΩ (D) 40 kΩ

Solution: (C)

$$A_v = \frac{V_o}{V_{in}} = \frac{-R_F}{R_1}$$

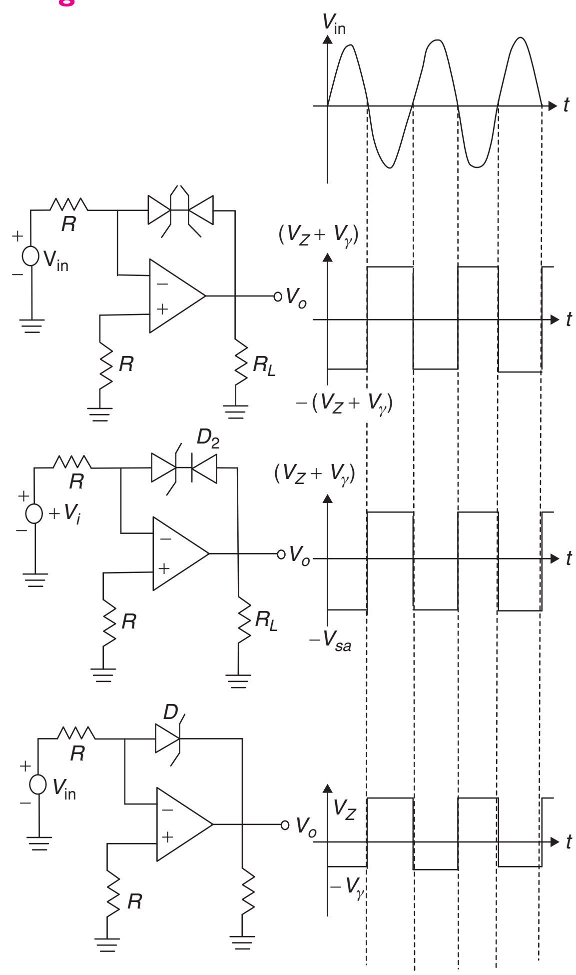
$$\text{for } A_n = -10 = \frac{-R_F}{R_1} \Rightarrow R_1 = 100\text{ k}\Omega$$

$$\text{for } A_n = -25 = \frac{-R_F}{R_1} \Rightarrow R_1 = 40\text{ k}\Omega$$

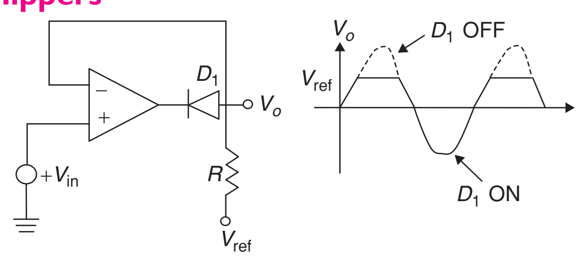
The maximum possible value of

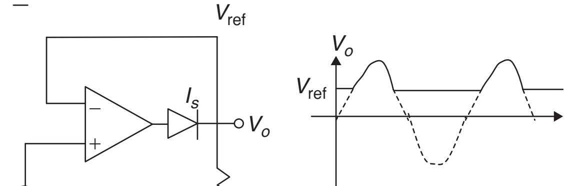
$$R_1 = 100\text{ k}\Omega$$

Voltage Limiters



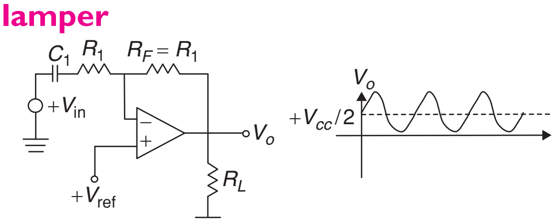
Clippers





If V_{ref} is zero it acts as half wave rectifier

Clamper



FILTERS

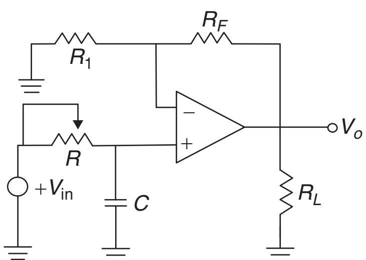
An electric filter is a frequency-selective circuit that passes a specified band of frequencies and blocks or attenuates signals of frequencies outside this band.

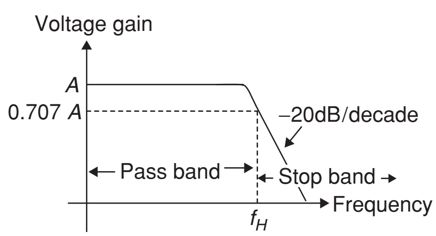
Filters can be classified in a number of ways

1. Analog or digital: Analog filters are designed to process analog signals, while digital filters process analog signals using digital techniques.
2. Passive or active: Elements used in passive filters are resistors, capacitors and inductors. Active filters on other hand employ transistors or op-amps in addition to passive components.
3. Audio or radio frequency filters: The type of element used dictates the operating frequency range of the filter, RC filters are used for audio or low frequency operation, where as LC or crystal filters are employed at RF or high frequencies, especially because of their high Q value.

Most Commonly Used Filters

First order low pass butterworth filter





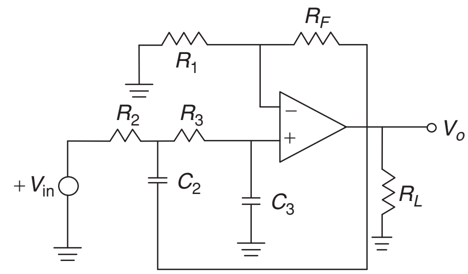
$$V_o = \left(1 + \frac{R_F}{R_1}\right) \frac{V_{in}}{1 + j\left(\frac{f}{f_H}\right)}$$

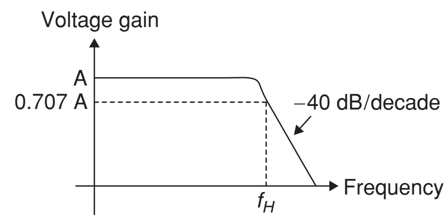
f = frequency of input signal

$$f_H = \frac{1}{2\pi RC} = \text{high cutoff frequency of filter}$$

$$\left|\frac{V_0}{V_{in}}\right| = \frac{A_F}{\sqrt{1 + \left(\frac{f}{f_H}\right)^2}}, \quad \phi = \tan^{-1}\left(\frac{f}{f_H}\right)$$

Second order low pass butterworth filter



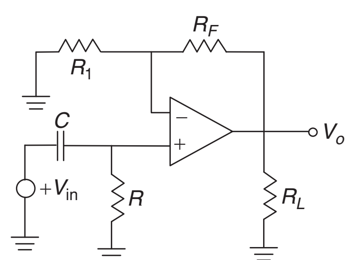


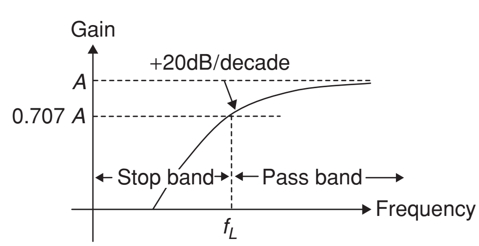
$$f_H = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}}$$

$$\left|\frac{V_o}{V_{in}}\right| = \left|\frac{A_F}{\sqrt{1 + \left(\frac{f}{f_H}\right)^2}}\right|$$

$$A_F = 1 + \frac{R_F}{R_1} \text{ pass band gain}$$

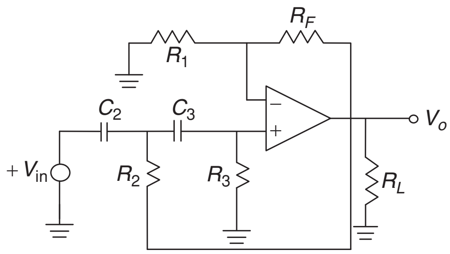
First order high pass butterworth filter

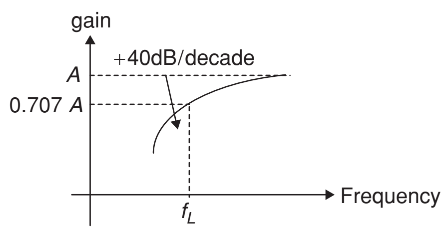




$$\left|\frac{V_0}{V_{in}}\right| = \frac{A_F\left(\frac{f}{f_L}\right)}{\sqrt{1 + \left(\frac{f}{f_H}\right)^2}}, \quad f_L = \frac{1}{2\pi RC}$$

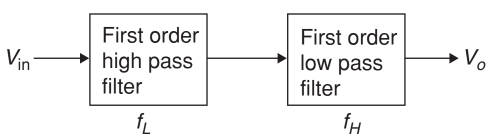
Second order high pass butterworth filter

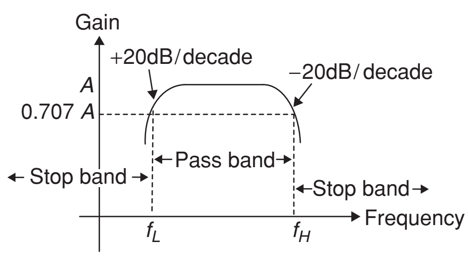




$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{1+\left(\frac{f_L}{f}\right)^4}},\ f_L = \frac{1}{2\pi\sqrt{R_2R_3C_2C_3}}$$

Wide band pass filter





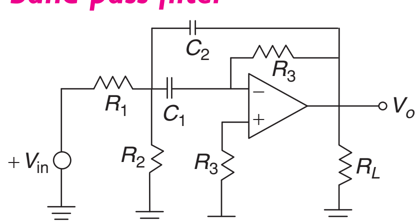
If figure of merit or Q factor $Q < 10$, then the filter is called as wide band pass filter

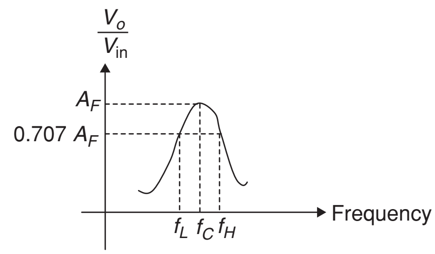
$$Q = \frac{f_0}{BW} = \frac{f_0}{f_H - f_L}$$

$$f_0 = \sqrt{f_H f_L}$$

f_H = high cutoff frequency
f_L = low cutoff frequency
f_0 = resonance frequency

Narrow band pass filter





if $C_1 = C_2 = C$

$$R_1 = \frac{Q}{2\pi f_c C A_F},\ R_2 = \frac{Q}{2\pi f_c C(2Q^2 - A_F)},$$

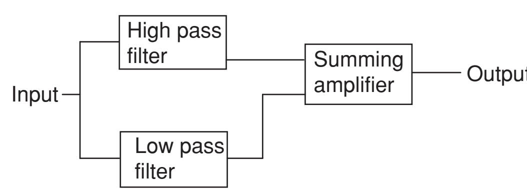
$$R_3 = \frac{Q}{\pi f_c},\ A_F = \frac{R_3}{2R_1},\ A_F = \text{gain at } f_c$$

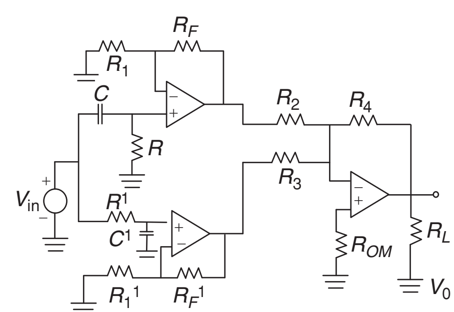
$$A_F < 2Q^2$$

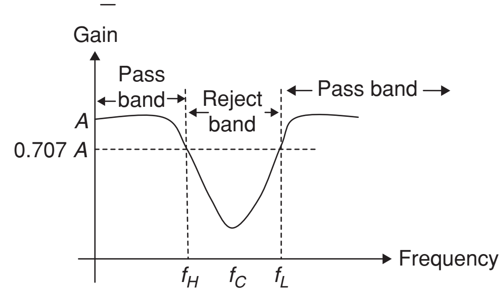
Another advantage of the multiple feedback filter is, its centre frequency f_c, can be changed, to a new frequency f_c', without changing the gain or bandwidth, this is accomplished by changing R_2 to R_2' so that

$$R_2' = R_2\left(\frac{f_c}{f_c'}\right)^2$$

Wide band reject filter

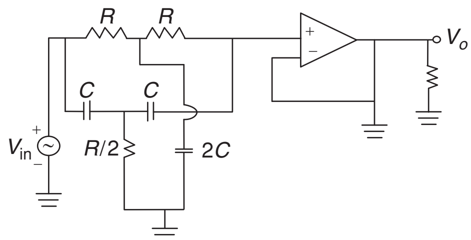




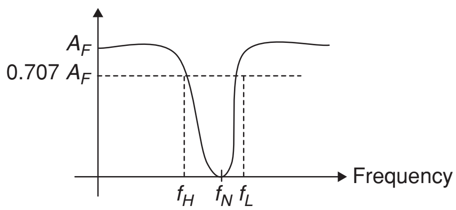


Wide band stop or wide band elimination filter, have lower (Q < 10); narrow band reject filter or notch filter will have higher Q.

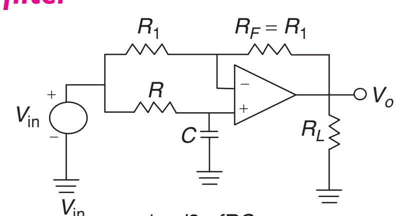
Narrow band reject filter



$$f_N = \frac{1}{2\pi RC}$$



All pass filter



$$V_0 = \frac{1 - j2\pi fRC}{1 + j2\pi fRC}$$

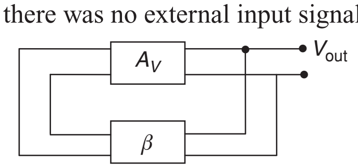
The phase shift between V_0 and V_{in} is a function of input frequency 'f'

$$\phi = -2\tan^{-1}\left(\frac{2\pi fRC}{1}\right)$$

Oscillators

Theory of Sinusoidal Oscillators

To build a sinusoidal oscillator, we need to use an amplifier with positive feedback, to use the feedback signal in place of the input signal. If the feedback signal is large enough and has the correct phase, there will be an output signal even though there was no external input signal.



In any oscillator, the loop gain $A_v\beta$ is greater than 1, when the power is first turned on. A small starting voltage (thermal noise) is applied to the input terminals and output voltage builds up, after the output voltage reaches a certain level, $A_v\beta$ automatically decreases to 1, and the peak to peak output becomes constant.

Gain without feedback $= A_v$

Gain with feedback $A_f = \dfrac{A_v}{A_V\beta}$

If $A_v\beta = 1 \Rightarrow A_f = \infty$, which means we can get the output with no input. However, oscillator works on circuit transients.

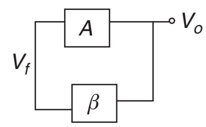
Bark–Hausen's criterion:

1. Magnitude of loop gain is unity
2. Phase angle of loop gain is 0° or 360°

Steps to solve an Oscillator problem:

1. Find β, $\beta = \dfrac{V_f}{V_0}$

   $\beta = \beta_{real} + \beta_{imaginary}$



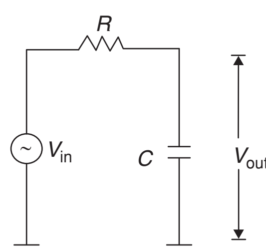
2. Find $A = \dfrac{V_0}{V_f}$

   Equate $= A\beta = 1$. Equate real parts and imaginary parts to get the frequency of oscillations and conditions for sustained oscillation.

The Wien Bridge Oscillator

The Wien bridge Oscillator is standard circuit for low to moderate frequencies in the range of 5 Hz to about 1 MHz.

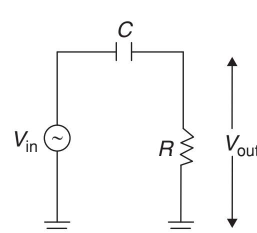
Lag circuit



$$\frac{V_{out}}{V_{in}} = \frac{X_c}{\sqrt{R^2 + X_c^2}}$$

The phase angle $\phi = -\tan^{-1}\left(\dfrac{R}{X_c}\right)$ negative sign in phase angle represents the output voltage lags the input voltage.

Lead circuit



$$\frac{V_{out}}{V_{in}} = \frac{R}{\sqrt{R^2 + X_c^2}}$$

$$\phi = \tan^{-1}\left(\frac{X_c}{R}\right)$$

The phase angle is positive, means the output voltage leads the input voltage.

Lead-lag circuit

Wien bridge oscillator uses resonant feedback circuit called a lead-lag circuit.

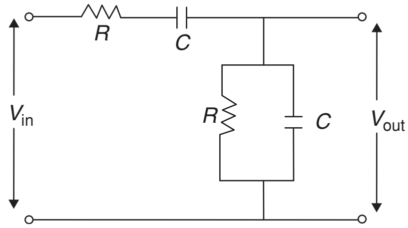


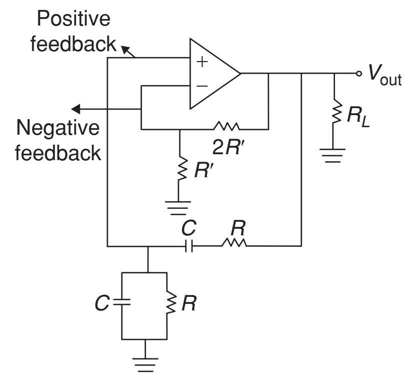
Figure 10 Lead-lag network

At very low frequencies the series capacitor appears, open to the input signal, and there is no output signal, at very high frequencies, the shunt capacitor looks shorted, and there is no output. In between these extremes, the output reaches a maximum value at resonant frequency f_r. at this frequency the feed back fraction B reaches a maximum value of 1/3.

Resonant frequency $f_r = \dfrac{1}{2\pi RC}$

$$\beta(\text{gain}) = \frac{1}{\sqrt{9-\left(\dfrac{X_c}{R}-\dfrac{R}{X_C}\right)^2}},$$

$$\phi = \tan^{-1}\left(\frac{X_c/R - R/X_c}{3}\right)$$



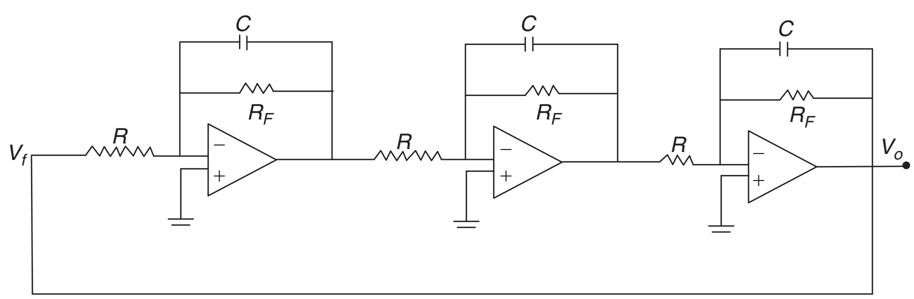
$$f_r = \frac{1}{2\pi RC}$$

Wien bridge oscillator uses both positive and negative feedback. The gain of the amplifier $(A_V) = 1 + \dfrac{2R'}{R'} = 3.$ at resonance ($X_c = R$), the gain of lead-lag network $\beta = \dfrac{1}{3}$. The loop gain $= A_V\,\beta = 1$.

The Wien bridge acts like a notch filter, a circuit with zero output at one particular frequencies, for a Wien bridge, the notch frequency equals to, $f_r = \dfrac{1}{2\pi RC}$.

Although it is superb at low frequencies, the Wien-bridge oscillator is not suited to high frequencies (well, above 1MH_Z). The main problem is the limited band width of op-amp.

RC–Phase Oscillator



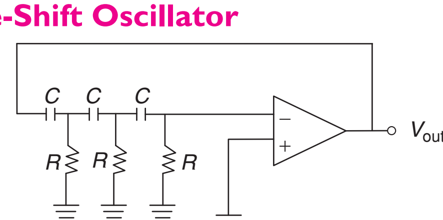
Properties:

1. Each section gives 120° phase shift
2. Frequency of oscillations required is

$$F = \frac{\sqrt{3}}{2\pi R_F C}$$

3. Condition for sustained oscillations: $R_F = 2R$
4. Minimum gain required is $|A| \geq 2$

Phase-Shift Oscillator



Phase-shift oscillator with three lead circuit in the feedback path, at some frequency the total phase shift of the three lead circuit is 180°. The amplifier has an additional 180° of phase shift, because the signal drives the inverting input. As a result, the phase shift around the loop will be 360° equal to 0°.

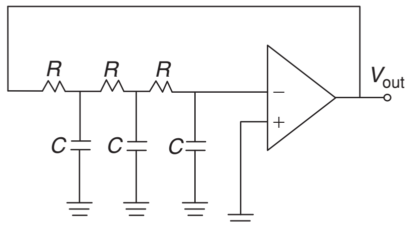
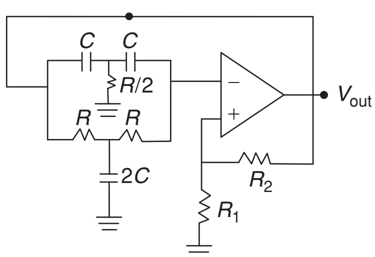


Figure 11 Phase shift oscillator with lag circuits

Properties:

1. Each RC section doesn't produce 60° phase shift due to loading effect. However 3 RC sections together produces a phase shift of 180°.
2. Frequency of oscillations $f = \dfrac{1}{2\pi RC\sqrt{6}}$.
3. Condition for sustained oscillations was $R_F = 29R_1$.
4. Minimum gain required was $|A| \geq 29$

Twin-T Oscillator



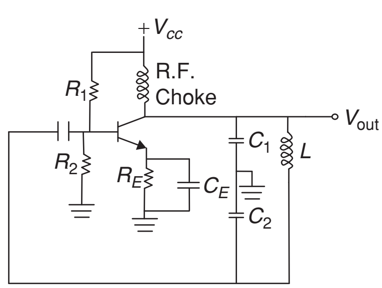
$$f_r = \frac{1}{2\pi RC}$$

The positive feedback to the non-inverting input is through a voltage divider. The negative feedback is through the twin T-filter.

To ensure that the oscillation frequency is close to the notch frequency, the voltage divider should have R_2 much larger than R_1, This forces the oscillator to operate at a frequency near the notch frequency.

The limitation is it works only at one frequency, it cannot be easily adjusted over a large frequency range.

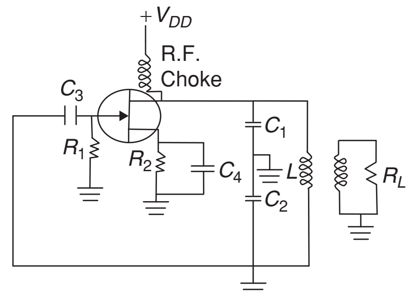
The Colpitts Oscillator



CE connection, Colpitts oscillator resonant frequency $f_r = \dfrac{1}{2\pi\sqrt{LC}}$

$$C = \frac{C_1C_2}{C_1 + C_2},$$

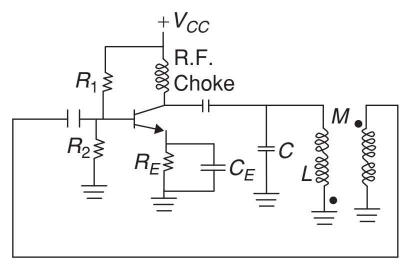
for $A_V B \geq 1$, $B = \dfrac{C_1}{C_2}$, $A_V = \dfrac{C_2}{C_1}$



JFET Oscillator has less loading effect on tank circuit. Resonant frequency $f_r = \dfrac{1}{2\pi\sqrt{LC}}$

$$C = \frac{C_1C_2}{C_1 + C_2},\ B = \frac{C_1}{C_2},\ A_{V(\min)} = \frac{C_2}{C_1}$$

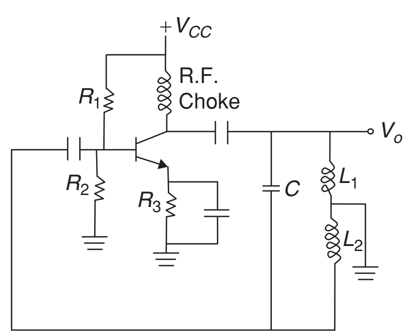
Armstrong Oscillator



$$f_r = \frac{1}{2\pi\sqrt{LC}},\ B = \frac{M}{L},\ A_{V(\text{mid})} = \frac{L}{M}$$

M-mutual inductance at output

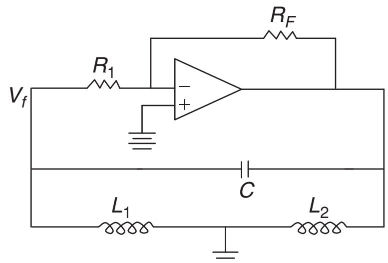
Hartley Oscillator



Hartley oscillator

$$f_r = \frac{1}{2\pi\sqrt{LC}},\ L = L_1 + L_2,\ B = \frac{L_2}{L_1},\ A_{V(\min)} = \frac{L_1}{L_2}$$

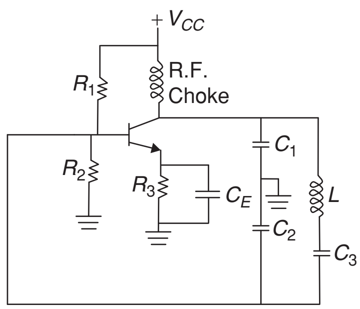
Hartley oscillator by using op-amp:



Frequency of Oscillation $f = \dfrac{1}{2\pi\sqrt{L_{eq}\cdot C}}$

$L_{eq} = L_1 + L_2 + 2M$ (series aiding)
$= L_1 + L_2 - 2M$ (series opposing)

Clapp oscillator

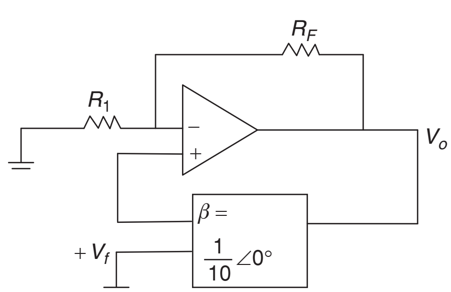


$$f_r = \frac{1}{2\pi\sqrt{LC}},$$

$$C = \frac{1}{1/c_1 + 1/c_2 + 1/c_3},\ B = \frac{C_1}{C_2}$$

$$A_{V(\text{mid})} = C_2/C_1$$

Example 16: Relation between R_1 and R_2 for sustained Oscillations if $\beta = \frac{1}{10}\angle 0°$ for the following circuits.



(A) $R_F = 4R_1$ (B) $R_F = 10R_1$
(C) $R_F = 2R_1$ (D) $R_F = 9R_1$

Solution: (D)

$$A = 1 + \frac{R_F}{R_1}$$

$$A\beta = 1$$

$$\Rightarrow \left[1 + \frac{R_F}{R_1}\right]\frac{1}{10}\angle 0° = 1\angle 0°$$

$$1 + \frac{R_F}{R_1} = 10$$

$$R_F = 9R_1$$

Example 17: A Colpitts oscillator has a coil with an inductance of 50 μH and is tuned by a capacitor 400 pF across amplifier input and 200 pF across the output. Then the frequency of oscillation and the minimum gain for maintaining oscillations?

(A) 1.95 MHz, 3 (B) 1.95 MHz, 2
(C) 2.9 MHz, 3 (D) 2.9 MHz, 2

Solution: (B)
For Colpitts oscillator

$$f_0 = \frac{1}{2\pi\sqrt{LC_{eq}}},\ C_{eq} = \frac{C_1C_2}{C_1 + C_2}$$

$$C_{eq} = \frac{400\times 200}{600} = 133.33\text{ pF}$$

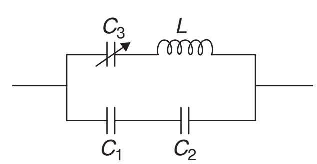
$$f_0 = \frac{1}{2\pi\sqrt{50\times 133.33\times 10^{18}}} = 1.95\text{ MHz}$$

For maintaining oscillations, $A\beta \Rightarrow 1$

$$A_{\text{loop}} = A_{v0}\cdot\frac{C_2}{C_1} = 1$$

$$A_{v0} = \frac{C_1}{C_2} = \frac{400}{200} = 2$$

Example 18: A clapp oscillator has the following circuit components C_1 = 5000 pF, C_2 = 500 pF, L = 50 μH and C_3 is a 50 to 250 pF variable capacitor. Find out the tuning frequency range?



(A) 1.98 – 10.34 MHz (B) 2.34 – 11.56 MHz
(C) 3.35 – 12.5 MHz (D) 5.34 – 15.4 MHz

Solution: (C)

$$f_0 = \frac{1}{2\pi\sqrt{LC_{eq}}},\ \frac{1}{C_{eq}} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}$$

$$C_{eq} = \frac{5000\times 500\times 50}{5000\times 500 + 5000\times 50 + 500\times 50}$$

$= 45.045$ pF for $C_3 = 50$ pF

$$f_0 = \frac{1}{2\pi\sqrt{50\times 45.045\times 10^{-18}}} = 3.35\text{ MHz}$$

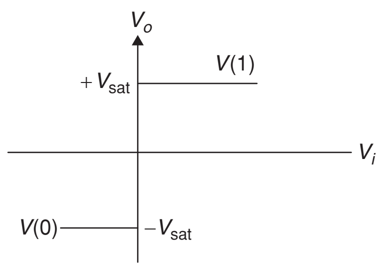
$C_{eq} = 161.29$ pF for $C_3 = 250$ pF

Then $f_0 = 12.5$ MHz

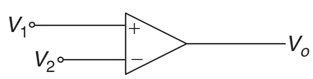
Waveform Generators and Wave Shaping Circuits

Comparators

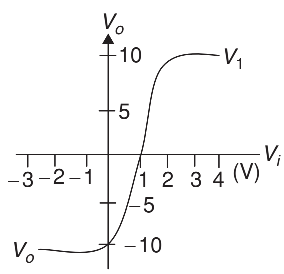
An analog comparator or simply comparator has two input voltages V_1 and V_2 and one output voltage V_o. Often one of the Input (V_2) is a constant reference voltage V_R, and the other is a time varying signal.



1. Transfer characteristics of ideal comparator

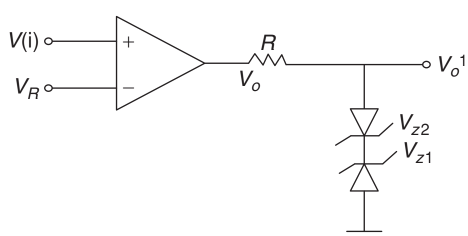


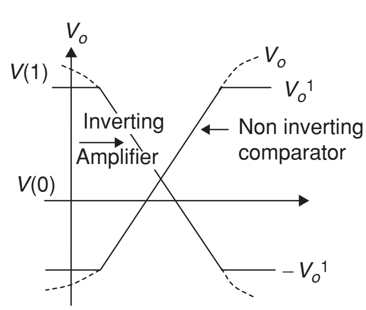
2. Op-amp operated in open loop becomes a comparator



3. Transfer characteristics of practical comparator.

   The Input is compared with the reference and the output is digitized into one of two states: $V_o = V(0)$ when $v(i) < V_R$ and $V_o = V(1)$ when $V_i > V_R$.





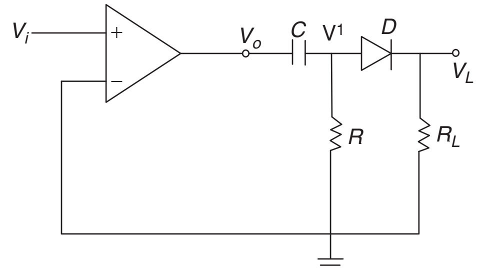
Practical comparator and transfer characteristics:

To obtain limiting output voltages which are independent of the power supply voltages, a Resistor R_1 and two back to back Zener diodes are added to clamp the output of comparator.

One more advantage of adding the Zener diodes is that the limiting may be much sharper for V_0^1 than for V_0 and disadvantage is poor transient response of the avalanche diode.

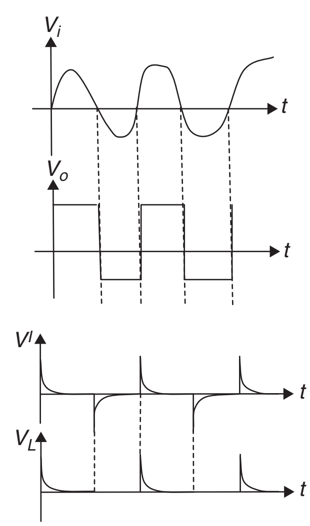
Square wave generation from sinusoid

The comparator performs highly non-linear wave shaping because the output bears no resemblance to the input wave form.



A zero crossing detector converts the sinusoid input (V_i) into a square wave, (V_0)

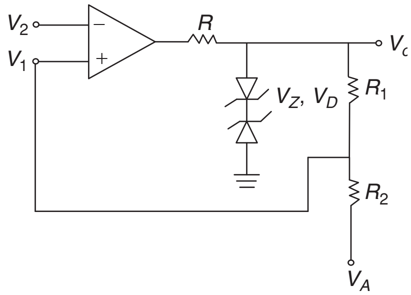
The pulse wave forms V' and V_L result from V_0 being fed into a short time-constant RC Circuit in cascade with a diode clipper.



Here a sinusoid has been converted into either a square wave or a pulse train.

Spurious positive and negative voltage spikes called noise super imposed on the input signal in the neighbour hood of the amplitude (V_R) may cause the output to chatter (change from one binary voltage to another) several times before settling down to the correct level. This difficulty can be avoided if positive feedback or regeneration is added to a comparator.

Regenerative Comparator (Schmitt Trigger)



Schmitt trigger

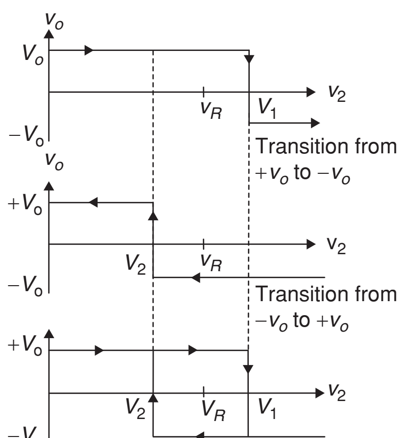
$$V_o = V_z + V_D,$$

assume $v_2 < v_1$, so that $V_o = +V_o$, and the voltage at the non inverting terminal (v_1) is

$$V_1 = V_A + \frac{R_2}{R_1 + R_2}(V_o - V_A)$$

If v_2 is now increased, the V_o remains constant at V_o, and $v_1 = V_1$ = constant until $v_2 = V_1$, at this threshold critical, or triggering voltage the output regeneratively switches to $v_o = -V_0$, and remains at this value as long as $v_2 > V_1$.

The voltage at the non inverting terminal (v_1) for $v_2 > V_1$ is $v_1 = V_A - \dfrac{R_2}{R_1 + R_2}(V_o + V_A) = V_2$.



Hysteresis

If we decrease v_2, the output remains at $-V_0$, until v_2 equals the voltage at positive terminal, or until $v_2 = V_2$. At this stage, regenerative transition takes place and the output returns to $+V_0$ almost instantly. One of the most important uses made of the Schmitt trigger is to convert a slowly varying input voltage into an output wave from displaying an abrut, almost discontinuous change.

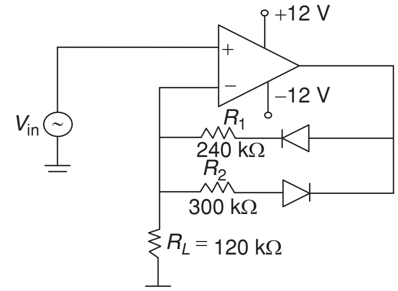
Note: $V_2 < V_1$, and the difference between these two values is called hysteresis

$$V_H = V_1 - V_2 = \frac{2R_2V_0}{R_1 + R_2}$$

UTP: (V_1) Output changes form $+V_{sat}$ to $-V_{sat}$

LTP: (V_2) Output changes form $-V_{sat}$ to $+V_{sat}$

Example 20: Find UTP, LTP and Hysteresis width for the following circuit assuming diodes are ideal.



Solution:

UTP: $V_0 = +V_{sat}$; Upper diode is 'ON'.

$$V_{UTP} = +V_{sat} \cdot \frac{R_L}{R_1 + R_L}$$

$$V_{UTP} = \frac{12(120\text{ K})}{(360\text{ K})} = +4\text{ V}$$

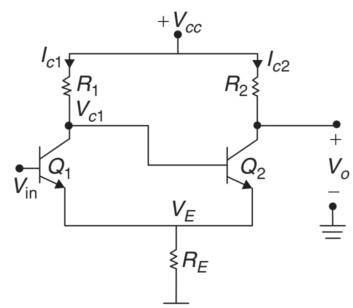
LTP: $V_0 = -V_{sat}$; Lower diode is 'ON'

$$V_{LTP} = \frac{V_{sat} * R_L}{R_L + R_2}$$

$$V_{LTP} = \frac{-12(120\text{ K})}{(420\text{ K})} = -3.4\text{ V}$$

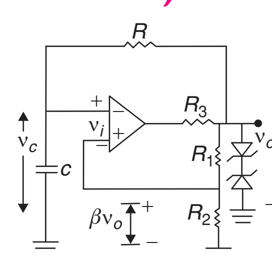
Hysteresis width = $V_{UTP} - V_{LTP}$ = 7.4 V

Emitter coupled schmitt trigger

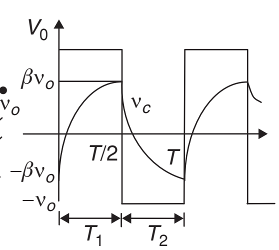


The basic Emitter coupled pair can be converted into a regenerative comparator. The resistances R_1 and R_2 are unequal ($R_1 > R_2$) and hence Q_1 and Q_2 have different currents when saturated. This difference results in the hysteresis as different input voltages are required to saturate and cutoff Q_1 and Q_2.

Square Wave Generator (Astable Multivibrator)



A square wave



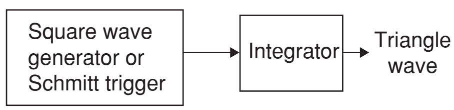
Output and capacitor voltage wave forms

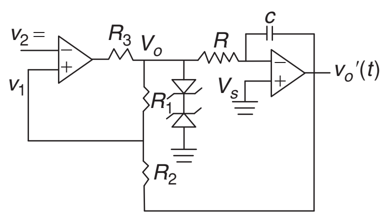
The inverting Schmitt trigger can be used to obtain a free running square wave generator by connecting an RC network between output and the inverting input.

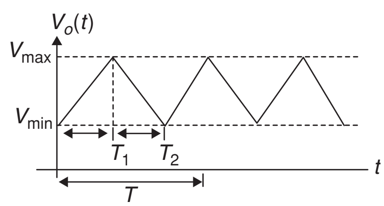
$$V_i = v_c - \beta v_0 = v_c - \frac{R_2}{R_1 + R_2} v_0$$

$$T = 2RC\ell_n\left(1 + \frac{2R_1}{R_2}\right),\ f_0 = \frac{1}{2RC} \text{ for } R_2 = 1.16R_1$$

Triangle Wave Generator







Output wave form, $T_1 = T_2$ if $V_s = 0$,

$$V_{max} = V_R\left(\frac{R_1 + R_2}{R_1}\right) + V_0\frac{R_2}{R_1}$$

$$V_{min} = V_R\left(\frac{R_1 + R_2}{R_1}\right) - V_0\frac{R_2}{R_1}$$

Peak to peak swing

$$V_{max} - V_{min} = 2V_0\frac{R_2}{R_1}$$

$$T = \frac{4R_2RC}{R_1},\ f = \frac{1}{T}$$

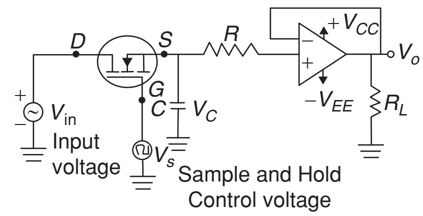
The frequency is independent of v_0. The maximum frequency is limited by either the slew rate of the integrator or its maximum output current, which determines the charging rate of C.

If unequal sweep intervals $T_1 \neq T_2$ is required apply $V_s \neq 0$ for integrator.

Then $\frac{T_1}{T_2} = \frac{V_0 - V_s}{V_0 + V_s}$ duty cycle $\frac{T_1}{T_0} = \delta = \frac{1}{2}\left(1 - \frac{V_s}{V_0}\right)$

Sample and Hold Circuit

The sample and hold circuit as it name implies, samples an input signal and holds on to its last sampled value until the input is sample again.



The Analog signal V_{in} to be sampled is applied to the drain, and sample and hold central voltage (V_s) is applied to the gate of E-MOSFET.

During positive portion of V_s, the MOSFET conducts and acts as a closed switch. This allows the input voltage to charge capacitor C, i.e., input voltage appears across C and in turn at the output.

When V_s is zero, the E-MOSFET is off (non-conductive) and acts as an open switch, the only discharge path for C is through op-amp. However the input resistance of op-amp is very high, so voltage across C is retained.

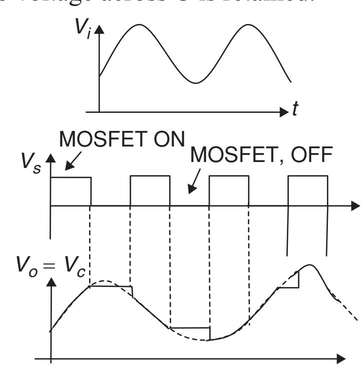
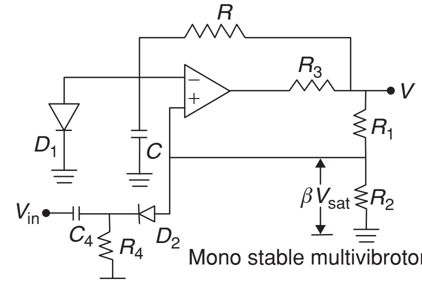


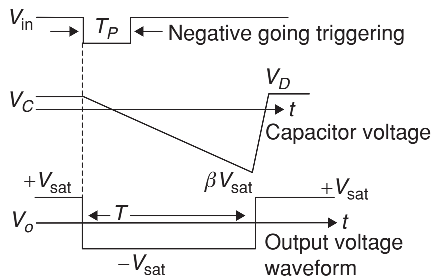
Figure 12 Input and output waveforms

To obtain close approximation of the input wave form, the frequency of the sample and hold control voltage must be significantly higher than that of the input. The sample and hold circuit is commonly used in digital interfacing and communications.

Monostable Multivibrator

Monostable multivibrator has one stable state and other is quasi-stable state. The circuit is useful for generating single output pulse of adjustable time duration, in response to a triggering signal.





V_D – diode forward voltage

$$T = RC\ell n\frac{(1+V_D/V_{sat})}{1-\beta}$$

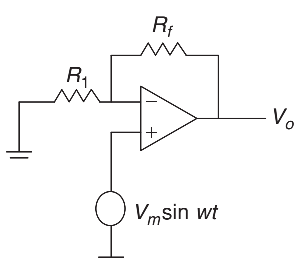
$$\beta = \frac{R_2}{R_1 + R_2}$$

if $V_{sat} >> V_D$, $R_1 = R_2$ So that $\beta = 0.5$, then $T = 0.69\ RC$.

Let us assume that in the stable state, the output is at $+V_{sat}$. The diode D_1 conducts and V_c the voltage across capacitor gets clamped to 0.7 V.

The voltage at (+) input terminal through R_1, R_2 potentiometer divider is $+\beta V_{sat}$. Now if a negative trigger of magnitude V_1 is applied to the (+) terminal. So that the effective signal at this terminal is less than 0.7 V. i.e., ([$\beta\ V_{sat} + (-V_1)$ < 0.7 V). The output of op-amp will switch from $+V_{sat}$ to $-V_{sat}$ through the resistance R. The voltage at the (+) input terminal is now $-\beta V_{sat}$, when capacitor C voltage becomes just slightly more negative than this voltage. The output of op-amp switches back to $+V_{sat}$. The capacitor C now starts charging to $+V_{sat}$ through R until V_c clamped to 0.7 V.

Example 21:



The op-amp has a slew rate of 1 V/μ second. The unity gain frequency is 1 MHz and the output saturation levels are of ±14 V. What is the maximum output frequency at which undistorted output can be obtained?

(A) 15.4 kHz (B) 13.8 kHz
(C) 12.39 kHz (D) 11.36 kHz

Solution: (D)

$$\text{Slew rate} = \left.\frac{dV}{dt}\right|_{\max} = \omega V_m$$

$$2\pi f_{\max} V_m = \text{Slew rate}$$

$$f_{\max} = \frac{\text{slew rate}}{2\pi V_m}$$

Here slew rate = 1 V/μs

V_m = 14 V

$$f_{\max} = \frac{1/10^{-6}}{2\pi \times 14} = 11.36 \text{ kHz}$$

Example 22: The values of R_f, R_1 for a non inverting amplifier to provide maximum low frequency gain for a bandwidth of 100 kHz are

(A) 9 kΩ, 1 kΩ
(B) 19 kΩ, 1 kΩ
(C) 29 kΩ, 1 kΩ
(D) Cannot be determined

Solution: (A)

For 1 MHz bandwidth, gain = 1 (unity)

$$\text{For 0.1 MHz, gain } = \frac{1}{0.1} = 10$$

$$\text{Closed loop gain } = 10 = 1 + \frac{R_f}{R_1}$$

$\Rightarrow R_1 = 1$ kΩ, $R_f = 9$ kΩ.

Example 23: The maximum peak to peak amplitude of the input signal of frequency 100 kHz for undistorted output?

(A) 15.9 V (B) 3.18 V
(C) 2.12 V (D) Not possible

Solution: (B)

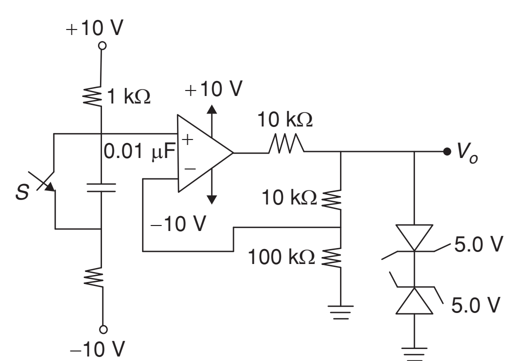
Slew rate = $2\pi f_{\max} \cdot V_m$

$$\text{Peak amplitude of input } = \frac{\text{Slew rate}}{2\pi f_{\max}}$$

$$= \frac{1/10^{-6}}{2\pi \times 100 \times 10^3} = 1.59 \text{ V}$$

Peak to peak (P–P) = 2 × 1.59 V = 3.18 V

Example 24: The switch S in the circuit was initially closed and opened at time t = 0, you may neglect the zener diode forward voltage drops. What is the behaviour of V_{out} for $t > 0$?



(A) It makes a transition from –10 V to +10 V at t = 12.98 μS.
(B) It makes a transition from –5 V to +5 V at t = 2.57 μS.

(C) It makes a transition from + 5 V to –5 V at $t = 2.57$ µS.
(D) It makes a transition from + 10 V to –10 V at $t = 12.95$ µS.

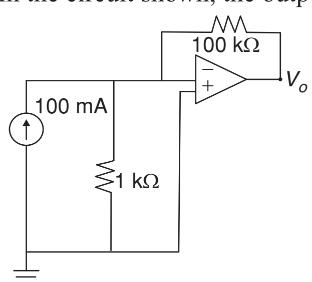
Solution: (C)
It is a limiter circuit.
It makes a transition from +5 V to –5 V

$$20(1-e^{-t/Rc}) = 5\times\frac{100}{110}$$

= Voltage Across 100 kΩ

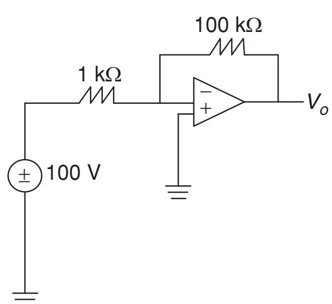
$RC = 0.01 \times 10^{-6} \times 10^{3}$
$t = 2.57$ µS

Example 25: In the circuit shown, the output voltage is



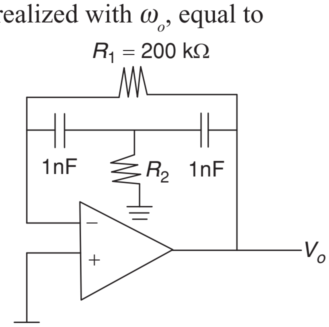
(A) – 9 V (B) – 10 V
(C) + 10 V (D) + 9 V

Solution: (B)
We can observe the current source 100 mA, in parallel with resistance 1 kΩ as



So $V_0 = \dfrac{-100}{1000}\times 100 = -10$ V

Example 26: In the active filter circuit, if $Q = 1$, a pair of poles will be realized with ω_o, equal to



(A) 1000 rad/s (B) 100 rad/s
(C) 10 rad/s (D) 1 rad/s

Solution: (A)

$$\frac{V_o(s)}{V_i} = \frac{\dfrac{s}{R_2C_1}}{s^2 + \dfrac{C_1+C_2}{R_1C_1C_2}s + \dfrac{1}{R_1R_2C_1C_2}}$$

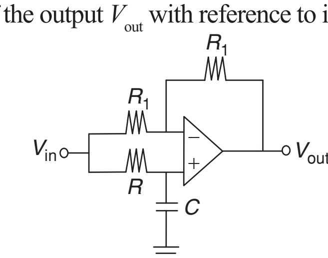
$$A_v(s) = \frac{(\omega_o/Q)A_o s}{s^2 + \left(\dfrac{\omega_o}{Q}\right)s + \omega_o^{\,2}}$$

By comparing, we have $\dfrac{\omega_o}{Q} = \dfrac{C_1+C_2}{R_1C_1C_2}$

$$\omega_o = Q\left(\frac{C_1+C_2}{R_1C_1C_2}\right) = 1\times\frac{(1+1)\times 10^{-9}}{200\times 10^{3}\times 10^{-18}}$$

$= 1000$ rad/s.

Example 27: For the circuit with an ideal op-amp, the maximum phase shift of the output V_{out} with reference to input V_{in} is



(A) –90° (B) 0°
(C) +90° (D) ±180°

Solution: (D)

$$V_+ = \frac{V_{in}}{1+j\omega RC}$$

$V_- = V_+$ (as its ideal op-amp)

$$\frac{V_{in}-V_-}{R_1} = \frac{V_- - V_o}{R_1}$$

$$V_o = 2V_- - V_{in} = 2V_+ - V_{in} = \left[\frac{2}{1+j\omega RC} - 1\right]V_{in} = \frac{1-j\omega RC}{1+j\omega RC}\cdot V_{in}$$

$\angle(V_o/V_i) = -2\tan^{-1}\omega RC$
for $-90° \le 0 \le +90°$, phase shift $\angle(V_o/V_i) = \pm 180°$

Power Supplies

The function of voltage regulator is to provide, astable DC voltage for powering other electronic circuits.

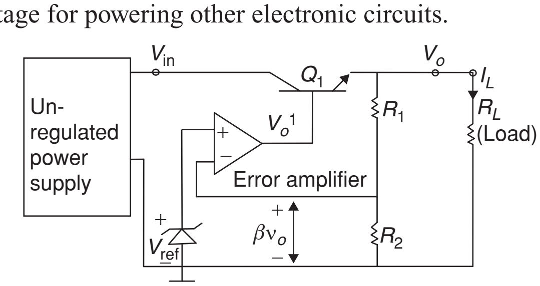


Figure 13 A regulated power supply

The circuit consists of four parts

1. Reference voltage Circuit
2. Error amplifier
3. Series pass transistor(Q_1)
4. Feedback network.

The power transistor Q_1 is in series with the unregulated DC voltage V_{in} and regulated output V_0. So it absorbs the difference between these two voltages, for fluctuations in voltages. Q_1, is connected as emitter follower and it provides sufficient current gain to drive load. The output voltage is sampled by $R_1 - R_2$ divider and feedback to the (−) input terminal, of the error-amplifier, the sampled voltage is compared with the reference voltage V_{ref} (obtained by a zener diode). The output of error amplifier drives the Q_1 transistor.

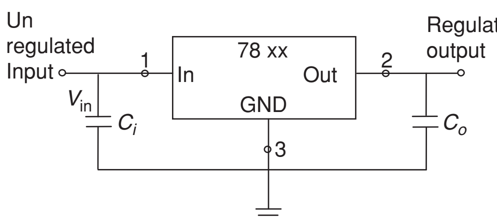
$$\beta = \frac{R_2}{R_1 + R_2}$$

This in turn, reduces the output voltage V_o, of the diff amp $(v_0^1 = \beta v_0)$, so V_0 follows v_o^1, so V_o also reduces. Hence, increase in V_0 is nullified, and reduction in output voltage also regulated.

IC Voltage Regulators

78XX series are three terminal, positive fixed voltage regulator available in 05, 06, 08, 12, 15, 18 and 24 V.

The last (XX) two numbers indicate output voltages.



The three terminal regulators have the following limitations:

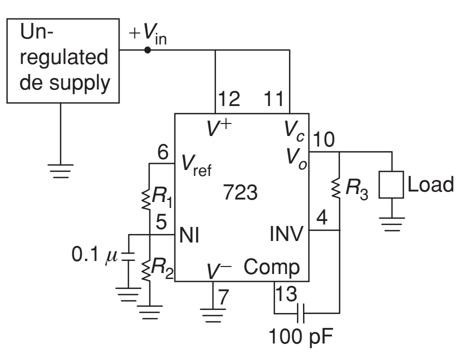
1. No short circuit protection
2. Output voltage (positive or negative) is fixed

These limitations have been overcome in 723 general purpose regulator.

Advantages: Adjustable to wide range of both + ve and –ve voltages, it can be boosted to provide 5A or more current

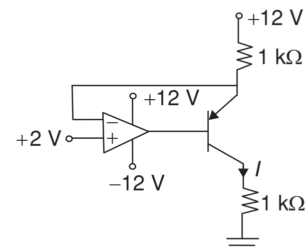
Limitations:

- No built in thermal protection
- No short circuit current limits.



Example 28: An op-amp circuit is shown in the figure, the current 'I' is

$$V_o = V_{ref} \frac{R_2}{R_1 + R_2}$$



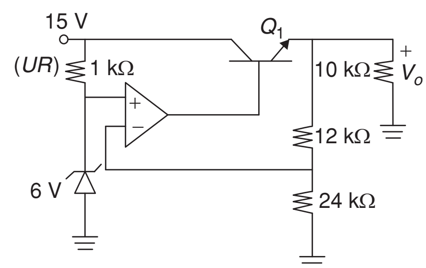
(A) 0 (B) 5 mA
(C) 10 mA (D) 12 mA

Solution: (C)

The current through emitter $I_E = \frac{(12-2)\text{ V}}{1\text{ k}\Omega} = 10\text{ mA}$

The current through collector $= I_C \approx I_E \approx 10$ mA

Example 29: A regulated power supply, shown in the figure below, has an unregulated input (UR) of 15 V, and generates a regulated output V_{out}. Use the component values shown, the power dissipation across the transistor Q_1 in the figure is



(A) 4.8 W (B) 5.0 W
(C) 5.4 W (D) 6.0 W

Solution: (C)

The zener is in break down region

$$V_+ = V_Z = +6\text{ V} = V_{in}$$

$$V_o = V_{in}\left(1 + \frac{RF}{R_1}\right)$$

$$V_{out} = V_o = 6\left(1 + \frac{12\text{ k}}{24\text{ k}}\right) = 9\text{ V}.$$

The current in 10 Ω resistor is very high when compared with current in 12 kΩ + 24 kΩ resistor, so it is negligible

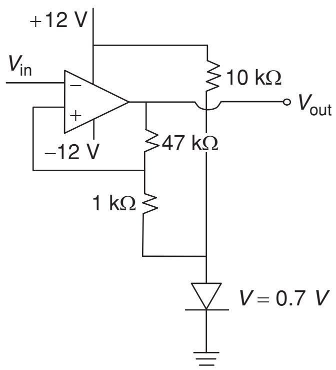
$$I_C \approx I_E \approx \frac{V_{out}}{R_L} = \frac{9}{10} = 0.9\text{A}$$

$$V_{CE} = 15 - 9 = 6\text{ V}$$

The power dissipated in transistor is P

$$= V_{CE} \times I_C = 6 \times 0.9 = 5.4\text{ W}$$

Example 30: The Schmitt trigger circuit is shown in the circuit, if $\pm V_{sat} = \pm 10$ V, the tripping point for the increasing input voltage will be?



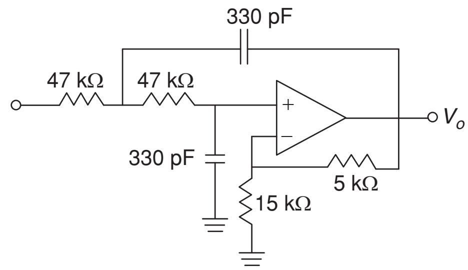
(A) 1 V (B) 0 · 893 V
(C) 0 · 477 V (D) 0 · 416 V

Solution: (B)

$$\text{Tripping point } = \frac{R_1}{R_1 + R_2}\cdot V_R + \frac{R_2}{R_1 + R_2}\cdot V_0$$

$$= \frac{1}{48}\times 10.7 + \frac{47}{48}\times 0.7 = 0.893 \text{ V}$$

Example 31: The pole frequency and Q of the filter shown in figure is



(A) 0.6 and 10.3 KHz (B) 0.5 and 10.3 KHz
(C) 0.5 and 5.15 KHz (D) 0.6 and 5.15 KHz

Solution: (A)

$$A_v = \frac{5}{15} + 1 = 1.33$$

$$Q = \frac{1}{3 - A_v} = \frac{1}{3 - 1.33} = 0.6 \text{ (Same for LPF and HPF)}$$

$$f_P = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}} = \frac{1}{2\pi RC} = 10.3 \text{ KHz}$$ for Butterworth filter.

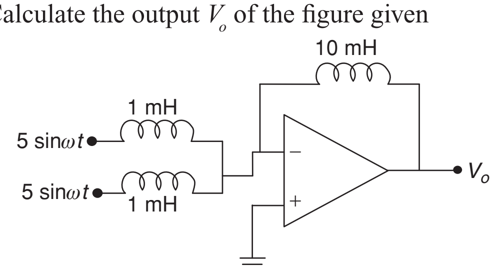
Pole frequency is same as cutoff.

Exercises

Practice Problems I

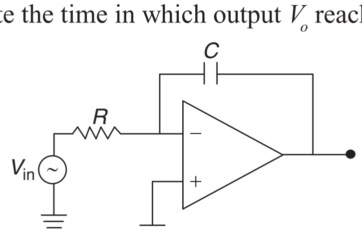
Directions for questions 1 to 41: Select the correct alternative from the given choices.

1. Calculate the output V_o of the figure given



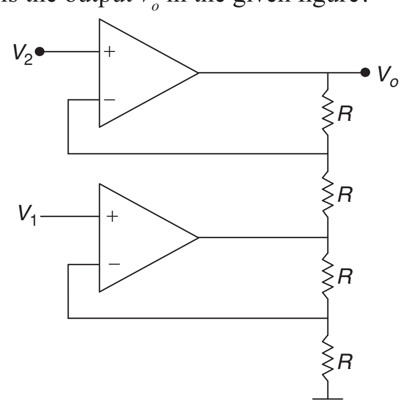
(A) 7 sinωt V (B) 3 sinω V
(C) −70 sinωt V (D) −10 sinωt V

2. An op-amp integrator with R = 10 MΩ and C = 0.1 μF is shown below. An input of 4sin100t V is applied. Calculate the time in which output V_o reach 20 mV.



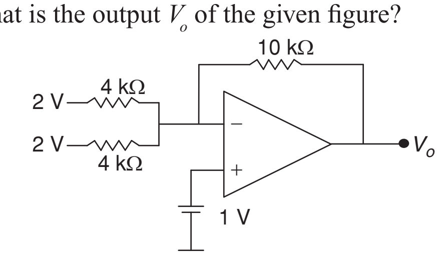
(A) 1.047 sec (B) 10.47 sec
(C) 10.47μsec (D) 10.47msec

3. What is the output V_o in the given figure?



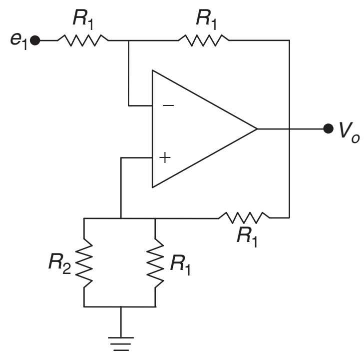
(A) $V_1 - V_2$ (B) $V_1 + V_2$
(C) $2(V_1 - V_2)$ (D) $2(V_2 - V_1)$

4. What is the output V_o of the given figure?



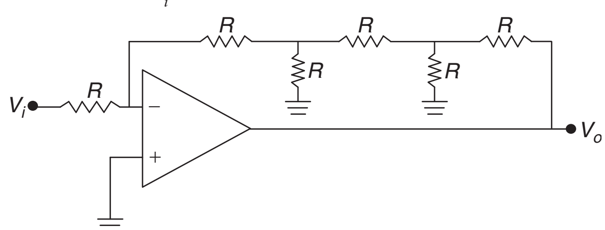
(A) 10 V (B) –6 V
(C) –4 V (D) –10 V

5. What is the current in R_2, given that $R_1 = 1$ kΩ, $R_2 = 2$ kΩ and $e_1 = 1$ volt?



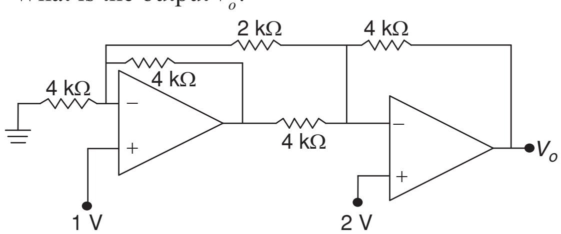
(A) –0.5 mA (B) –1 mA
(C) –2 mA (D) None

6. Calculate $\frac{V_o}{V_i}$ of the given figure.



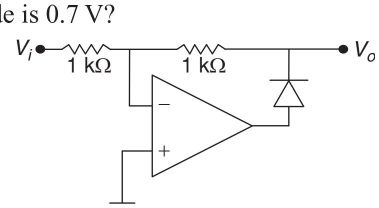
(A) 4 (B) –8
(C) –4 (D) None

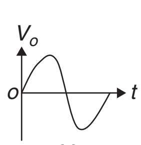
7. What is the output V_o?

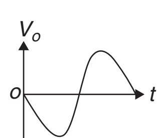


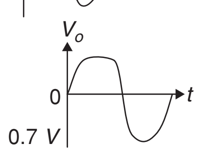
(A) 2 V (B) 4 V
(C) 6 V (D) 0 V

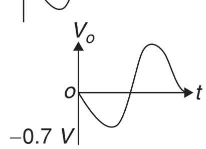
8. What is the output wave form for the input sinusoidal for the circuit given assuming the forward voltage drop of diode is 0.7 V?



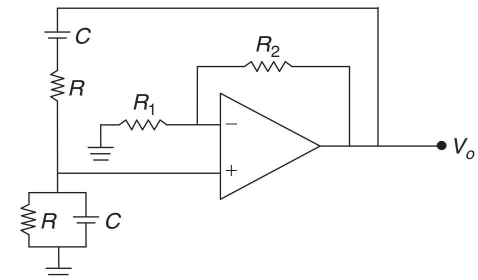
(A)


(B)


(C)


(D)


9. A Wien bridge oscillator is shown below with $R = 2$ kΩ, $C = 0.16$ µF.



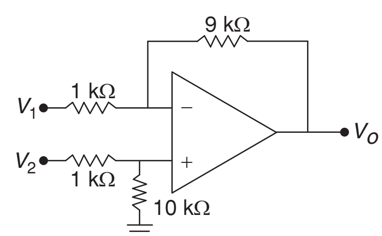
If $R_1 = 0.5$ kΩ, the value of R_2 to sustained oscillations is

(A) 0.5 kΩ (B) 1 kΩ
(C) 2 kΩ (D) 1.5 kΩ

10. The frequency of output is

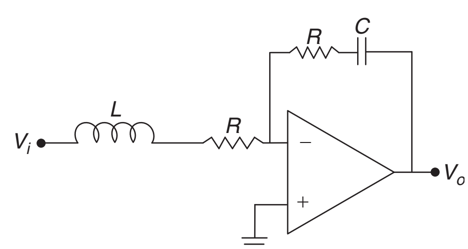
(A) 50 Hz (B) 1 KHz
(C) 5 KHz (D) 500 Hz

11. The CMRR of the given figure is



(A) 900 (B) 9
(C) 90 (D) Infinite

12. Given op-amp is ideal $R = \sqrt{\frac{L}{C}}$. What is the phase angle between V_o and V_i at $\omega = \frac{1}{\sqrt{LC}}$?

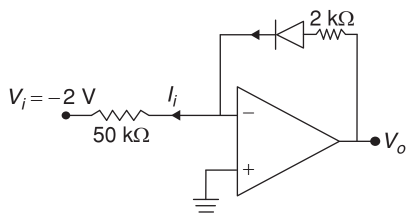


(A) 180° (B) 270°
(C) 0° (D) 90°

13. The op-amp shown is ideal. The V–I characteristic of diode is given by

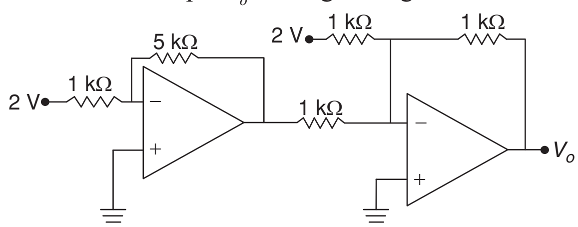
$$I = I_o\left[e^{\frac{V_d}{\eta V_T}} - 1\right] \text{ where}$$

$V_T = 26$ mV, $I_o = 10$ µA and V_d = Voltage across diode.
The output V_o for $V_i = -2$ V is ________



(A) 0.122 V (B) 0.6 V
(C) 1.2 V (D) None

14. What is the output V_o in the given figure?



(A) 8 V (B) −8 V
(C) 10 V (D) −10 V

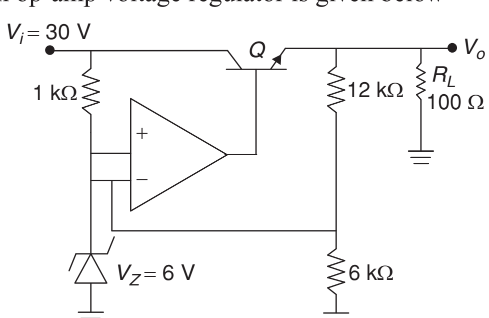
15. An op-amp has open loop gain '*A*' of 2×10^3, the input impedance Z_i = 100 kΩ and output impedance Z_o = 2 kΩ. The op-amp is used in non-inverting mode with closed loop gain 100. The effective input and output impedances are __________

(A) Z_{if} = 2.1 MΩ and Z_{of} = 42 kΩ
(B) Z_{if} = 4.8 kΩ and Z_{of} = 95 Ω
(C) Z_{if} = 2.1 MΩ and Z_{of} = 95 Ω
(D) Z_{if} = 4.8 kΩ and Z_{of} = 42 kΩ

16. A differential amplifier has a typical common mode gain 30 db and CMRR of 70 dB. What is the output voltage V_o when input voltages are 0.14 mV and 0.16 mV

(A) 2.047 V (B) 1.99 V
(C) 4.74 V (D) 4.4 V

17. An op-amp voltage regulator is given below



The regulated output V_o is

(A) 10 V (B) 20 V
(C) 9 V (D) 18 V

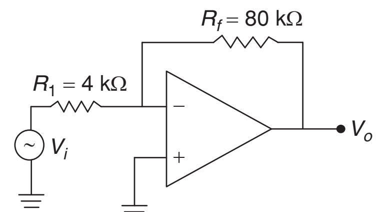
18. The power dissipation by transistor is

(A) 1.08 W (B) 2.16 W
(C) 4 W (D) 3.2 W

19. For a non-inverting amplifier R_1 = 20 kΩ, R_f = 100 kΩ, is used. A peak to peak voltage of 2 V is applied at input. Given slew rate = 0.5 V/μs, what is maximum operating frequency

(A) 6.66 kHz (B) 13.33 kHz
(C) 16 kHz (D) 8 kHz

20. An op-amp circuit given below



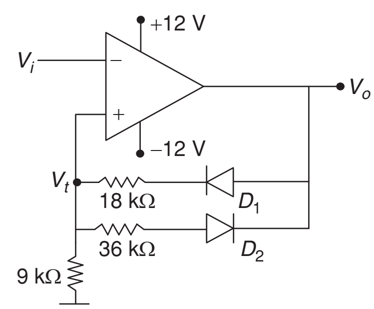
The feedback implemented is

(A) voltage series
(B) voltage shunt
(C) current series
(D) current shunt

21. Feedback ratio β is

(A) 95.2% (B) 5.2%
(C) 5% (D) 4.7%

22. Given that diodes and op-amp are ideal, calculate UTP and LTP.

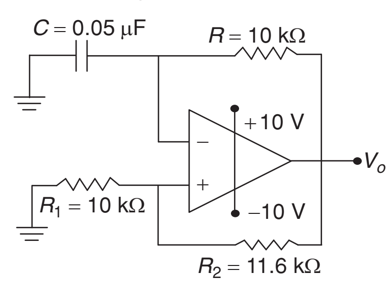


(A) V_{UTP} = 8 V V_{LTP} = −8 V
(B) V_{UTP} = 9.6 V V_{LTP} = −9.6 V
(C) V_{UTP} = 4 V V_{LTP} = −2.4 V
(D) V_{UTP} = −4 V V_{LTP} = 2.4 V

23. An op-amp has unity gain frequency of 400 MHz with band width of 60 kHz. Calculate gain in dB

(A) 56.5 dB (B) 20 dB
(C) 76.48 dB (D) None

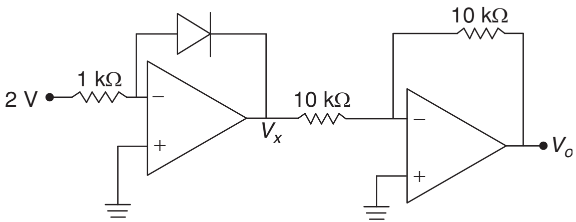
Common Data for Questions 24 and 25: A square wave generator (astable) using op-amp is shown below.



24. The frequency of the square wave output is
(A) 500 Hz (B) 2.5 kHz
(C) 1 kHz (D) None

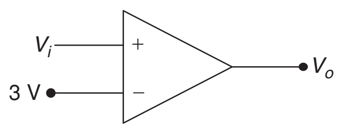
25. The feedback ratio β of the circuit is
(A) 0.463 (B) 1
(C) 0.72 (D) 0.537

26. Calculate the output V_o of the given figure. Given V_T = 25 mV



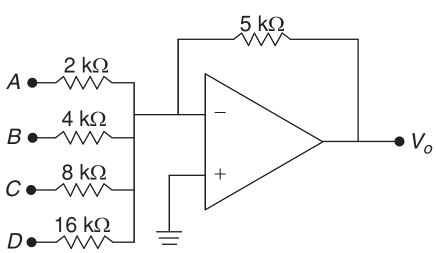
(A) –17.3 mV (B) 17.3 mV
(C) 0.69 mV (D) –0.69 mV

27. A comparator is shown below. A sinusoidal input of peak value 6 V is applied. The length (in degrees) for which the output high is



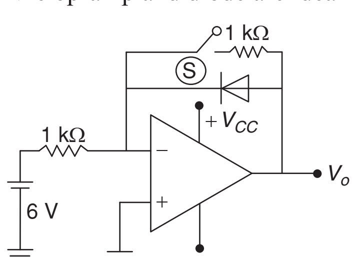
(A) 180° (B) 60°
(C) 120° (D) 150°

28. Calculate the output voltage of the figure given below if the digital input 0101 =



Digital input is 0 V (or) +5 V for 0 or 1 respectively
(A) –7.81 V (B) –4.87 V
(C) –5.87 V (D) –3.87 V

29. Consider the op-amp and diode are ideal

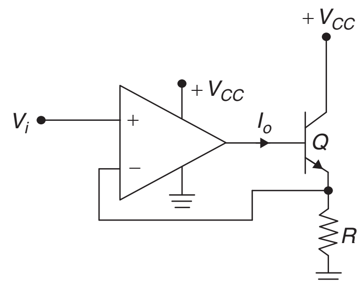


What is the output V_o when switch 'S' is open
(A) 0.7 V (B) $+V_{cc}$
(C) 0 V (D) $-V_{EE}$

30. What is the output V_o when switch S is closed
(A) –60 V (B) 0 V
(C) –6 V (D) $-V_{EE}$

31. In an inverting op-amp, the input bias current is −2μA. The input and feedback resistance are both 50 kΩ. Calculate the output voltage for input voltage of 1.5 V.
(A) –1.6 V (B) –2 V
(C) –1.5 V (D) –3 V

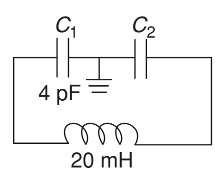
32. Assume that V_i = 3 V, R = 20 Ω, β of a transistor is 80, V_{CC} = 12 V. Calculate I_o



(A) 3.8 mA (B) 1.8 mA
(C) 0.15 A (D) 4 mA

33. The feedback network of Hartley oscillator have L_1 = 10 mH, L_2 = 5 mH and C = 100 PF. The mutual inductance between L_1 and L_2 is 2.5 mH. The frequency of oscillation is ______.
(A) 0.13 MHz (B) 11.3 kHz
(C) 0.113 MHz (D) None

Common Data for Questions 34 and 35: The feedback network used in Colpitts oscillator is given below.

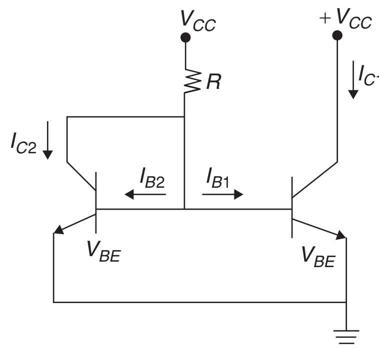


34. The value of C_2 to have frequency of oscillation 1 MHz is ______.
(A) 0.8 pF (B) 4 pF
(C) 1.8 pF (D) 2.2 pF

35. Feedback ratio β is _______.
(A) 0.45 (B) 0.2
(C) 0.9 (D) None

36. The RC network of Wien bridge oscillator has $R_1 = R_2$ = 80 kΩ, let us assume $C_1 = C_2 = C$ then what is the value of C required for the frequency of oscillation 5 kHz?
(A) 200 pF (B) 400 pF
(C) 50 pF (D) 1 pF

37. The current mirror in the figure is designed to provide I_C = 0.5 mA, V_{CC} = 10 V, β = 100, V_{BE} = 0.7 V. The value of R is



(A) 18.23 kΩ (B) 8.5 kΩ
(C) 12.9 kΩ (D) 15.3 kΩ

38. If V_{BE} changes by $\frac{-2.2\text{ mV}}{°\text{C}}$ what is the permissible temperature range if I_{C1} is to remain within 1% of its normal design value of the above problem?

(A) 21°C (B) 42°C
(C) 93°C (D) 12°C

39. Match List I and List II

LIST I	LIST II
P. Wien bridge oscillator	**1.** Low output Impedance
Q. Voltage shunt feedback Amplifier	**2.** RF frequency range
R. Crystal Oscillator	**3.** Audio Frequency range
S. Current Shunt feedback Amplifier	**4.** High Input Impedance
	5. High Output Impedance

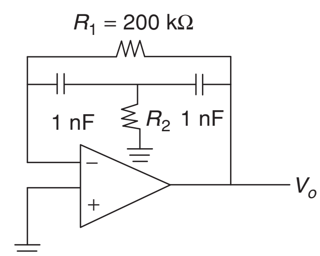
	P	Q	R	S
(A)	2	1	3	5
(B)	5	4	2	1
(C)	3	4	2	1
(D)	3	1	2	5

40. The slew rate of an op-amp is 0.5 V/micro seconds. The maximum frequency of a sinusoidal input of $2V_{(rms)}$ that can be handled without excessive distortion is

(A) 3 kHz
(B) 30 kHz
(C) 200 kHz
(D) 2 MHz

41. In the active filter circuit, if $Q = 2$, a pair of poles will be realized with ω_o, equal to

(A) 2000 rad/s
(B) 200 rad/s
(C) 20 rad/s
(D) 2 rad/s



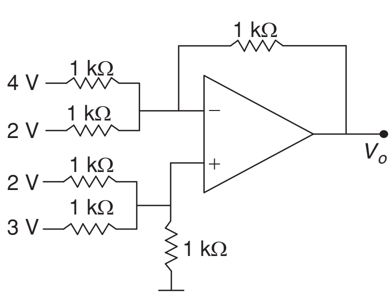
Practice Problems 2

Directions for questions 1 to 39: Select the correct alternative from the given choices.

1. An op-amp has an open loop gain 60 dB and common mode gain is 1.2. Calculate CMRR in dB

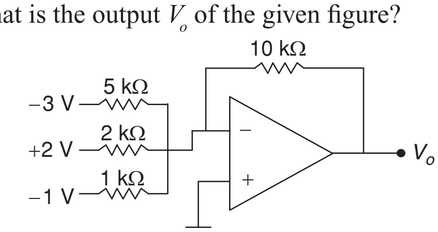
(A) 50 dB (B) 58.42 dB
(C) 72 dB (D) 58.8 dB

2. What is the output V_o of the given figure?



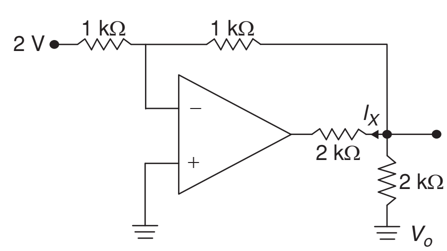
(A) –1 V (B) +1 V
(C) 0 V (D) 2 V

3. What is the output V_o of the given figure?



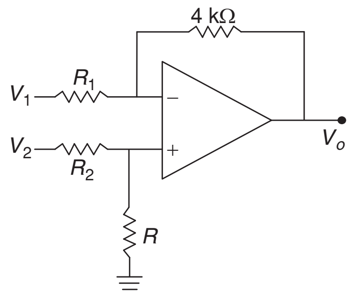
(A) 0 V (B) 6 V
(C) –6 V (D) –14 V

4. What is the current I_x of the given figure?



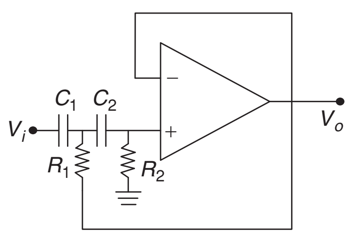
(A) 3 mA (B) 2 mA
(C) 1.5 mA (D) 0

5. What is the value of R as if the magnitude of gains in inverting and non-inverting modes is equal. ($R_1 = R_2$)



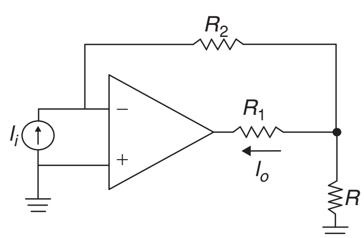
(A) 4 kΩ (B) 2 kΩ
(C) 1 kΩ (D) 8 kΩ

6. What is the cutoff frequency of the given figure.
$C_1 = c_2 = 0.08\ \mu F$
$R_1 = 7.07\ k\Omega$
$R_2 = 14.14\ k\Omega$



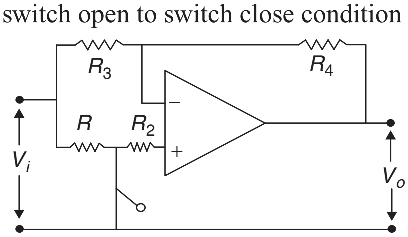
(A) 2 kHz (B) 20 kHz
(C) 0.2 kHz (D) None

7. In the circuit given below, I_o/I_i is



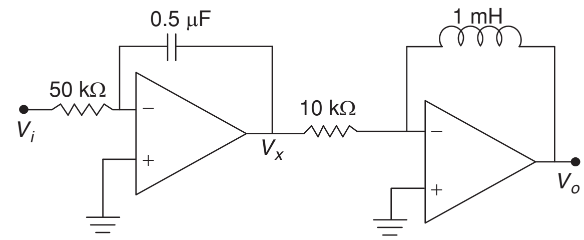
(A) $1+\frac{R_2}{R}$ (B) $1+\frac{R_1}{R}$
(C) $\frac{R_2}{R}$ (D) $\frac{R_1}{R}$

8. What is the ratio of gain of the circuit given below when switch open to switch close condition



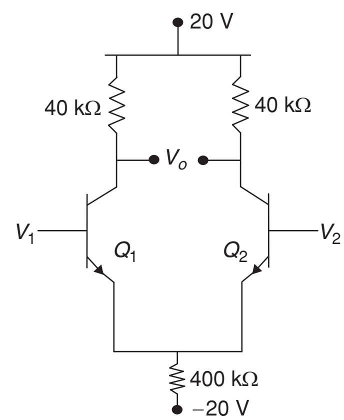
(A) $\frac{-R_3}{R_4}$ (B) $R_1+\frac{R_3}{R_4}$
(C) $\frac{-R_4}{R_3}$ (D) $R_2+\frac{R_4}{R_3}$

9. Calculate the output V_o of the figure given below.



Where $V_i = 10\cos100t$ Volt
(A) $0.04\cos100t$ mV (B) $0.2\sin100t$ V
(C) $-4\cos100t$ mV (D) $-4\sin100t$ V

Common Data for Questions 10 to 12: A differential amplifier is given below that has following specifications:
$r_\pi = 2\ M\Omega,\ \beta = 4 \times 10^3$

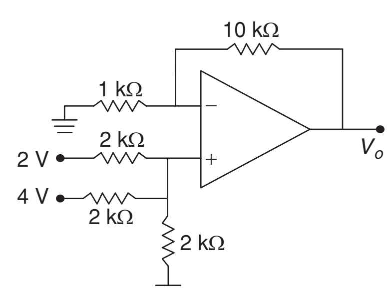


10. The differential mode gain is
(A) 100 (B) 80
(C) 90 (D) None

11. Common mode gain is
(A) 0.125 (B) 0.05
(C) 1 (D) 0

12. CMRR in dB is
(A) 64.08 dB (B) 21.8 dB
(C) 41.3 dB (D) None

13. What is the output V_o of the figure given below?

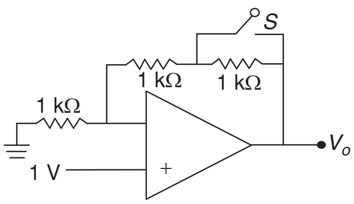


(A) 11 V (B) 33 V
(C) 22 V (D) 5.5 V

14. The CMRR of a differential amplifier is 60 dB. If the differential mode gain is 1400, what is the common mode gain A_C?

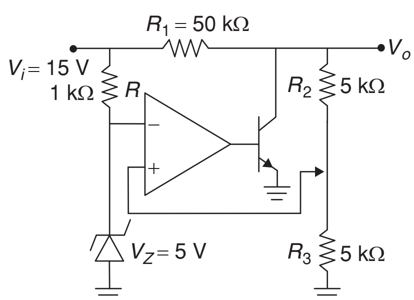
(A) 1.4 (B) 2.1
(C) 0.8 (D) None

15. An op-amp shown below give output is x when the switch S is open. What is the output when switch S is closed?



(A) x (B) $2x$
(C) $\frac{1}{2}x$ (D) $\frac{2}{3}x$

16. Calculate the power rating of R_1 if the maximum input voltage is 15 V.



(A) 4.5 W (B) 3.1 W
(C) 2.7 W (D) None

17. The change in the op-amp input offset voltage V_{io} caused by variation in supply voltage is 60 μv. Calculate the change in supply voltage. Given SVRR = 104 dB

(A) 0 V (B) 9.5 V
(C) 2 V (D) None

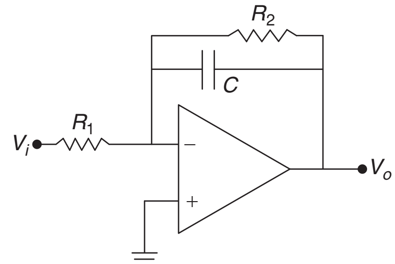
18. For non-inverting amplifier how much is the feedback resistance required to produce an output of 10 V for input of 1.5 V, given that input resistance is 2.5 kΩ?

(A) 2.26 kΩ
(B) 0.37 kΩ
(C) 14.2 kΩ
(D) 0.37 kΩ

19. An amplifier using op-amp with a slew rate 0.5 V/μsec has a gain 20 dB. If this amplifier has to faithfully amplify sinusoidal signals from DC to 30 kHz without any distortion, what is the limit of the input signal level?

(A) 266 mV (B) 2.6 V
(C) 26.6 mV (D) None

20. Recognize the type of filter shown below

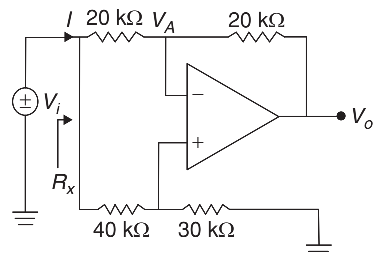


(A) Low pass filter (B) High pass filter
(C) Band pass filter (D) None

21. If R_1 = 10 kΩ, R_2 = 1 kΩ and C = 0.01μf, the cutoff frequency f_o is________

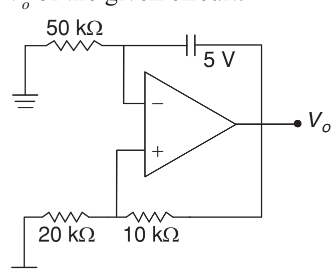
(A) 1.6 kHz (B) 1.45 kHz
(C) 160 Hz (D) None

22. Calculate R_x of the figure given below



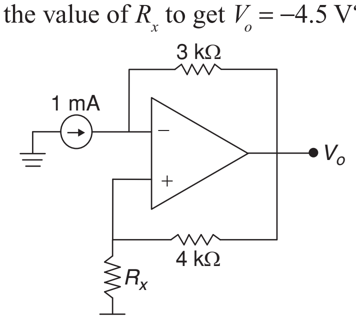
(A) 20 kΩ (B) 60 kΩ
(C) 23.3 kΩ (D) $\frac{40}{3}$ kΩ

23. Calculate V_o of the given circuit.



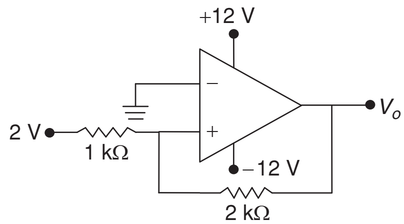
(A) 15 V (B) 0 V
(C) −5 V (D) 5 V

24. What is the value of R_x to get V_o = −4.5 V?



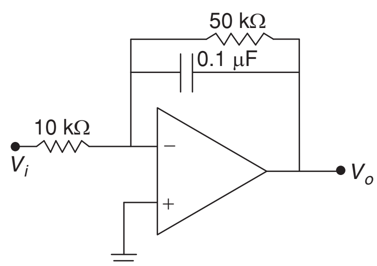
(A) 2 kΩ (B) 1 kΩ
(C) 1.5 kΩ (D) 4 kΩ

25. What is the output V_o of the given figure?



(A) +12 V (B) ±12 V
(C) −12 V (D) 6 V

26. What is the very low frequency gain of low pass filter shown in the figure given below?

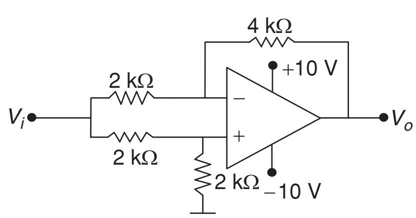


(A) ∞ (B) 6
(C) 5 (D) 0

27. An op-amp based non-inverting amplifier has a gain of 20 and bandwidth of 200 kHz. If the gain of the amplifier is reduced to unity, the band width will changes to ________

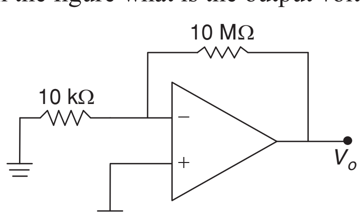
(A) 200 kHz (B) 4 MHz
(C) 1 MHz (D) 10 MHz

28. In the op-amp circuit shown, the voltage ratio V_o/V_i is



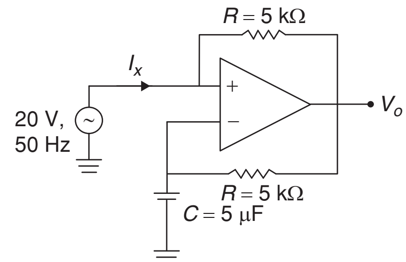
(A) –0.5 (B) –1
(C) 0.5 (D) 4

29. An op-amp has offset voltage of 1.2 mV and is ideal in all other respects. If this op-amp is used in the circuit shown in the figure what is the output voltage



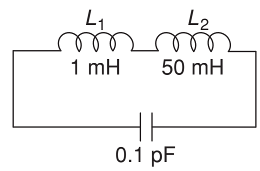
(A) 1.2 mV (B) ±1.2 V
(C) 0.6 V (D) 0 V

30. In the figure given, calculate I_x from the source



(A) 31.4 mA lead by 90° (B) 31.4 mA lag by 90°
(C) 62.8 mA lead by 90° (D) 62.8 mA lag by 90°

31. The feedback network of Hartley oscillator is shown below. The minimum gain of a transistor required for oscillation is ________.

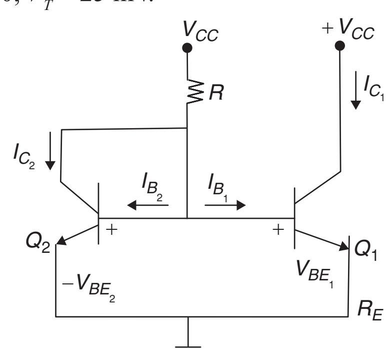


(A) 0.02 (B) 1
(C) 50 (D) None

32. The resonant circuit oscillator has a frequency of 5 MHz. If the capacitance is increased by 50%, the new frequency of oscillation is ________

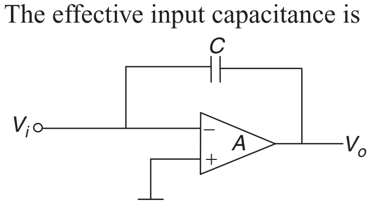
(A) 5 MHz (B) 10 MHz
(C) 2.5 MHz (D) 4.08 MHz

33. For low collector current I_{C_1} = 50 μA, this circuit is used. Determine the value of R_E, given I_{C_2} = 0.5 mA, $\beta = 100$, $V_T = 25$ mV.



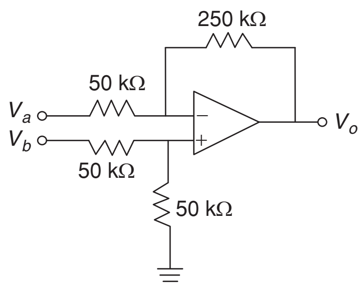
(A) 1.139 kΩ
(B) 4.34 kΩ
(C) 7.57 kΩ
(D) Its not possible to calculate

34. An amplifier of gain A is bridged by a capacitor C as shown. The effective input capacitance is



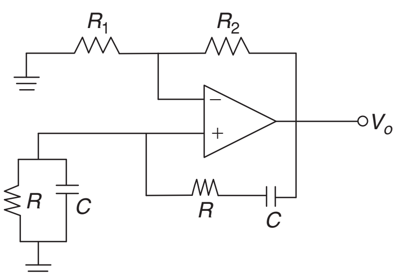
(A) $\frac{C}{A}$ (B) $C(1 - A)$
(C) $C(1 + A)$ (D) CA

35. What is the output voltage V_o of the given circuit?



(A) $-5V_a + 2.5V_b$ (B) $-5V_a + 3V_b$
(C) $-2.5V_a + 2.5V_b$ (D) $-2.5V_a + 5V_b$

36. Consider the following statements for the circuit shown in figure?

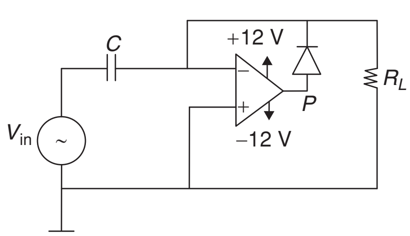


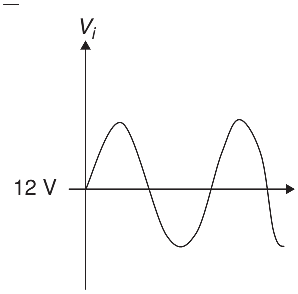
(1) For $R = 1\text{ k}\Omega, C = \left(\frac{1}{2\pi}\right)\mu\text{F}, f = 1\text{ kHz}$

(2) for $R = 3\text{ k}\Omega, C = \left(\frac{1}{18\pi}\right)\mu\text{F}, f = 3\text{ kHz}$

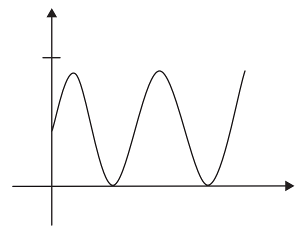
Which of the statements given are true?
(A) (1) only (B) (2) only
(C) both (D) Neither

37. For the given sinusoidal input voltage, the voltage waveform at point P of the clamper circuit shown in figure is.

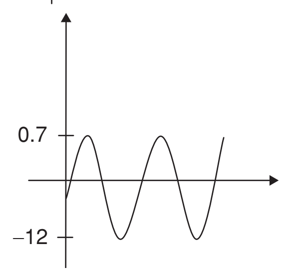




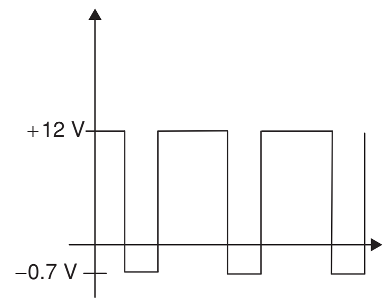
(A)



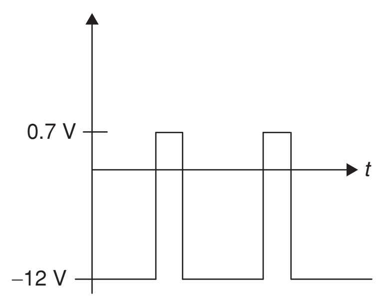
(B)



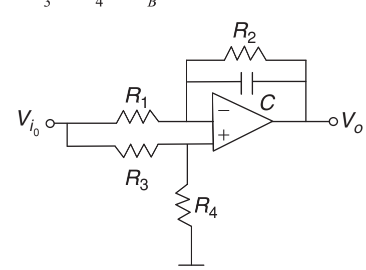
(C)



(D)

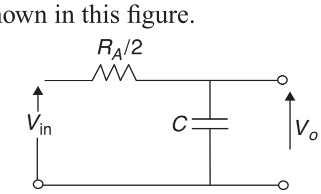


38. A general filter circuit is shown in the figure if $R_1 = R_2 = R_A$, and $R_3 = R_4 = R_B$ then the circuit acts as



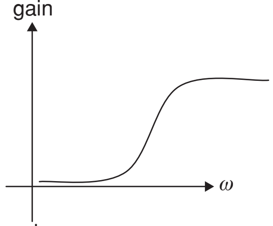
(A) All pass filter (B) Band pass filter
(C) High pass filter (D) Low pass filter

39. The output of the above filter is given to input of the circuit shown in this figure.

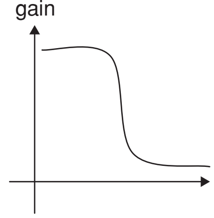


The gain V_s frequency characteristic of the output V_o will be

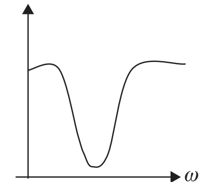
(A)



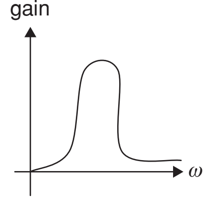
(B)



(C)

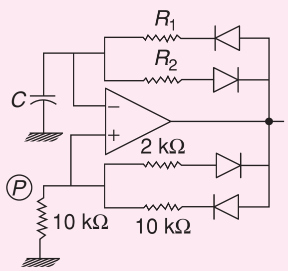


(D)

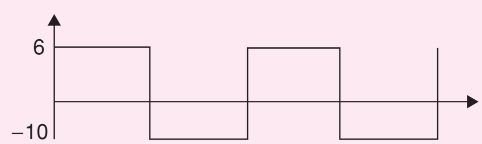


Previous Years' Questions

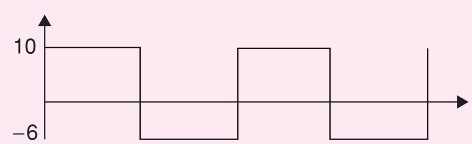
1. A relaxation oscillator is made using op-amp as shown in figure. The supply voltages of the op-amp are ±12 V. The voltage waveform at point P will be **[2006]**



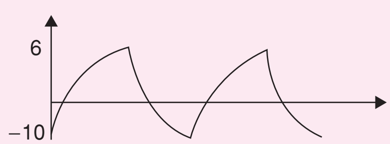
(A)



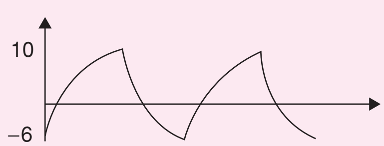
(B)



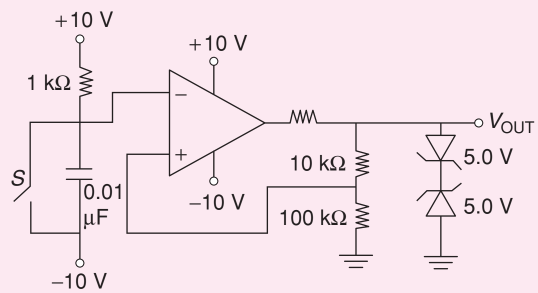
(C)



(D)



2. The switch S in the circuit of the figure is initially closed. It is opened at time $t = 0$. **[2007]**



You may neglect the Zener diode forward voltage drops. What is the behaviour of V_{OUT} for $t > 0$?

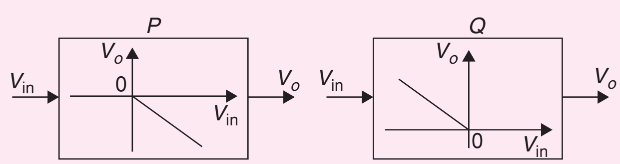
(A) It makes a transition from –5V to +5V at $t = 12.98$ µs

(B) It makes a transition from –5V to +5V at $t = 2.57$ µs

(C) It makes a transition from –5V to +5V at $t = 12.98$ µs

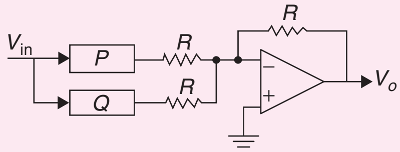
(D) It makes a transition from + 5V to –5V at $t = 2.57$ µs

3. The block diagrams of two types of half wave rectifiers are shown in the figure. The transfer characteristics of the rectifiers are also shown within the block.

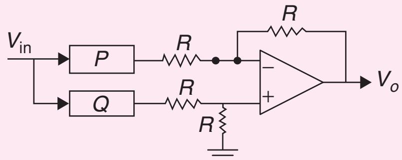


It is desired to make full-wave rectifier using above two half-wave rectifiers. The resultant circuit will be **[2008]**

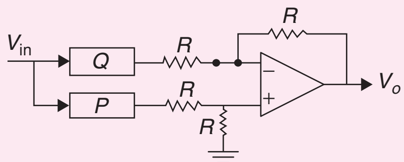
(A)



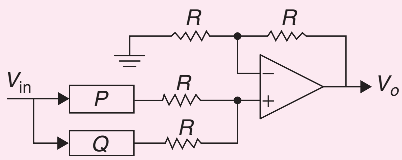
(B)



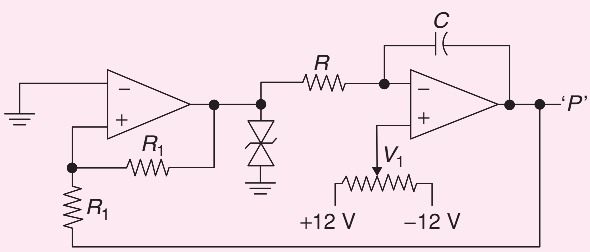
(C)



(D)

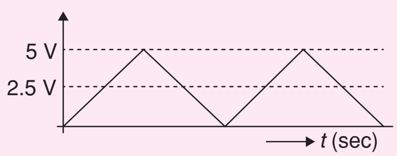


4. A waveform generator circuit using op-amps is shown in the figure. It produces a triangular wave at point 'P' with a peak to peak voltage of 5 V for $V_i = 0$ V. **[2008]**

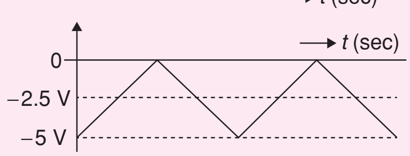


If the voltage v is made +2.5 V, the voltage waveform at point 'P' will become

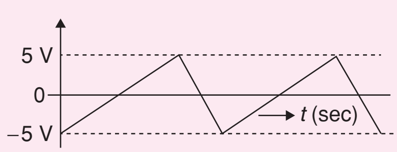
(A)



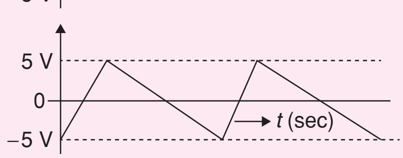
(B)



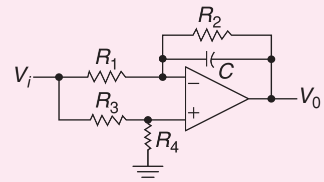
(C)



(D)



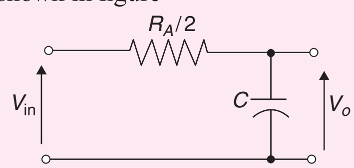
Common Data for Questions 5 and 6: A general filter circuit is shown in the figure



5. If $R_1 = R_2 = R_A$ and $R_3 = R_4 = R_s$, the circuit acts as a **[2008]**

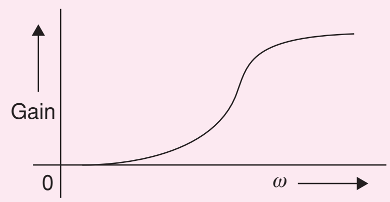
(A) all pass filter (B) band pass filter
(C) high pass filter (D) low pass filter

6. The output of the filter in question 12 is given to the circuit shown in figure **[2008]**

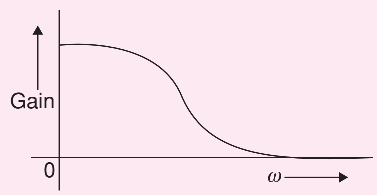


The given vs. frequency characteristic of the output (V_0) will be

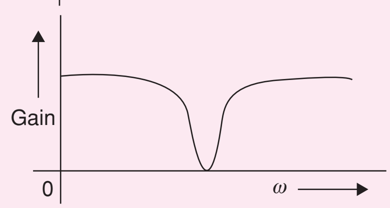
(A)



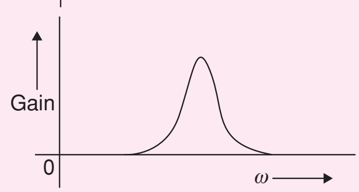
(B)



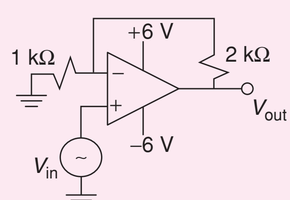
(C)



(D)

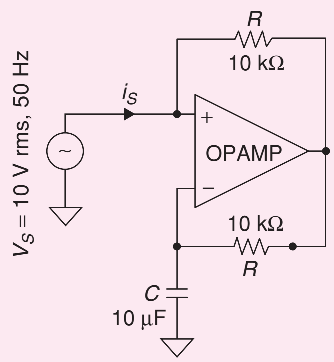


7. The nature of feedback in the op-amp circuit shown is **[2009]**



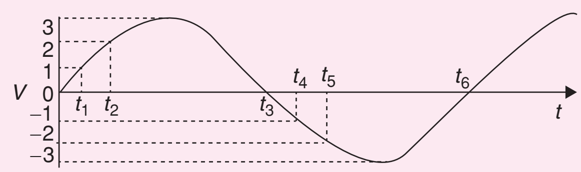
(A) Current–Current feedback
(B) Voltage–Voltage feedback
(C) Current–Voltage feedback
(D) Voltage–Current feedback

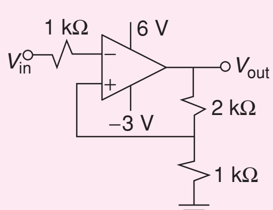
8. The following circuit has R = 10 kΩ, C = 10 μF. The input voltage is a sinusoid at 50 Hz with an rms value of 10 V. Under ideal conditions, the current i_s from the source is **[2009]**



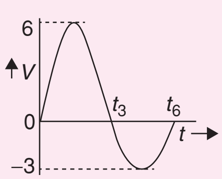
(A) 10π mA leading by 90°
(B) 20π mA leading by 90°
(C) 10 mA leading by 90°
(D) 10π mA lagging by 90°

9. An ideal op-amp circuit and its input waveform are shown in the figures. The output waveform of this circuit will be **[2009]**

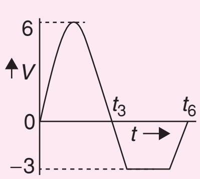




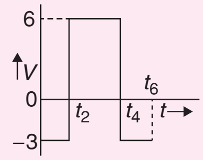
(A)



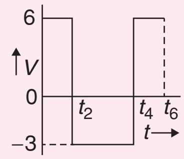
(B)



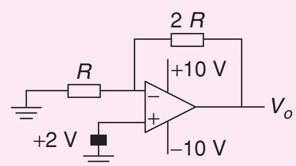
(C)



(D)

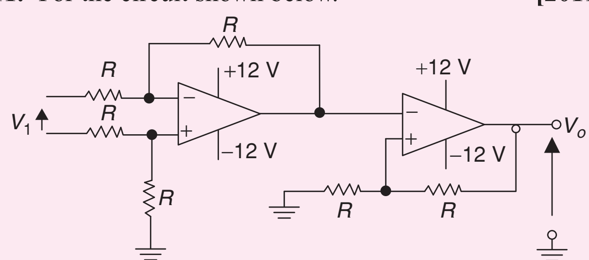


10. Given that the op-amp is ideal, the output voltage V_0 is **[2010]**



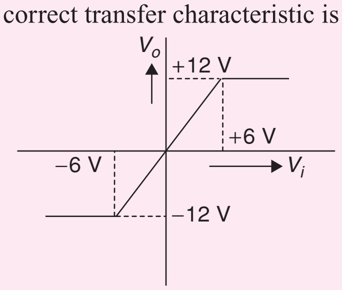
(A) 4 V
(B) 6 V
(C) 7.5 V
(D) 12.12 V

11. For the circuit shown below. **[2011]**

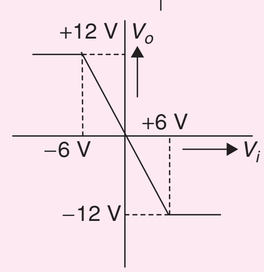


the correct transfer characteristic is

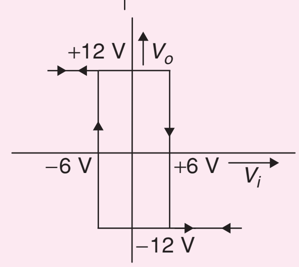
(A)



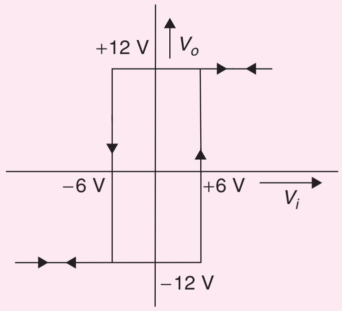
(B)



(C)



(D)



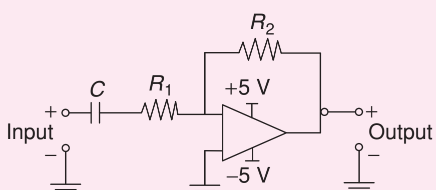
12. A dual trace oscilloscope is set to operate in the alternate mode. The control input of the multiplexer used in the y-circuit is fed with a signal having a frequency equal to: **[2011]**

(A) the highest frequency that the multiplexer can operate properly.
(B) twice the frequency of the time base (sweep) oscillator.
(C) the frequency of the time base (sweep) oscillator.
(D) half the frequency of the time base (sweep) oscillator.

13. A low-pass filter with a cutoff frequency of 30 Hz is cascaded with a high-pass filter with a cutoff frequency of 20 Hz. The resultant system of filters will function as. **[2011]**

(A) an all-pass filter
(B) an all-stop filter
(C) a band-stop (band-reject) filter
(D) a band-pass filter

14. The circuit shown is a **[2012]**



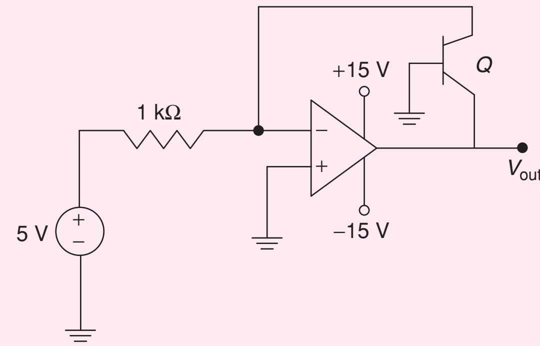
(A) low pass filter with $f_{3\text{dB}} = \dfrac{1}{(R_1 + R_2)C}$ rad/s

(B) high pass filter with $f_{3\text{dB}} = \dfrac{1}{R_1 C}$ rad/s

(C) low pass filter with $f_{3\text{dB}} = \dfrac{1}{R_1 C}$ rad/s

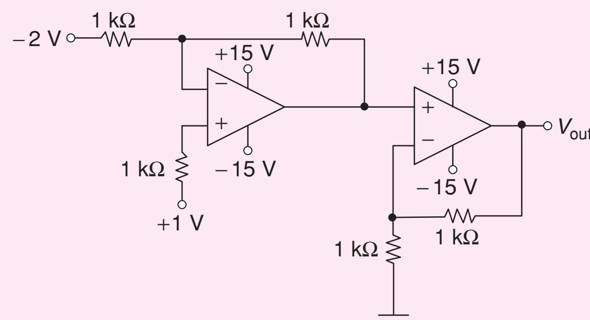
(D) high pass filter with $f_{3\text{dB}} = \dfrac{1}{(R_1 + R_2)C}$ rad/s

15. In the circuit shown below, what is the output voltage (V_{out}) in V if a silicon transistor Q and an ideal op-amp are used? **[2013]**



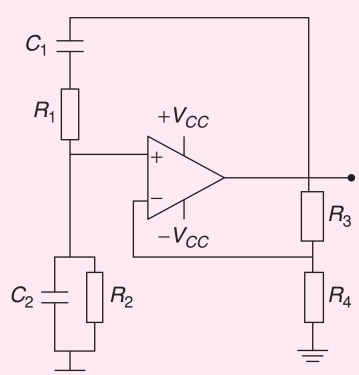
(A) −15
(B) −0.7
(C) +0.7
(D) +15

16. In the circuit shown below the op-amps are ideal. Then V_{out} in V is **[2013]**



(A) 4
(B) 6
(C) 8
(D) 10

17. In the Wien bridge oscillator circuit shown in figure, the bridge is balanced when **[2013]**



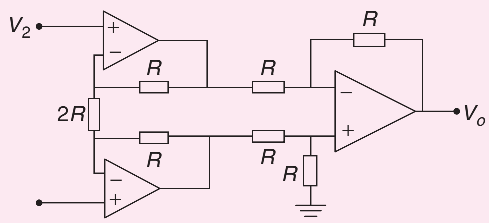
(A) $\dfrac{R_3}{R_4} = \dfrac{R_1}{R_2}, \omega = \dfrac{1}{\sqrt{R_1C_1R_2C_2}}$

(B) $\dfrac{R_2}{R_1} = \dfrac{C_2}{C_1}, \omega = \dfrac{1}{R_1C_1R_2C_2}$

(C) $\dfrac{R_3}{R_4} = \dfrac{R_1}{R_2} + \dfrac{C_2}{C_1}, \omega = \dfrac{1}{\sqrt{R_1C_1R_2C_2}}$

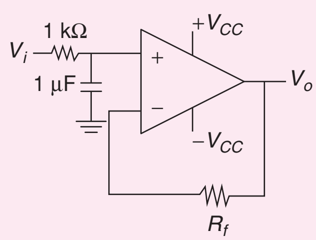
(D) $\dfrac{R_3}{R_4} + \dfrac{R_1}{R_2} = \dfrac{C_2}{C_1}, \omega = \dfrac{1}{R_1C_1R_2C_2}$

18. Given that the op-amps in the figure are ideal, the output voltage V_o is **[2014]**

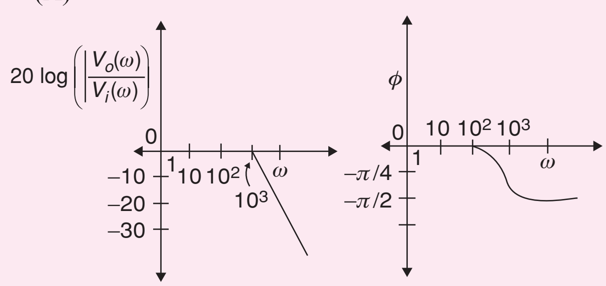


(A) $(V_1 - V_2)$ (B) $2(V_1 - V_2)$
(C) $(V_1 - V_2)/2$ (D) $(V_1 + V_2)$

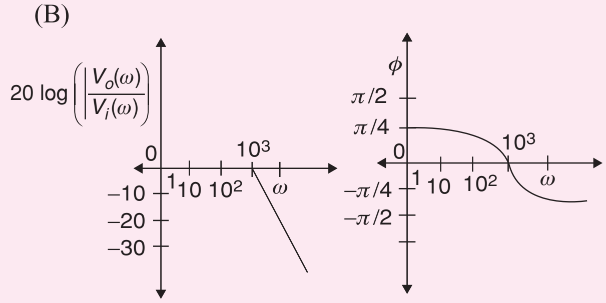
19. In the figure shown, assume the op-amp to be ideal. Which of the alternatives gives the correct Bode plots for the transfer function $\dfrac{V_o(\omega)}{V_i(\omega)}$? **[2014]**



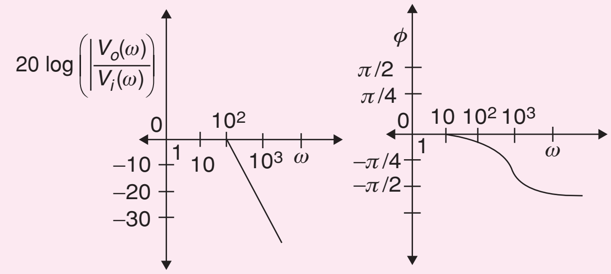
(A)



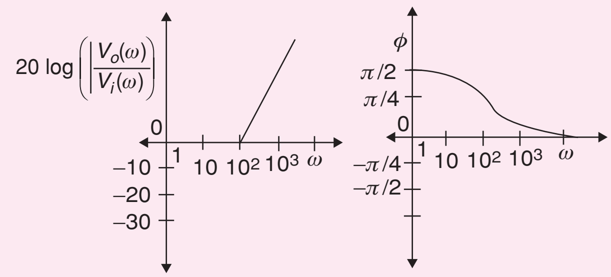
(B)



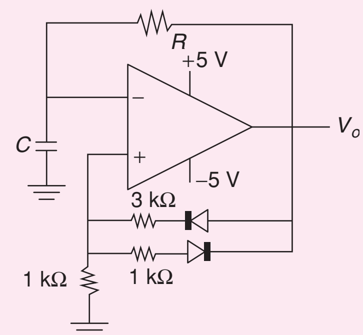
(C)



(D)

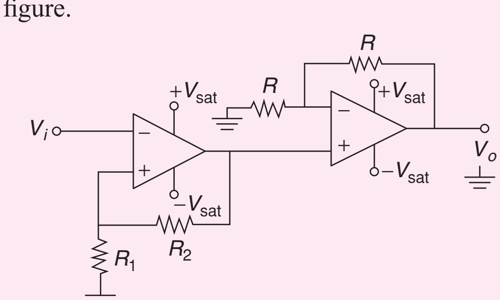


20. An oscillator circuit using ideal op-amp and diodes is shown in the figure. **[2014]**



The time duration for +ve part of the cycle is Δt_1 and for –ve part is Δt_2. The value of $e^{\frac{\Delta t_1 - \Delta t_2}{RC}}$ will be ______________.

21. An operational-amplifier circuit is shown in the figure. **[2014]**

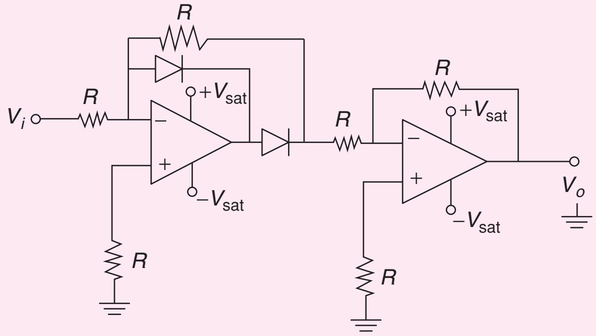


The output of the circuit for a given input v_1 is

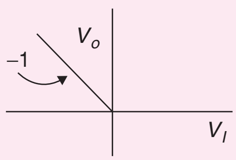
(A) $-\left(\dfrac{R_2}{R_1}\right)v_i$ (B) $-\left(1+\dfrac{R_2}{R_1}\right)v_i$

(C) $\left(1+\dfrac{R_2}{R_1}\right)v_i$ (D) $+V_{sat}$ or $-V_{sat}$

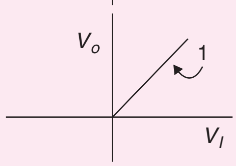
22. The transfer characteristic of the op-amp circuit shown in figure is **[2014]**



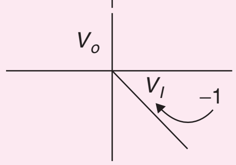
(A)



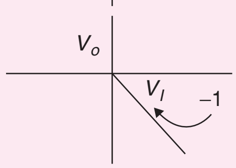
(B)



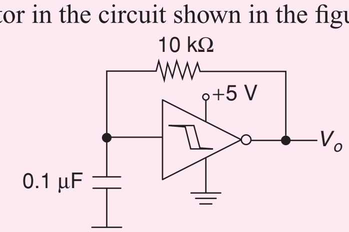
(C)



(D)

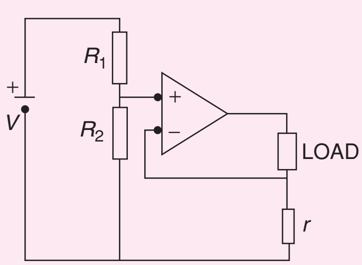


23. A hysteresis type TTL inverter is used to realize an oscillator in the circuit shown in the figure. **[2014]**



If the lower and upper trigger level voltages are 0.9 V and 1.7 V, the period (in ms), for which output is low, is ______.

24. The circuit shown in the figure is **[2007]**



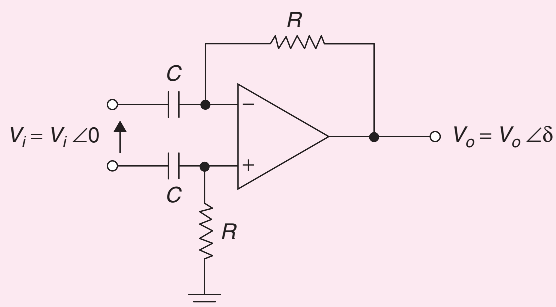
(A) a voltage source with voltage $\dfrac{rV}{R_1 \| R_2}$

(B) a voltage source with voltage $\dfrac{r \| R_2}{R_1} V$

(C) a current source with current $\dfrac{r \| R_2}{R_1 + R_2} \cdot \dfrac{V}{r}$

(D) a current source with current $\dfrac{R_2}{R_1 + R_2} \cdot \dfrac{V}{r}$

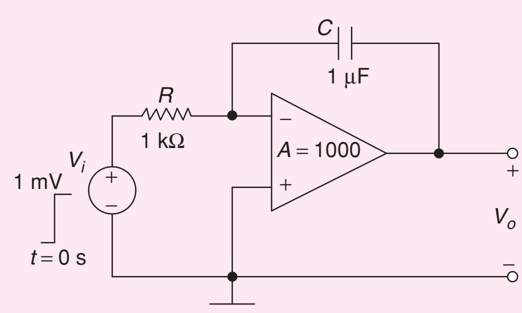
25. Consider the circuit shown in the figure. In this circuit $R = 1\ k\ \Omega$, and $C = 1\ \mu F$. The input voltage is sinusoidal with a frequency of 50 Hz, represented as a phasor with magnitude V_i and phase angle 0 radian as shown in the figure. The output voltage is represented as a phasor with magnitude V_o and phase angle δ radian. What is the value of the output phase angle δ(in radian) relative to the phase angle of the input voltage? **[2015]**



(A) 0 (B) π

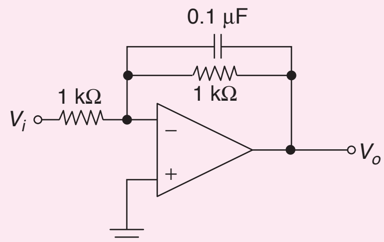
(C) $\dfrac{\pi}{2}$ (D) $-\dfrac{\pi}{2}$

26. The op-amp shown in the figure has finite gain $A = 1000$ and an infinite input resistance. A step-voltage $V_i = 1$ mV is applied at the input at time $t = 0$ as shown. Assuming that the operational amplifier is not saturated, the time constant (in millisecond) of the output voltage V_o is **[2015]**

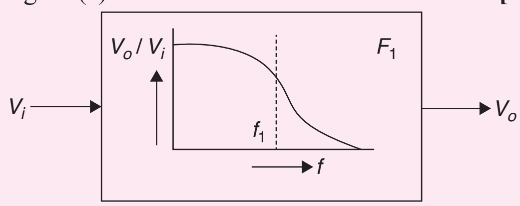


(A) 1001 (B) 101
(C) 11 (D) 1

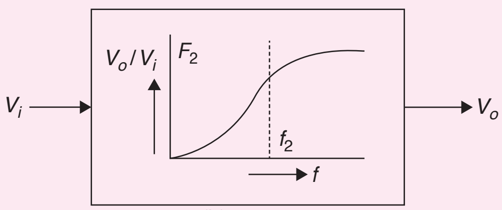
27. The operational amplifier shown in the figure is ideal. The input voltage (in Volt) is $V_i = 2\sin(2\pi \times 2000t)$. The amplitude of the output voltage V_o (in Volt) is ________. **[2015]**



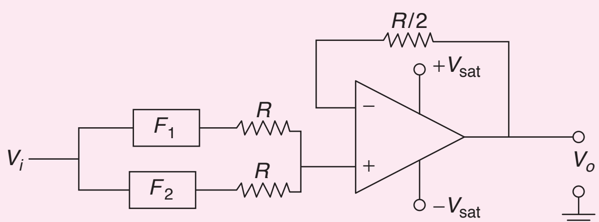
28. The filters $F1$ and $F2$ having characteristics as shown in Figures (a) and (b) are connected as shown in Figure (c). **[2015]**



(a)



(b)

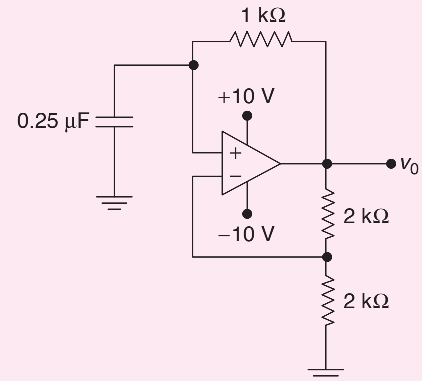


(c)

The cut-off frequencies of $F1$ and $F2$ are f_1 and f_2 respectively. If $f_1 < f_2$, the resultant circuit exhibits the characteristics of a

(A) Band-pass filter (B) Band-stop filter
(C) All pass filter (D) High-Q filter

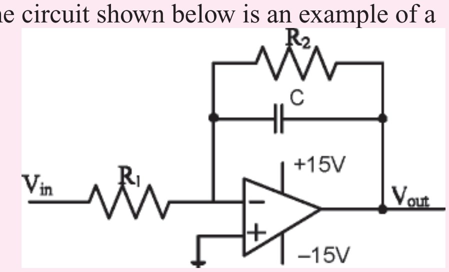
29.



The saturation voltage of the ideal op-amp shown below is ±10 V. The output voltage v_0 of the following circuit in the steady-state is **[2015]**

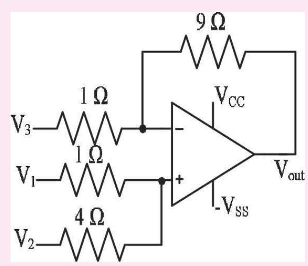
(A) square wave of period 0.55 ms.
(B) triangular wave of period 0.55 ms.
(C) square wave of period 0.25 ms.
(D) triangular wave of period 0.25 ms.

30. The circuit shown below is an example of a **[2016]**



(A) Low pass filter (B) Band pass filter
(C) high pass filter (D) Notch filter

31. For the circuit shown below, taking the opamp as ideal, the output voltage V_{out} in terms of the input voltages V_1, V_2, and V_3 is ______. **[2016]**



(A) $1.8V_1 + 7.2V_2 - V_3$ (B) $2V_1 + 8V_2 - 9V_3$
(C) $7.2V_1 + 1.8V_2 - V_3$ (D) $8V_1 + 2V_2 - 9V_3$

Answer Keys

Exercises

Practice Problems 1

1. C	**2.** D	**3.** D	**4.** C	**5.** B	**6.** B	**7.** C	**8.** D	**9.** B	**10.** D
11. C	**12.** D	**13.** A	**14.** A	**15.** C	**16.** A	**17.** D	**18.** B	**19.** B	**20.** B
21. D	**22.** C	**23.** C	**24.** C	**25.** A	**26.** B	**27.** C	**28.** A	**29.** D	**30.** C
31. A	**32.** B	**33.** C	**34.** C	**35.** A	**36.** C	**37.** A	**38.** B	**39.** D	**40.** B
41. A									

Practice Problems 2

1. B	**2.** A	**3.** B	**4.** A	**5.** A	**6.** C	**7.** A	**8.** A	**9.** A	**10.** B
11. B	**12.** A	**13.** B	**14.** A	**15.** D	**16.** A	**17.** B	**18.** C	**19.** A	**20.** A
21. A	**22.** C	**23.** A	**24.** A	**25.** A	**26.** C	**27.** B	**28.** A	**29.** B	**30.** B
31. C	**32.** D	**33.** A	**34.** B	**35.** B	**36.** C	**37.** D	**38.** C	**39.** D	

Previous Years' Questions

1. A	**2.** D	**3.** B	**4.** A	**5.** C	**6.** D	**7.** B	**8.** D	**9.** D	**10.** B
11. D	**12.** D	**13.** D	**14.** B	**15.** B	**16.** C	**17.** C	**18.** B	**19.** A	
20. 0.7977		**21.** D	**22.** C	**23.** 0.635	**24.** D	**25.** D	**26.** A	**27.** 1.1 to 1.4	
28. B	**29.** A	**30.** A	**31.** D						