Long Answer Questions

Q. 1. (a) State briefly the processes involved in the formation of p-n junction explaining clearly how the depletion region is formed.

(b) Using the necessary circuit diagrams, show how the V–I characteristics of a p-n junction are obtained in

(i) Forward biasing (ii) Reverse biasing How are these characteristics made use of in rectification? [CBSE Delhi 2014]

OR

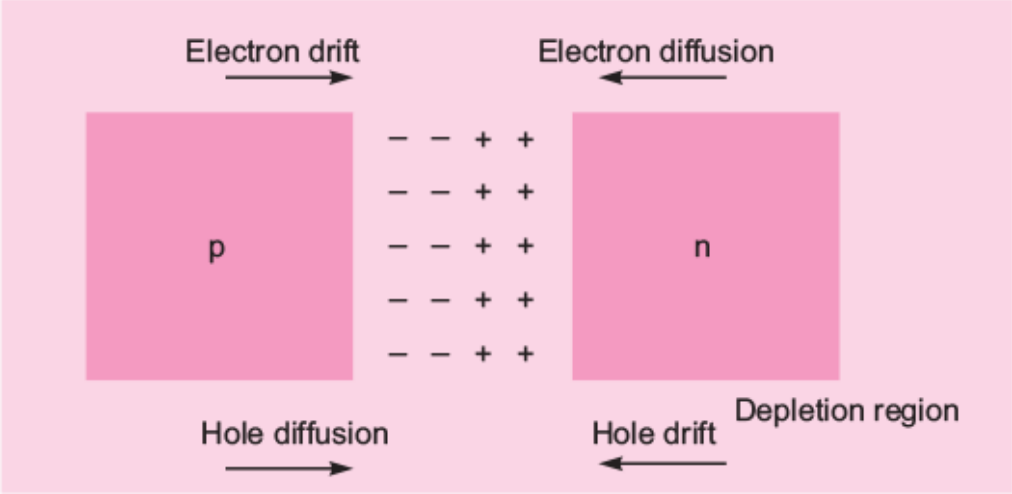
Draw the circuit arrangement for studying the V–I characteristics of a p-n junction diode (i) in forward bias and (ii) in reverse bias. Draw the typical V–I characteristics of a silicon diode.

Describe briefly the following terms:

(i) "Minority carrier injection" in forward bias

(ii) "Breakdown voltage" in reverse bias. [CBSE Chennai 2015]

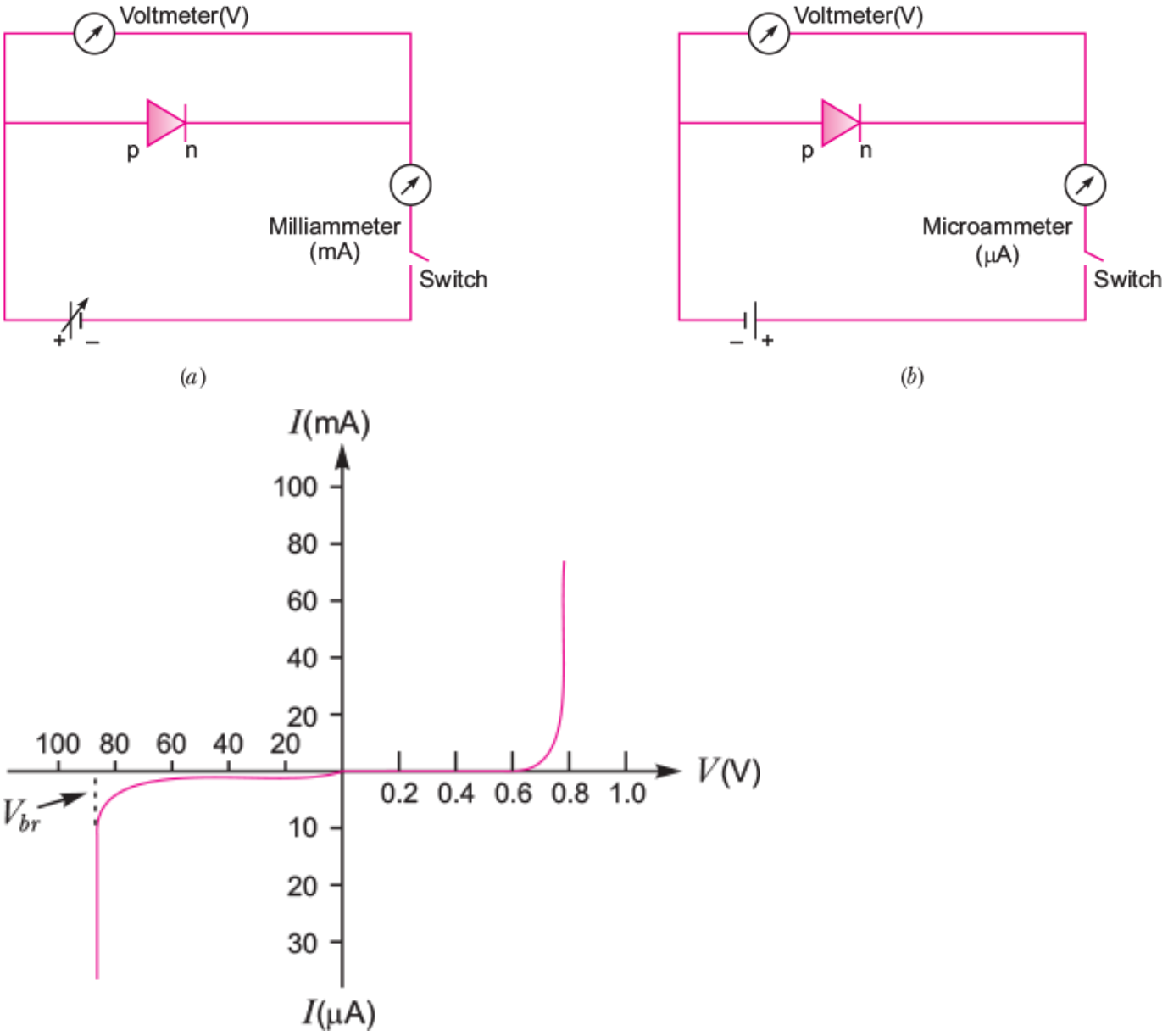
Ans. (a)



Two processes occur during the formation of a p-n junction are diffusion and drift. Due to the concentration gradient across p and n-sides of the junction, holes diffuse from p-side to n-side (p → n) and electrons diffuse from n-side to p-side (n → p). This movement of charge carriers leaves behind ionised acceptors (negative charge φ-immobile) on the p-side and donors (positive charge immobile) on the n-side of the junction. This space charge region on either side of the junction together is known as depletion region.

(b) The circuit arrangement for studying the V–I characteristics of a diode are shown in Fig. (a) and (b). For different values of voltages the value of current is noted. A graph between V and I is obtained as in Figure (c).

From the V–I characteristic of a junction diode it is clear that it allows current to pass only when it is forward biased. So if an alternating voltage is applied across a diode the current flows only in that part of the cycle when the diode is forward biased. This property is used to rectify alternating voltages.

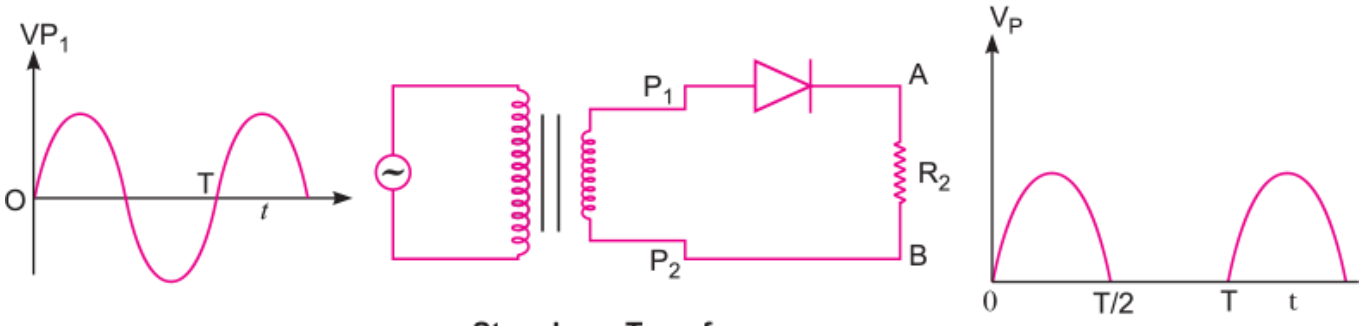


(i) Minority Carrier Injection: Due to the applied voltage, electrons from n-side cross the depletion region and reach p-side (where they are minority carriers). Similarly, holes from p-side cross this junction and reach the n-side (where they are minority carriers). This process under forward bias is known as minority carrier injection.

(ii) Breakdown Voltage: It is a critical reverse bias voltage at which current is independent of applied voltage.

Q. 2. Explain, with the help of a circuit diagram, the working of a p-n junction diode as a half-wave rectifier. [CBSE (AI) 2014]

Ans.



Step down Transformer

Working

(i) During positive half cycle of input alternating voltage, the diode is forward biased and a current flows through the load resistor R_L and we get an output voltage.

(ii) During other negative half cycle of the input alternating voltage, the diode is reverse biased and it does not conduct (under break down region).

Hence, AC voltage can be rectified in the pulsating and unidirectional voltage.

Q. 3. State the principle of working of p-n diode as a rectifier. Explain with the help of a circuit diagram, the use of p-n diode as a full wave rectifier. Draw a sketch of the input and output waveforms. [CBSE Delhi 2012]

OR

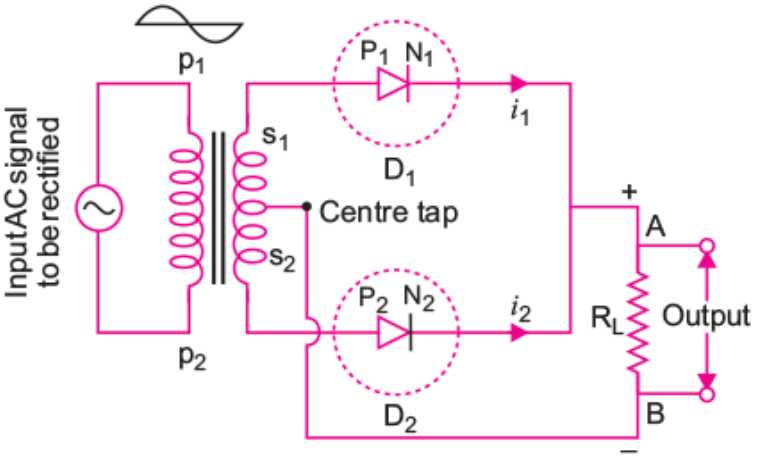
Draw a circuit diagram of a full wave rectifier. Explain the working principle. Draw the input/output waveforms indicating clearly the functions of the two diodes used.
[CBSE (AI) 2011]

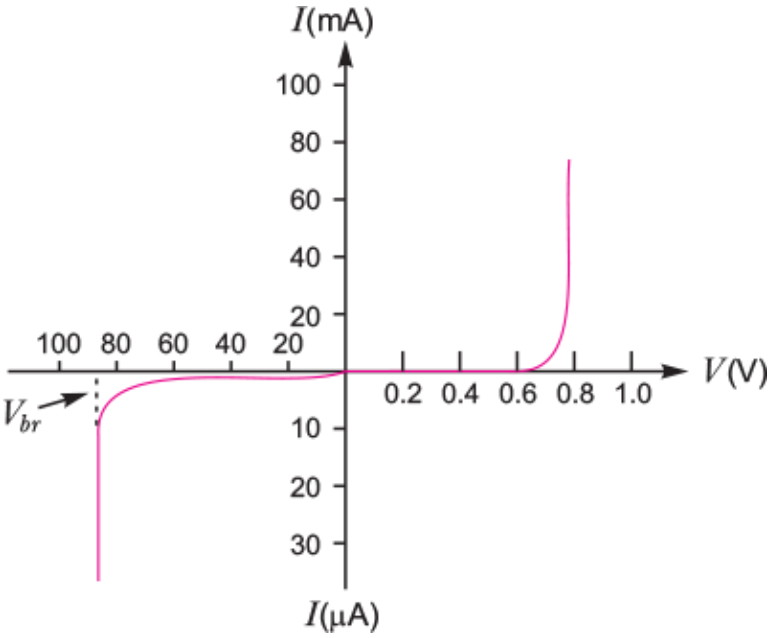
OR

With the help of a circuit diagram, explain the working of a junction diode as a full wave rectifier. Draw its input and output waveforms. Which characteristic property makes the junction diode suitable for rectification?
[CBSE Ajmer 2015, North 2016]

Ans. Rectification: Rectification means conversion of ac into dc. A *p-n* diode acts as a rectifier because an ac changes polarity periodically and a *p-n* diode allows the current to pass only when it is forward biased. This makes the diode suitable for rectification.

Working: The ac input voltage across secondary s_1 and s_2 changes polarity after each half cycle. Suppose during the first half cycle of input ac signal, the terminal s_1 is positive relative to centre tap O and s_2 is negative relative to O. Then diode D_1 is forward biased and diode D_2 is reverse biased. Therefore, diode D_1conducts while diode D_2 does not. The direction of current (i_1) due to diode D_1 in load resistance R_L is directed from A to B In next half cycle, the terminal s_1 is negative and s_2 is positive relative to centre tap O. The diode D_1 is reverse biased and diode D_2 is forward biased. Therefore, diode D_2 conducts while D_1 does not. The direction of current (i_2) due to diode D_2 in load resistance R_L is still from A to B. Thus, the current in load resistance R_L is in the same direction for both half cycles of input ac voltage. Thus *for input ac signal the output current is a continuous series of unidirectional pulses.*





In a full wave rectifier, if input frequency is f hertz, then output frequency will be 2f hertz because for each cycle of input, two positive half cycles of output are obtained.

Q. 4. Answer the following questions.

(i) Explain, how the heavy doping of both p-and n-sides of a p-n junction diode results in the electric field of the junction being extremely high even with a reverse bias voltage of a few volts. [CBSE (F) 2013]

Ans. (i) If p-type and n-type semiconductor are heavily doped. Then due to diffusion of electrons from n-region to p-region, and of holes from p-region to n-region, a depletion region formed of size of order less than 1 μm. The electric field directing from n-region to p-region produces a reverse bias voltage of about 5V and electric field becomes very large.

$$E = \frac{\Delta V}{\Delta x} = \frac{5V}{1\mu m} \approx 5 \times 10^6 V/m$$

Q. 5. Why is a Zener diode considered as a special purpose semiconductor diode?

Draw the I–V characteristic of a zener diode and explain briefly how reverse current suddenly increases at the breakdown voltage.

Describe briefly with the help of a circuit diagram how a Zener diode works to obtain a constant dc voltage from the unregulated dc output of a rectifier. [CBSE (F) 2012]

OR

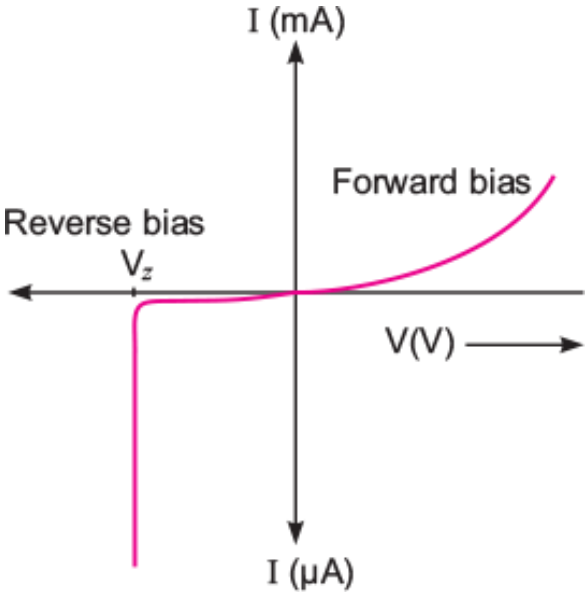
How is Zener diode fabricated? What causes the setting up of high electric field even for small reverse bias voltage across the diode?

Describe with the help of a circuit diagram, the working of Zener diode as a voltage regulator. [CBSE Panchkula 2015]

Ans. A Zener diode is considered as a special purpose semiconductor diode because it is designed to operate under reverse bias in the breakdown region.

Zener diode is fabricated by heavy doping of its p and n sections. Since doping is high, depletion layer becomes very thin.

Hence, electric field $\left(= \frac{v}{l}\right)$ becomes high even for a small reverse bias.

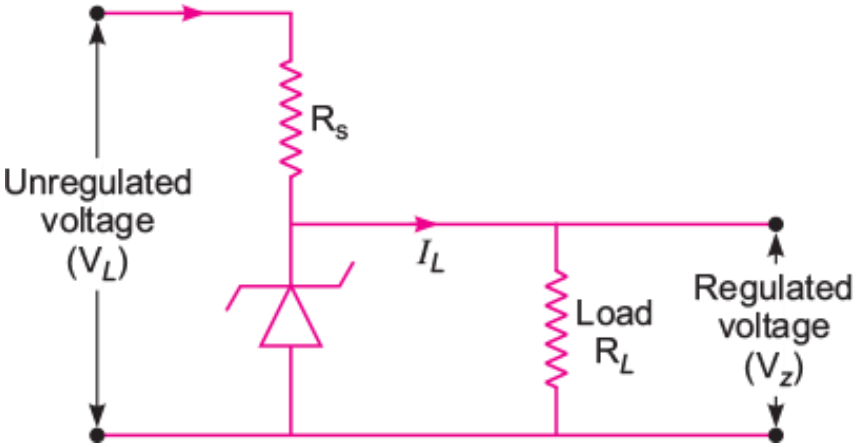


We know that reverse current is due to the flow of electrons (minority carriers) from $p \rightarrow n$ and holes from $n \rightarrow p$. As the reverse bias voltage is increased, the electric field at the junction becomes significant. When the reverse bias voltage $V = V_Z$, then the electric field strength is high enough to pull valence electrons from the host atoms on the *p*-side which are accelerated to *n*-side. These electrons causes high current at breakdown.

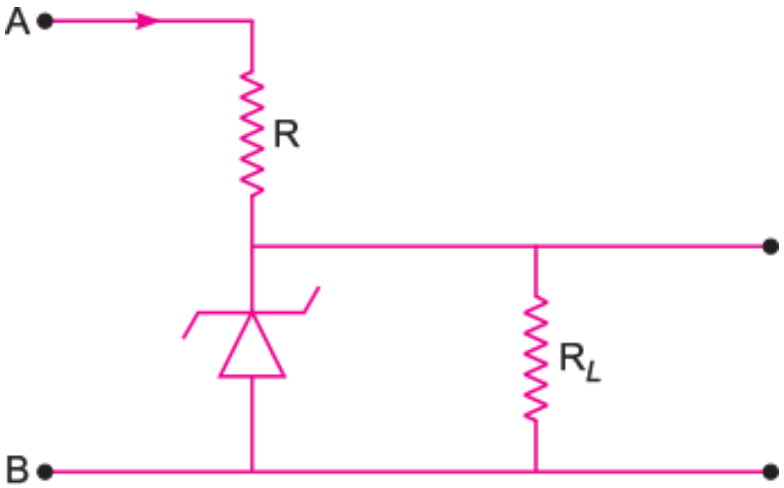
Working:

The unregulated dc voltage output of a rectifier is connected to the zener diode through a series resistance R_s such that the Zener diode is reverse biased. Now, any increase/decrease in the input voltage results in increase/decrease of the voltage drop across R_s without any change in voltage across the Zener diode. Thus, the Zener diode acts as a voltage regulator.

Explanation of voltage regulator.

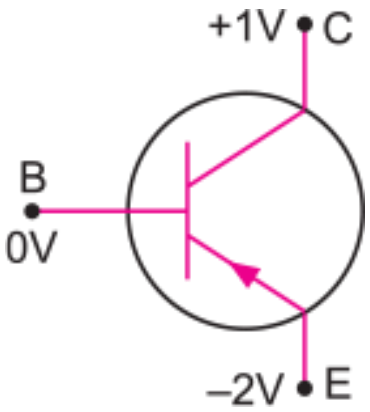


If reverse bias voltage V reaches the breakdown voltage V_Z of zener diode, there is a large change in the current. After that (just above V_Z there is a large change in the current by almost insignificant change in reverse bias voltage. This means diode voltage remains constant.



For example: If unregulated voltage is supplied at terminals A and B, and input voltage increases, the current through resistor R_Z and diode also increases. This current increases the voltage across R_Z without any change in the voltage across diode. Thus, we have a regulated voltage across load resistor R_L.

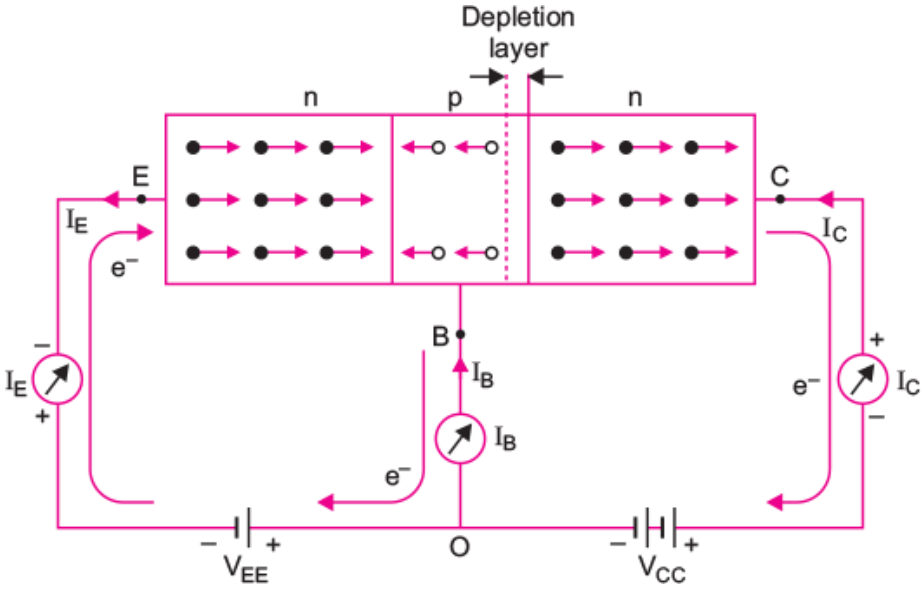
Q. 6. In the figure given alongside, is (i) the emitter and (ii) the collector forward or reverse biased? With the help of a circuit diagram explain the action of npn transistor.
[CBSE (AI) 2012]



Ans. The given transistor is *p-n-p* transistor. The emitter is reverse biased and the collector is forward biased.

Action of *n-p-n* transistor

An *npn* transistor is equivalent to two *p-n* junction diodes placed back to back with their very thin *p*-regions connected together. The circuit diagram for the operation of *npn* transistor is shown in fig. The two batteries V_{EE} and V_{CC} represent emitter supply and collector supply respectively.



Transistor Action: Transistor works only when its emitter-base junction is forward biased and collector-emitter junction is reversed biased. Due to this the majority charge carriers from the emitter, accelerate to collector side and create I_E, I_B and I_C such that $I_E = I_B + I_C$.

Base Current and Collector Current: Under forward bias of emitter-base junction, the electrons in emitter and holes in base are compelled to move towards the junction, thus the depletion layer of emitter-base junction is eliminated. As the base region is very thin, most electrons (about 98%) starting from emitter region cross the base region and reach the collector while only a few of them (about 2%) combine with an equal number of holes of base-region and get neutralised. As soon as a hole (in -region) combines with an electron, a covalent bond of crystal atom of base region breaks releasing an electron-hole pair. The electron released is attracted by positive terminal of emitter battery V_{EE}, giving rise to a feeble base current *(I_B).* Its direction in external circuit is from emitter to base. The hole released in the base region compensates the loss of hole neutralised by electrons.

The electrons crossing the base and entering the collector, due to reverse biasing of collector-base junction, are attracted towards the positive terminal of collector battery V_{CC}. In the process an equal number of electrons leave the negative terminal of battery V_{CC} and enter the positive terminal of battery V_{EE}. This causes a current in collector circuit, called the collector current. In addition to this the collector current is also due to flow of minority charge carriers under reverse bias of base-collector junction. This current is called the leakage current.

Thus, collector current is formed of two components:

(i) Current (I_{nc}) due to flow of electrons (majority charge carriers) moving from emitter to collector.

(ii) Leakage current ($I_{leakage}$) due to minority charge carriers, *i.e.*, $I_c = I_{nc} + I_{leakage}$.

Emitter Current: When electrons enter the emitter battery V_{EE} from the base causing base current or electrons enter the collector battery V_{CC} from the collector causing collector current, an equal number of electrons enter from emitter battery V_{EE} to emitter, causing the emitter current. The process continues.

Relation between Emitter, Base and Collector Currents:

Applying Kirchhoff's *I* law at terminal *O*, we get

$I_E = I_B + I_C$

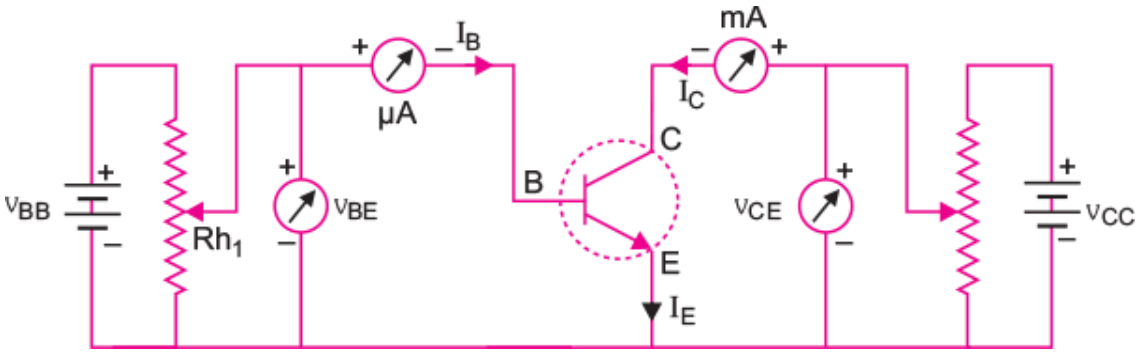
That is, the emitter current I_E is the sum of base current I_B and the collector current I_C. This is the fundamental relation between currents in the bipolar transistor circuit.

Q. 7. Draw the circuit diagram to study the characteristics of npn transistor in common emitter configuration. Sketch typical (i) input characteristics (ii) output characteristics for such a configuration. Explain how the current gain of transistor is calculated from output characteristics. [CBSE Delhi 2009]

OR

Draw the circuit arrangement for studying the input and output characteristics of an n-p-n transistor in CE configuration. With the help of these characteristics define (i) input resistance, (ii) current amplification factor.
[CBSE (AI) 2010; (F) 2013, Delhi 2015]

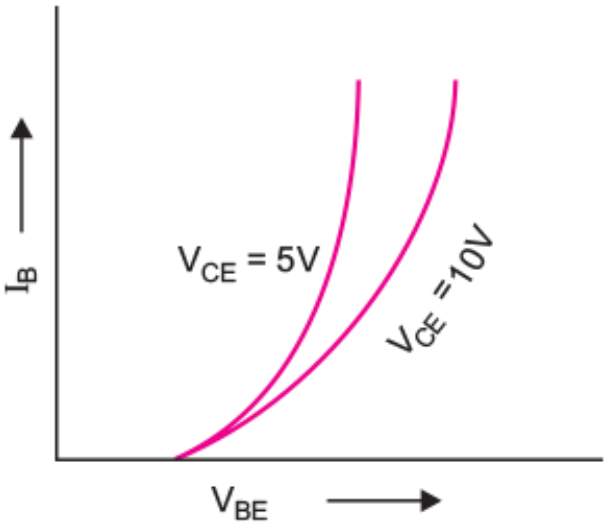
Ans. Characteristic Curves: The circuit diagram for determining the static characteristic curves of an n-p-n transistor in common-emitter configuration is shown in figure.



Common Emitter Characteristics:

(i) Input characteristics are obtained by recording the values of base current I_B for different values of base-emitter voltage V_{BE} at constant collector emitter voltage V_{CE}.

(ii) Output characteristics are obtained by recording the values of collector current I_C for different values of collector emitter voltage V_{CE} at constant base current I_B.



The characteristic curves show:

When collector-emitter voltage V_{CE} is increased from zero, the collector current I_C increases as V_{CE} increases from 0 to 1 V only and then the collector current becomes almost constant and independent of V_{CE}. The value of V_{CE} upto which collector current I_C changes is called the knee voltage V_{knee}

Definition of Input resistance:

Refer to Point 11(*a*) of Basic Concepts.

Definition of Amplification Factor: Refer to Point 12 of Basic Concepts.

Determination of Current Gain

$$\text{Current gain } \beta = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}}$$

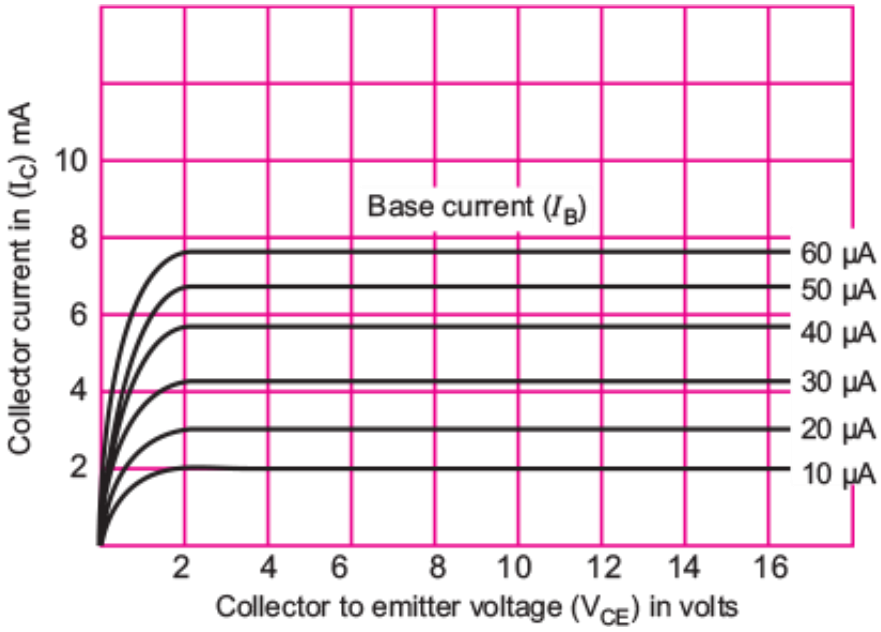
We take the active region of output characteristics *i.e,* the region where collector current (I_C) is almost independent of V_{CE}.

Now we choose any two characteristic curves for given values of I_B and find the two corresponding values of I_C.

Then $\beta = \left(\frac{\Delta I_C}{\Delta I_B}\right) = \frac{(I_C)_2 - (I_C)_1}{(I_B)_2 - (I_B)_1}$

From graph $(I_C)_1$ =5.2 mA, $(I_C)_2$ =7.3 mA,

$(I_B)_1$ =30 μA, $(I_B)_2$ = 40 μA



$$\beta = \frac{(7.3 - 5.2)\ \text{mA}}{(40 - 30)\mu A} = \frac{2.1\times10^{-3}}{10\times10^{-6}} = 210$$

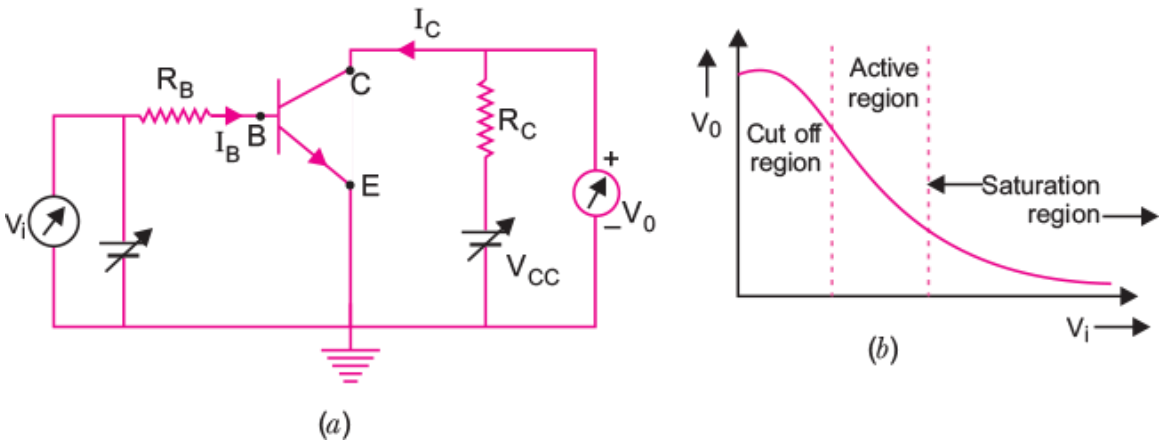
Q. 8. Draw the transfer characteristics of a base biased transistor in common emitter configuration. Explain briefly the meaning of the term active region in these characteristics. For what practical use, do we use the transistor in this active region?

Explain clearly how the active region of the V_0 versus V_i curve in a transistor is used as an amplifier. [CBSE Delhi 2011]

Ans. Transfer characteristics of a base biased transistor in common-emitter configuration:

These are the curves representing the variation of output voltage (V_{BE}) with input voltage (V_{CE})

Circuit Diagram: It is shown in fig. (*a*).



For plotting the curve the input voltage (V_i) is changed in small steps and the corresponding output voltage is measured. The curve obtained is shown in fig. Curve is nearly linear.

In active region the transistor is used as an amplifier.

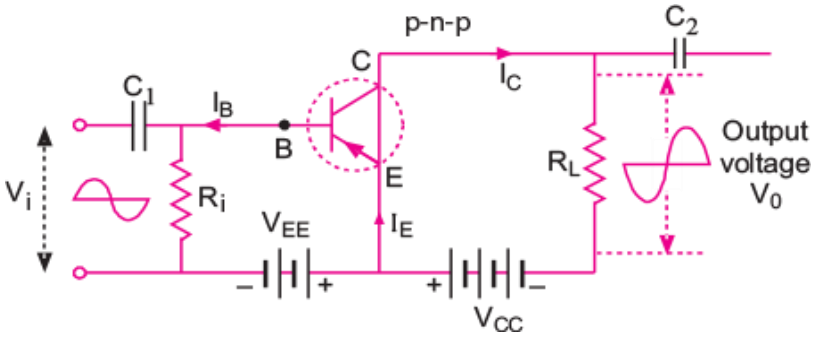
The switching circuits are designed in such a way that the transistor does not remain in active state.

In the active region, a small increase of V_i results in a large (almost linear) increase in I_C. This results in an increase in the voltage drop across R_C.

Q. 9. Draw a labelled circuit diagram of a common emitter amplifier using a p-n-p transistor. Define the term voltage gain and write an expression for it. Explain how the input and output voltages are out of phase by 180° for a common-emitter transistor amplifiers.

Ans. Common-Emitter Transistor Amplifier: Given below is the circuit for a p-n-p transistor. In this circuit, the emitter is common to both the input (emitter-base) and output (collector-emitter) circuits and is grounded. The emitter-base circuit is forward biased and the base-collector circuit is reverse biased.

In a common-emitter circuit, the collector-current is controlled by the base-current rather than the emitter-current. Since in a transistor, when input signal is applied to base, a very small change in base-current provides a much larger change in collector-current and thus extremely large current gains are possible.



When positive half cycle is fed to the input circuit, it opposes the forward bias of the circuit which causes the collector current to decrease. It decreases the voltage drop across load R_L and thus makes collector voltage more negative. Thus, when input cycle varies through a positive half cycle, the output voltage developed at the collector varies through a negative half cycle and vice versa. Thus, the output voltage in common-emitter amplifier is in antiphase with the input signal or the output and input voltages are 180° out of phase.

Current Gain. The ratio of change in collector current (ΔI_C) to the change in base current (ΔI_B) is called the alternating current gain denoted by β Thus,

$$\beta(\text{ ac }) = \frac{\Delta I_C}{\Delta I_B}$$

β has positive values and is generally greater than 20.

Voltage Gain. The voltage gain of common- emitter transistor amplifier is given by

$$A_v = \frac{\Delta V_{out}}{\Delta V_{in}} = \frac{R_L \, \Delta I_C}{R_i \, \Delta \, I_b} = \left(\frac{\Delta I_C}{\Delta I_b}\right) . \frac{R_L}{R_i}$$

$$\Rightarrow \qquad A_v = \beta \frac{R_L}{R_i}$$

Q. 10. (a) Differentiate between three segments of a transistor on the basis of their size and level of doping.

(b) How is a transistor biased to be in active state? [CBSE Delhi 2014]

(c) With the help of necessary circuit diagram describe briefly how npn transistor in CE configuration amplifies a small sinusoidal input voltage. Write the expression for ac current gain.

OR

Explain with the help of a circuit diagram the working of npn transistor as a common emitter amplifier. [CBSE Delhi 2009, South 2016]

OR

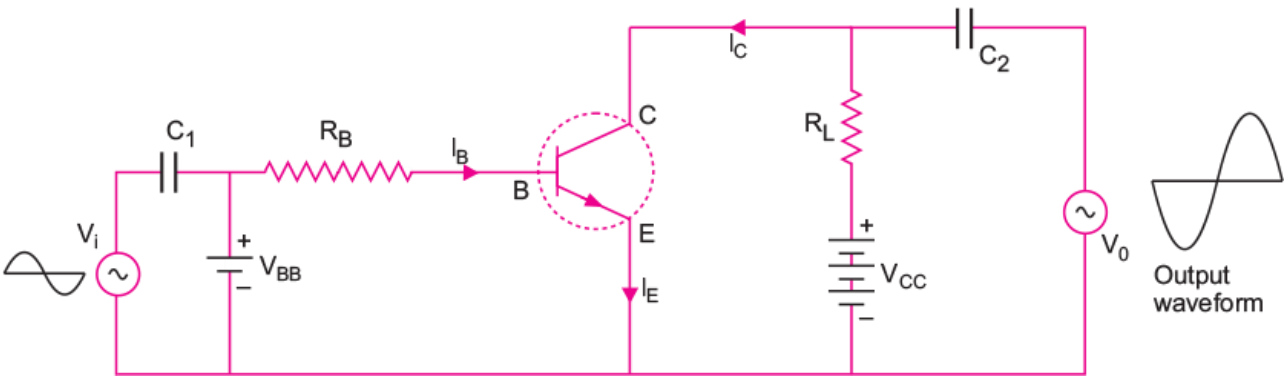
Draw the circuit diagram of a common-emitter amplifier using an npn transistor. What is the phase difference between the input signal and output voltage? Draw the input and output waveforms of the signal. Write the expression for its voltage gain. State two reasons why a common emitter amplifier is preferred to a common base amplifier. [CBSE (AI) 2009, Allahabad 2015]

Ans. (a) Emitter: It is of moderate size and heavily doped.

Base: It is very thin and lightly doped.
Collector: The collector side is moderately doped and larger in size as compared to the emitter.

(b) Transistor is said to be in active state when its emitter-base junction is suitably forward biased and base-collector junction is suitably reverse biased.

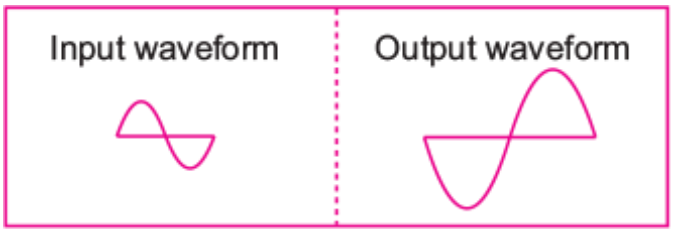
(c) The circuit of common emitter amplifier using n-p-n transistor is shown below:



Working: If a small sinusoidal voltage, with amplitude V_s, is superposed on dc basic bias (by connecting the sinusoidal voltage in series with base supply V_{BB}), the base current will have sinusoidal variations superposed on the base current I_B. As a consequence the collector current is also sinusoidal variations superimposed on the value of collector current I_C, this will produce corresponding amplified changes in the value of output voltage V_0. The ac variations across input and output terminals may be measured by blocking the dc voltage by large capacitors.

The phase difference between input signal and output voltage is 180°.

The input and output waveforms are shown in fig.



Voltage gain $A_v = \beta \frac{R_L}{R_i}$;

ac current gain, $\beta_{ac} = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}}$

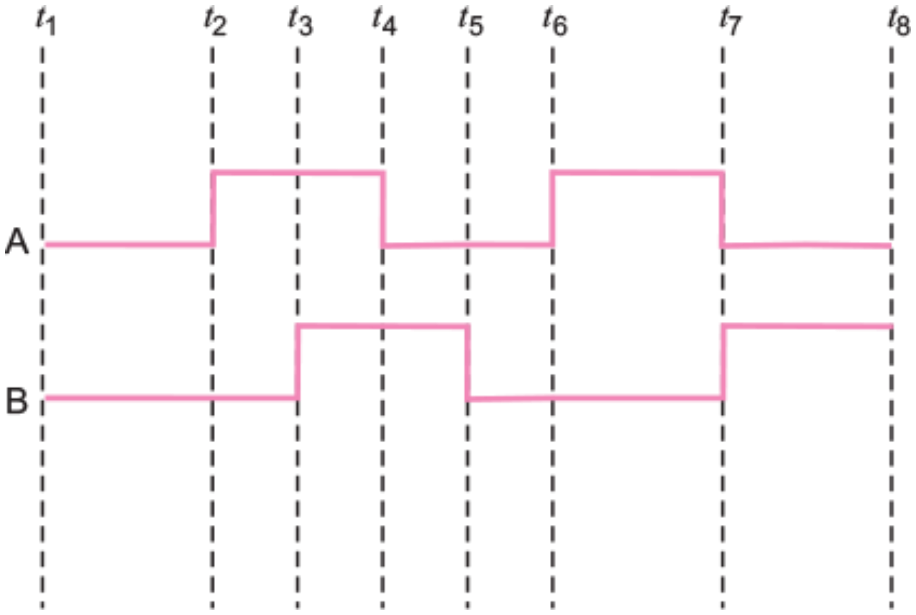
Reasons for using a common emitter amplifier:

(i) Voltage gain is quite high.
(ii) Voltage gain is uniform over a wide frequency range or power gain is high.

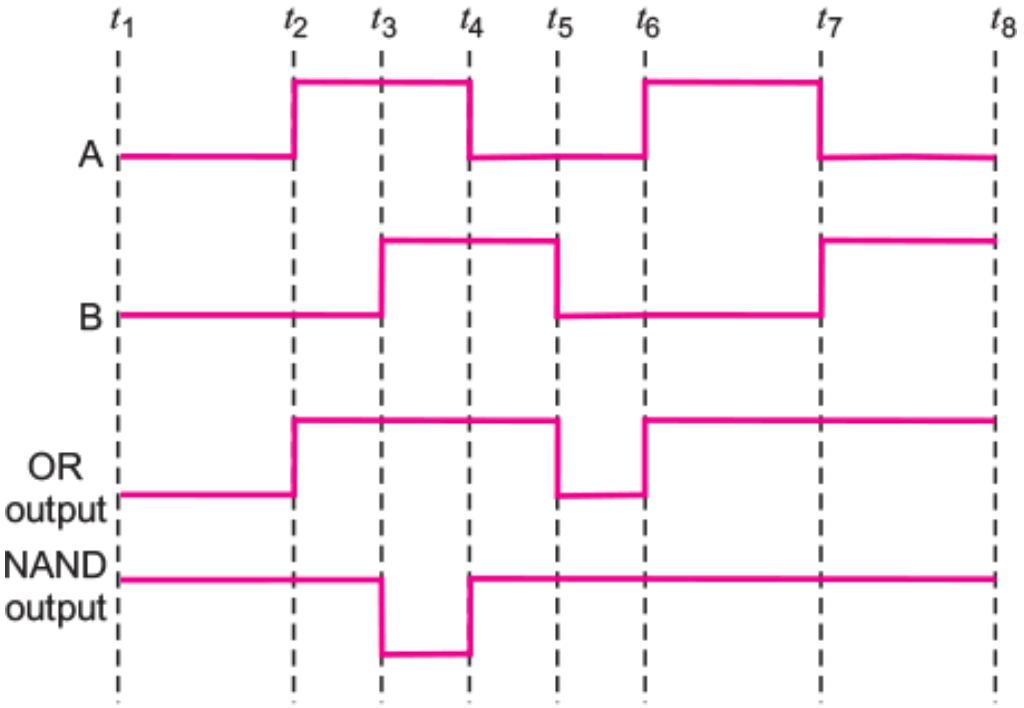
Q. 11. Answer the following questions.

(i) Show the output waveforms (Y) for the following inputs A and B of

(i) OR gate (ii) NAND gate [CBSE Delhi 2012]

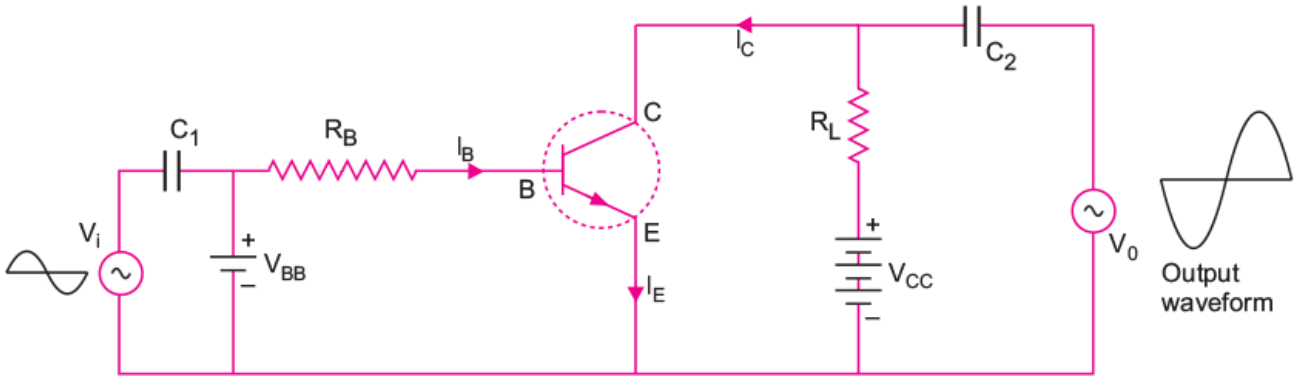


Ans. (i) Output waveforms for the following inputs A and B of OR gate and NAND gate.



Q. 12. Draw a simple circuit of a CE transistor amplifier. Explain its working. Show that the voltage gain AV, of the amplifier is given by $A_V = -\frac{B_{ac} R_L}{r_i}$, where β_{ac} is the current gain, R_L is the load resistance and r_i is the input resistance of the transistor. What is the significance of the negative sign in the expression for the voltage gain?
[CBSE Delhi 2012]

Ans. Circuit diagram of CE transistor Amplifier.



When an ac input signal V_i (to be amplified) is superimposed on the bias V_{BB}, the output, which is measured between collector and ground, increases.

We first assume that $V_i = 0$. Then, applying Kirchhoff's law to the output loop.

$V_{CC} = V_{CE} + I_C R_L$

Similarly, the input loop gives

$V_{BB} = V_{BE} + I_B R_B$

When V_i is not zero, we have

$V_{BE} + V_i = V_{BE} + I_B R_B + \Delta I_B (R_B + R_i)$

$\Rightarrow V_i = \Delta I_B (R_B + R_i) \quad \Rightarrow \quad V_i = r\Delta I_B$

Change in I_B causes a change in I_C

$$\text{Hence, } \beta_{ac} = \frac{\Delta I_C}{\Delta I_B} = \frac{I_C}{I_B}$$

$$\text{As } \Delta V_{CC} = \Delta V_{CE} + R_L \Delta I_C = 0 \quad \Rightarrow \quad \Delta V_{CE} = -R_L \Delta I_C$$

The change in V_{CE} is the output voltage V_0

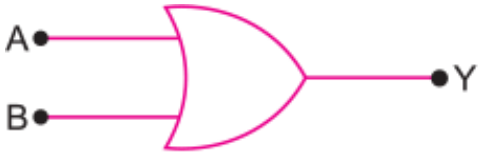
$$\Rightarrow V_0 = R_L \Delta I_C = \beta_{ac} \Delta I_B R_L$$

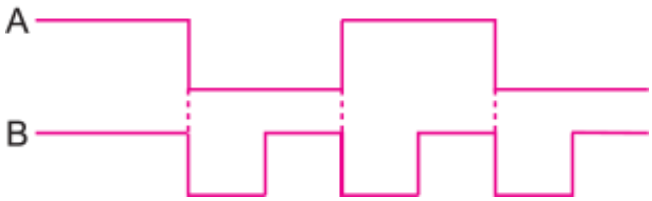
The voltage gain of the amplifier is

$$A_V = \frac{V_0}{V_i} = \frac{\Delta V_{CE}}{r\Delta I_B} = \frac{-\beta_{ac} \Delta I_B R_L}{r\Delta I_B} = -\beta_{ac} \frac{R_L}{r}$$

Negative sign in the expression shows that output voltage and input voltage have phase difference of π.

Q. 13. In fig., the circuit symbol of a logic gate and two input waveforms A and B are shown:





(i) Name the logic gate.
(ii) Write its truth table.
(iii) Give the output waveform.

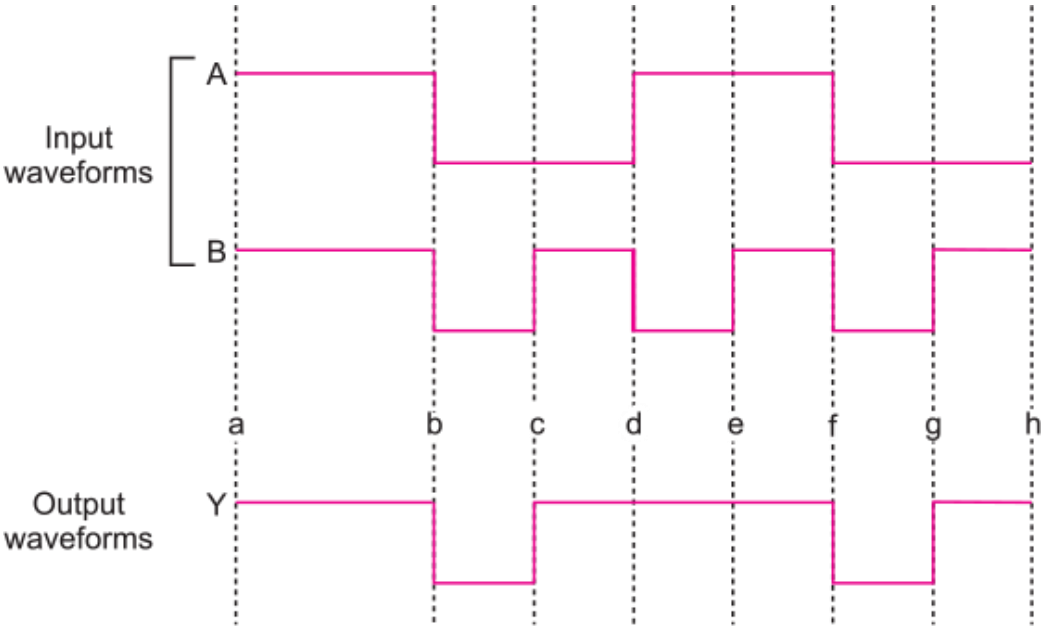
Ans. (i) The logic gate shown is **OR gate.**

(ii) Truth table of OR gate is

Truth table of OR gate is

A	*B*	*Y*
0	0	0
1	0	0
0	1	0
1	1	1

(iii) The input waveforms A and B are discrete square waves. The components of waveforms A and B are shown by vertical dotted lines.



Between *a* and *b, A* = 1, *B* = 1 → Y =1

Between *b* and *c*, *A* = 0, *B* = 0 → Y = 0

Between *c* and *d, A* = 0, *B* = 1 → Y = 1

Between *d* and *e*, *A* =1, *B* = 0 → Y = 1

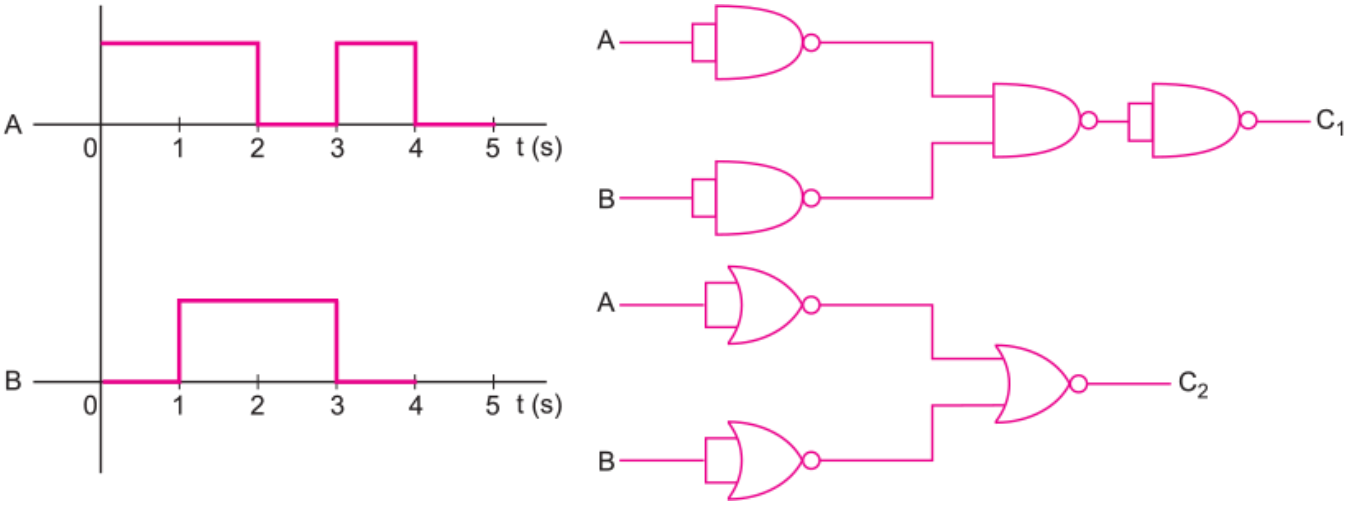
Between *e* and *f*, *A* = 1, *B* = 1 → Y = 1

Between *f* and *g*, *A* = 0, *B* = 0 → Y = 0

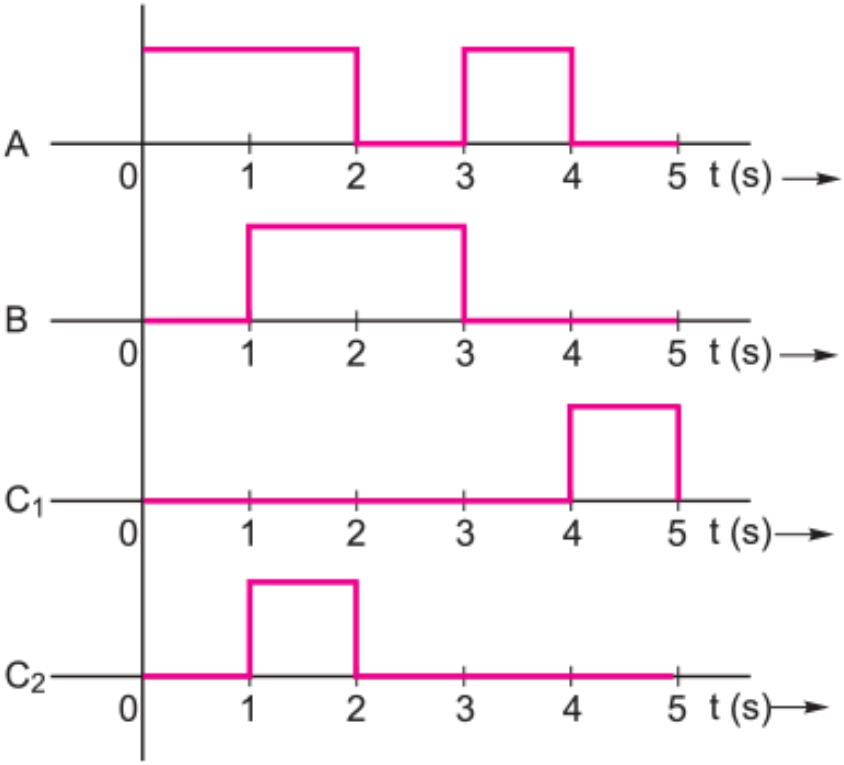
Between *g* and *h*, *A* = 0, *B* = 1 → Y = 1

Accordingly, the waveform *Y* is shown as above.

Q. 14. Draw the output signals C_1 and C_2 in the given combination of gates (Fig.) [HOTS][NCERT Exemplar]



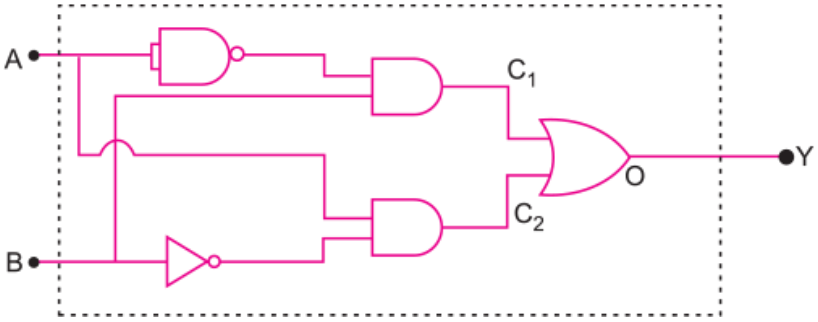
Ans. The output signals C_1 and C_2 are as shown.

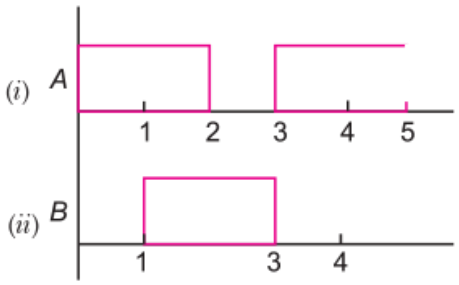


Q. 15. Input signals A and B are applied to the input terminals of the 'dotted box' set-up shown here. Let Y be the final output signal from the box.

Draw the wave forms of the signals labelled as C_1 and C_2 within the box, giving (in brief) the reasons for getting these wave forms. Hence draw the wave form of the final output signal Y. Give reasons for your choice.

What can we state (in words) as the relation between the final output signal Y and the input signals A and B? [HOTS]





Ans.

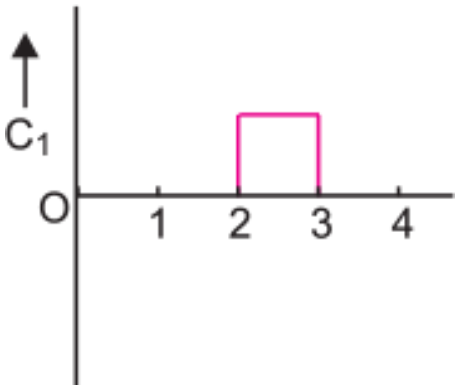
$$C_1 = \bar{A}.B, C_2 = A.\bar{B}$$

$$Y = C_1 + C_2 = \bar{A}B + \bar{B}A$$

This is Boolean expression for **NOT XOR gate.**

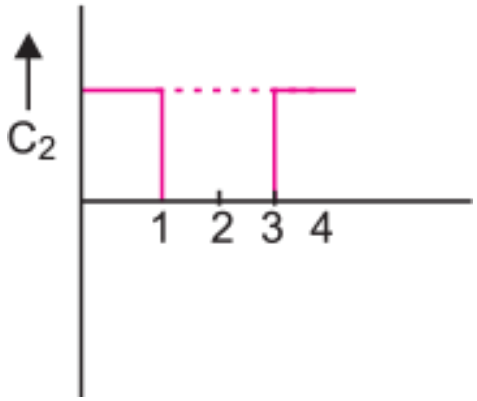
$$C_1 = \bar{A}.B$$

	A	B	$C_1 = \bar{A}.B$
From 0 to 1	1	0	0
From 1 to 2	1	1	0
From 2 to 3	0	1	1
From 3 to 4	1	0	0
From 4 onwards	1	0	0



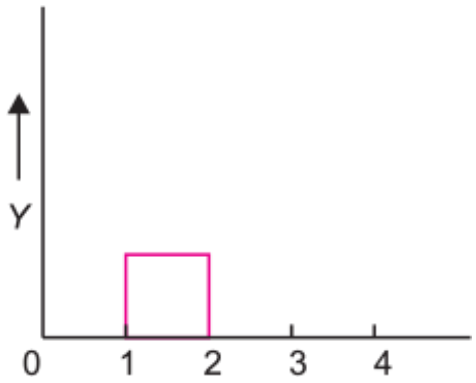
$C_2 = A \cdot \bar{B}$

	A	B	$C_2 = A \cdot \bar{B}$
From 0 to 1	1	0	1
From 1 to 2	1	1	0
From 2 to 3	0	1	0
From 3 to 4	1	0	1
From 4 onwards	1	0	1



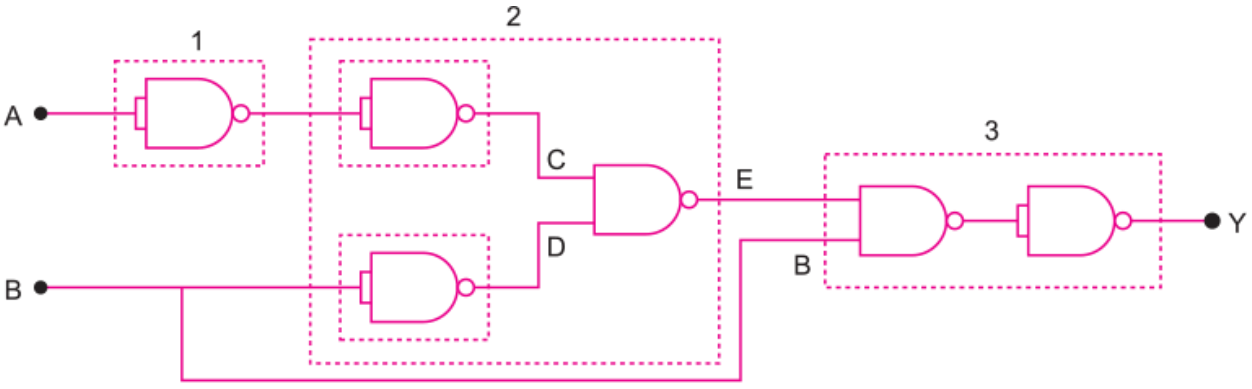
$Y = C_1 \bar{+} C_2$

	A	B	$Y = C_1 \bar{+} C_2$
From 0 to 1	0	1	0
From 1 to 2	0	0	1
From 2 to 3	1	0	0
From 3 to 4	0	1	0
From 4 onwards	0	1	0



The gate shown in circuit is NOT XOR gate. According to definition the output Y is obtained only if either both signals are 0 or 1.

Q. 16. Identify which logic gate OR, AND and NOT is represented by the circuits in the dotted line boxes 1, 2 and 3. Give the truth table for the entire circuit for all possible values of A and B. [HOTS]



Ans. The dotted line box 1 represents NOT gate.

The dotted line box 2 represents OR gate.

The dotted line box 3 represents AND gate.

The output of box 1 is $\bar{A}$

The inputs of box 2 are A and $\bar{B}$

As box 2 is OR gate, therefore, output of box 2 is E = $(\bar{A} + B)$.

The inputs of box 3 are E and B Box 3 represents AND gate; therefore, output of box 3 is

$$Y = EB = (\bar{A} + B)\, B$$

Truth table of the entire circuit is

A	B	$Y = (\bar{A} + B)B$
0	0	$(1 + 0) \cdot 0 = 0$
1	0	$(0 + 0) \cdot 0 = 0$
0	1	$(1 + 1) \cdot 1 = 1 \cdot 1 = 1$
1	1	$(0 + 1) \cdot 1 = 1 \cdot 1 = 1$