CHAPTER 4

Thyristors

4.1 Thyristor

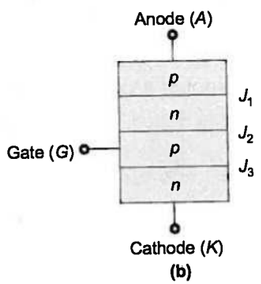
- The name 'Thyristor', is derived by a combination of the capital letters from THYRatron and transISTOR.
- International Electrotechnical Commission (IEC) in 1963 decided the definition of thyristor as under:
  (*i*) It constitues three or more p-n junctions.
  (*ii*) It has two stable states, an ON-state and an OFF-state and can change its state from one to another.
- Thyristor is a four layer, three-junction, p-n-p-n semiconductor switching device.

4.2 Silicon Controlled Rectifier (SCR)

- SCR is the oldest and first member of the thyristor family.
- It is called SCR because, silicon is used for its construction and its operation as a rectifier (very low resistance in forward conduction and very high resistance in the reverse direction) can be controlled.
- It has three terminals:
  (*i*) Anode (*A*)
  (*ii*) Cathode (*K*)
  (*iii*) Gate (*G*)

Circuit symbol of SCR
(a)

- The structure of SCR



(b)

***Figure*-4.1 :** *(a) and (b)*

The terminal connected to outer '*p*' region is called Anode (*A*).
The terminal connected to outer '*n*' region is called Cathode (*K*).
The terminal connected to inner '*p*' region is called the Gate (*G*).

- SCR is a unidirectional device. It blocks the current flow from cathode to anode.

Static V-I Characteristics of SCR

- An elementary circuit diagram for obtaining static V-I characteristics of SCR is shown in figure,

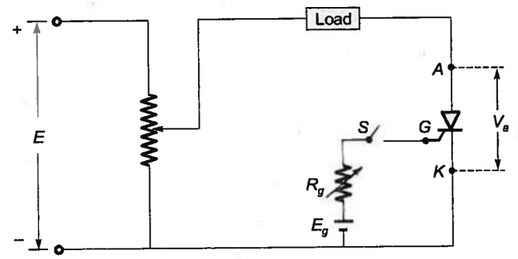


***Figure*-4.2**

- The Anode and Cathode are connected to main source through the load.
- The Gate and Cathode are fed from another source 'E_g'.
- The static V-I characteristics of SCR are shown below.

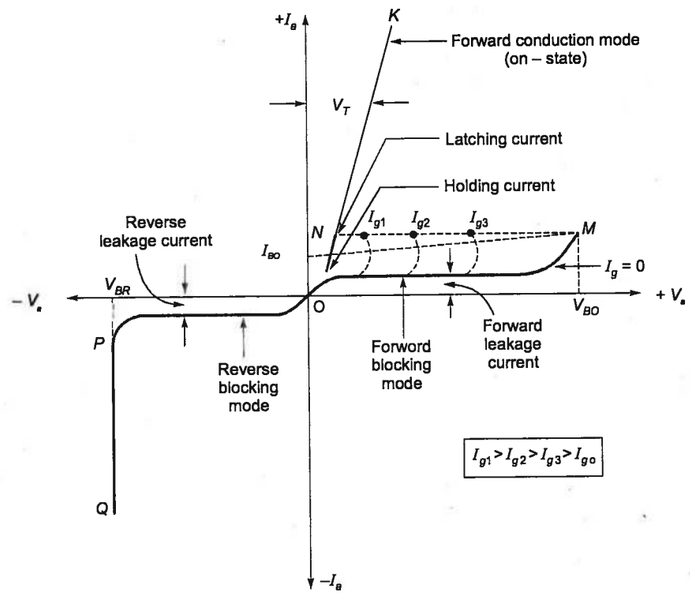


***Figure*-4.3**

V_a = Anode voltage ; I_a = Anode current
V_{BO} = Forward breakover voltage
V_{BR} = Reverse breakdown voltage

I_g = Gate current
I_L = Latching current
I_H = Holding current

- The three basic modes of operation of SCR are:
  (*i*) Forward blocking mode
  (*ii*) Forward conduction mode
  (*iii*) Reverse blocking mode

1. Forward Blocking Mode

- When anode is at a higher potential than cathode, with gate circuit open, thyristor is said to be forward biased.
- It is seen from the figure that J_1, J_3 are forward bias but junction J_2 is reverse bias.
- In this mode, a small current, called forward leakage current flows from anode to cathode.
- OM in the VI characteristics represents the forward blocking mode of SCR.
- SCR is treated as an open switch in the forward blocking mode.

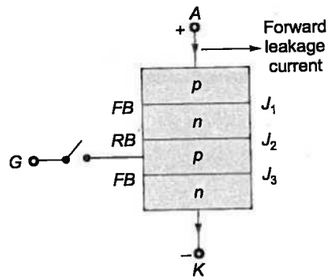


Figure-4.4

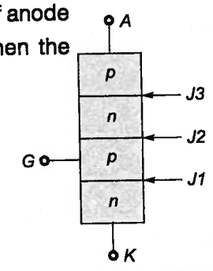
2. Forward Conduction Mode

- When anode to cathode forward voltage is increased with gate circuit open, reverse biased junction J_2 will have an avalanche breakdown at a voltage called forward breakover voltage V_{BO}.
- After this breakdown, thyristor gets turned ON with point '*M*' at once shifting to '*N*'. Here NK represents the forward conduction mode.
- A thyristor can be brought from forward blocking mode to forward conducting mode by turning it on by applying
  (*i*) a positive Gate pulse between gate and cathode (or)
  (*ii*) a forward breakover voltage (VBO) across anode and cathode
- Voltage drop across the SCR 'V_T' increases slightly with an increase in anode current. It can be seen from *NK*.

Example - 4.1 **Figure shows a thyristor with the standard terminations of anode (*A*), cathode (*K*), gate (*G*) and the different junctions named *J*1, *J*2 and *J*3. When the thyristor is turned on and conducting.**

(a) *J*1 and *J*2 are forward biased and *J*3 is reverse biased
(b) *J*1 and *J*3 are forward biased and *J*2 is reverse biased
(c) *J*1 is forward biased and *J*2 and *J*3 are revese biased
(d) *J*1, *J*2 and *J*3 are all forward biased

Solution:(d)



Latching Current (I_L)

- It is defined as the minimum value of anode current (I_a) which it must attain during turn-on process to maintain conduction when gate signal is removed.
- The gate pulse width should be choosen to ensure that the anode current rises above the latching current (I_L).

Example - 4.2 **Latching current for an SCR, inserted in between a dc voltage source of 200 V and the load, is 100 mA. Compute the minimum width of gate pulse current required to turn-on this SCR in case the load consists of (a) L = 0.2 H, (b) R = 20 Ω in seris with L = 0.2 H and (c) R = 20 Ω in series with L = 2.0 H.**

Solution:

(a) When load consists of pure inductance L, the voltage equation is

$$E = L\cdot\frac{di}{dt} \text{ or } di = \frac{E}{L}dt \text{ or } i = \frac{E}{L}t$$

$$\therefore \quad 0.100 = \frac{200}{0.2}t \text{ or } t = \frac{0.1\times 0.2}{200} = 100\ \mu\text{sec}$$

Thus, minimum gate-pulse width is 100 μsec.

(b) The voltage equation for R-L load is

$$E = R_i + L\frac{di}{dt} \quad \text{or} \quad i = \frac{E}{R}\left(1-e^{-\frac{R}{L}t}\right) \text{ or } 0.100 = \frac{200}{20}(1-e^{-100t})$$

or, t = 100.503 μsec.

∴ Minimum gate-pulse width is 100.503 μsec

(c)
$$i = \frac{E}{R}\left(1-e^{-\frac{R}{L}t}\right) \quad \text{or} \quad 0.1 = \frac{200}{20}(1-e^{-10t}) \text{ or } t = 1005.03\ \mu\text{sec}$$

This example shows that if load resistance is increased from zero to 20 Ω, the gate-pulse width remains almost unaffected. But with an increase in inductance from 0.2H to 2H, the gate-pulse width becomes 10 times its previous value.

Holding Current (I_H)

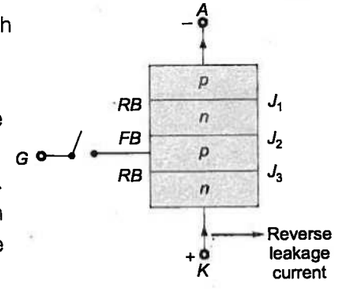
- It is defined as the minimum value of anode current below which it must fall for turning off the SCR.
- Latching current (I_L) is more than holding current (I_H).

$$\boxed{I_L > I_H}$$

- Latching current (I_L) is associated with turn-on process.
  Holding current (I_H) is associated with turn-off process.

3. Reverse Blocking Mode

- When cathode is made high potential with respect to anode with gate open, then the SCR is said to be reverse biased.
- J_1 and J_3 are reverse biased and J_2 is forward biased.
- A small current flows through the SCR this is called as reverse leakage current.
- This is reverse blocking mode, called the OFF state of the SCR.
- If the reverse voltage is increased, then at reverse breakdown voltage (V_{BR}), an avalanche occures at J_1 and J_3 and the reverse current increases rapidly. (*PQ*)
- The SCR in the reverse blocking mode may therefore be treated as an open switch.



Dynamic or Switching Characteristics of SCR

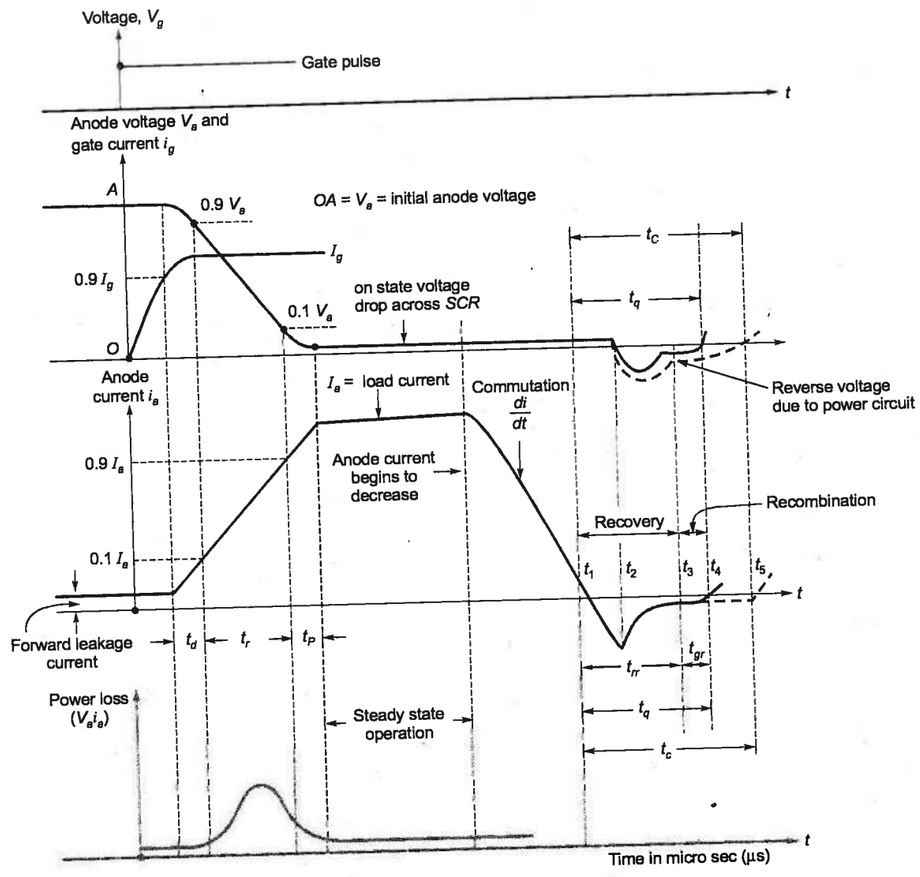


***Figure*-4.6**

- SCR voltage and current waveforms during turn-on and turn-off process.
- Switching characteristics are also known as dynamic characteristics or transient characteristics.
- The time variations of the voltage across the SCR and the current through it during turn-on and turn-off processes give the dynamic or switching characteristics.

Switching Characteristics During Turn-on

- SCR turn on time, is defined as the time during which SCR changes from forward blocking mode to final on state.
- Total turn on-time can be divided into three intervals;
  (*i*) Delay time (t_d) (*ii*) Rise time (t_r) (*iii*) Spread time (t_p)

$$\text{Turn on time} = t_d + t_r + t_p$$

Delay Time (t_d)

The delay time (t_d) is the time between the instant at which gate current reaches 0.9 I_g to the instant at which anode current reaches 0.1 I_a. Here I_g and I_a are respectively the final values of gate and anode currents.

(or)

The delay time (t_d) may also be defined as the time during which anode voltage falls from V_a to 0.9 V_a where V_a = initial value of anode voltage.

(or)

The time during which anode current rises from forward leakage current to 0.1 I_a where I_a = final value of anode current.

Rise Time (t_r)

The time taken by the anode current to rise from 0.1 I_a to 0.9 I_a.

(or)

The rise time is also defined as the time required for the forward blocking off state voltage to fall from 0.9 to 0.1 of its initial value *OA*.

During rise time, turn-on losses in the thyristor are high due to high anode voltage (V_a) and large anode current (I_a) occuring together in the thyristor.

Spread Time (t_p)

The time taken by the anode current to rise from 0.9 I_a to I_a.

(or)

It is also defined as the time for the forward blocking voltage to fall from 0.1 of its initial value to the on-state voltage drop.

Switching Characteristics During Turn-off

SCR turn-off means that it has changed from on to off state and is capable of blocking the forward voltage. This dynamic process of the SCR from conduction state to forward blocking state is called commutation process or turn-off process.

If forward voltage is applied to the SCR at the moment its anode current falls to zero, the device will not be able to block this forward voltage, as the carriers (holes and electrons) in the four layers are still favourable for conduction. The device will therefore go into conduction immediately even though gate signal is not applied. So to solve this problem it is essential that the thyristor is reverse biased for a finite period after the anode current has reached zero.

Turn-off Time (t_q)

It is the time between the instant anode current becomes zero and the instant SCR regains forward blocking capability.

During this time (t_q) all the excess carriers from four layers of SCR must be removed.

The turn-off time is divided into two intervals:

(*i*) Reverse recovery time (t_{rr})

(*ii*) Gate recovery time (t_{gr})

$$t_q = t_{rr} + t_{gr}$$

- After 't_1', anode current builds up in the reverse direction with the same *di/dt* slope. The reason for the reversal of anode current is due to the presence of charge carriers stored in the four layers.
- At instant t_3, when reverse recovery current has fallen to nearly zero value, end junctions J_1 and J_3 recover and SCR is able to block the reverse voltage.
- At the end of reverse recovery period 't_3', the middle junction 'J_2' still has charges, therefore, the thyristor is not able to block the forward voltage at t_3.
- The charge carriers at J_2 cannot flow to the external circuit, therefore they must decay only by recombination. This is possible if a reverse voltage is maintained across SCR. The time taken for this ($t_4 - t_3$) is called gate recovery time (t_{gr}).
- The thyristor turn-off time 't_q' is depended upon magnitude of forward current, *di/dt* at the time of commutation and junction temperature.

Circuit Turn-off Time 't_c'

It is defined as the time between the instant anode current becomes zero and the instant reverse voltage due to practical circuit reaches zero.

NOTE: $t_c > t_q$ for reliable turn-off, otherwise the device may turn-on at an undesired instant, a process called commutation failure.

- Thyristors with slow turn-off time are called converter grade SCR's.
  Ex.: Phase controlled rectifiers, cyclo-converters and ac voltage controllers.
- SCR with fast turn-off time are called inverter grade SCR's.
  Ex.: Inverters, choppers and forced commutation converters.

Gate Characteristics of SCR

Trigger circuit connected to gate-cathode circuit of an SCR.

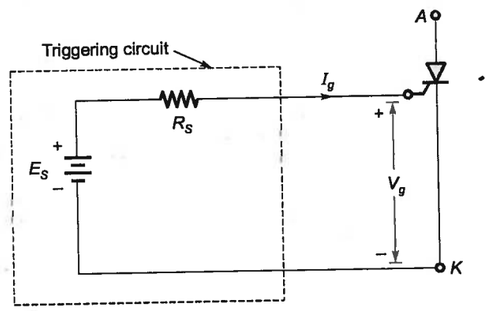


Figure-4.7

$$E_s = V_g + I_g R_s$$

Forward Gate Characteristics of SCR

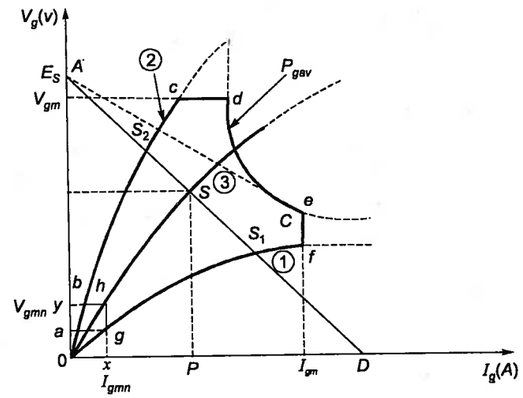


Figure-4.8

- V_g, I_g characteristics has spread between two curves (1) and (2) as shown in figure.
- Curve (1) correspondes to gate with maximum doping. So it requires lowest votlage values that must be applied to turn-on the SCR.
- Curve (2) corresponds to gate with minimum doping. So it requires highest possible voltage values that can be safely applied to gate circuit.
- Each SCR has maximum limits as V_{gm} for gate voltage and I_{gm} for gate current. There is also average gate power dissipation 'P_{gav}' specified for each SCR.
- V_{gmn} and I_{gmn} are the minimum limits for gate voltage and gate current for turn-on of SCR.
- The above figure shows that the preferred gate drive area for an SCR is '*bcdefghb*'.
- For selecting the operating point of the circuit load line is drawn from *A* to *D*. ($\overline{AD}$ = load line), where as.
  E_s = Gate source voltage = *OA*
  OD = Trigger circuit short circuit current = $[E_s/R_s]$
  Curve (3) gives the operating point 'S'. Thus for this SCR,
  Gate voltage = *PS* and
  Gate current = *OP*
- Operating point '*s*' which may change from s_1 to s_2 and must lie within the limit curves 1 and 2 and must be as close to the P_{gav} curve as possible.
- The minimum value of gate source series resistance 'R_s', is obtained by drawing a line AC tangent to P_{gav} curve.

Example - 4.3 **For an *SCR*, gate-cathode characteristic is given by $V_g = 1 + 10\, I_g$. Gate source voltage is a rectangular pulse of 15 V with 20 μsec duration. For an average gate power dissipation of 0.3 W and a peak gate drive power of 5 W, compute:**

(*i*) the resistance to be connected in series with the *SCR* gate,
(*ii*) the triggering frequency, and
(*iii*) the duty cycle of the triggering pulse.

Solution:

(*i*) Here, $V_g = 1 + 10\,I_g$

For pulse-triggering of SCRs,

(Peak gate voltage) (Peak gate current) during pulse-on period = peak gate drive power, P_{gm}

As the gate pulse width is 20 μsec (less than 100 μsec), the dc data does not apply. Had the gate pulse width been more than 100 μsec, the relation $(1 + 10I_g)\,I_g = 0.3$ W will hold good. But as the dc data does not apply, we have here

$$(1 + 10I_g)\,I_g = 5\text{ W} \quad \text{or} \quad 10I_g^2 + I_g - 5 = 0$$

Its solution gives, $I_g = 0.659$ A

$\therefore$ Amplitude of current pulse = 0.659 A

During the pulse-on period,

$$E_s = R_s I_g + V_g \quad \text{or} \quad 15 = R_s I_g + 1 + 10I_g$$

$$\therefore \quad R_s = \frac{15-1}{0.659} - 10 = 11.244\ \Omega$$

(*ii*) $$P_{gm} = \frac{P_{gav}}{fT} \qquad \text{(Here } T = 20\ \mu\text{sec)}$$

$\therefore$ Triggering frequency, $f = \dfrac{0.3\times10^6}{5\times20} = 3$ kHz

(*iii*) Duty cycle, $\delta = fT = 3 \times 10^3 \times 20 \times 10^{-6} = 0.06$

Rating of Thyristor

Thyristor current $(I_T)_{rms}$ rating:

Rms rating of the thyristor is specified by manufacturer

$$\underbrace{(I_T)_{rms}}_{\substack{\text{Calculated value}\\ \text{in converter}}} \quad \text{value} \le (I_T)_{rms} \text{ rating}$$

It remains same for all the conduction angle.

I_{TAV} (Average on state current):

It is not specified by manufacturer.

It depends on the smoothness of thyristor current wave form

$$I_{TAV}\text{ rating of SCR} = \frac{(I_T)_{rms}\text{ rating of SCR}}{\text{Form factor}}$$

As the conduction angle of SCR is increase then smoothness of current wave form is improved that is form factor decreases and I_{TAV} rating of SCR increases.

As load inducatnce (L) increases then smoothness of SCR current wave form is also increases that is form factor reduces and I_{TAV} rating of SCR increases.

I^2t Rating of SCR

I^2t rating of SCR is specified for a selection of a proper fuse or other protective equipment.

I^2t rating of thyristors > I^2t rating of fuse.

Surge Current Rating of SCR

Surge current rating is inversely proportional to the duration of the surge.

This rating is specified interms of the number of surge cycles with corresponding surge current peak.

n-cycle surge current rating (I_{sn}): It is the surge current that the SCR with stands for n-cycle.

$$I_{sn}^2 \cdot n \cdot \frac{T}{2} = I^2t \text{ rating of SCR} \quad \left\{\begin{matrix}\text{One cycle SCR} \Rightarrow T/2 \text{ sec}\\ \text{Conducts}\end{matrix}\right\}$$

$$I_{sn}^2 = \frac{2I^2t}{nT}$$

One cycle surge current rating (I_{s1}): It is the surge current that the SCR withstands for one cycle

$$I_{s_1}^2 \cdot \frac{T}{2} = I_{sn}^2 \cdot n \cdot \frac{T}{2}$$

$$I_{s1} = \sqrt{n}\, I_{sn}$$

Sub-cycle Surge Current Rating $(I_s)_{1/n}$

It is the surge current that the SCR withstand for $(1/n)^{th}$ period of a cycle

$$(I_s)_{1/n}^2 \cdot \frac{1}{n}\left(\frac{T}{2}\right) = I_{s1}^2 \cdot 1 \cdot \frac{T}{2}$$

$$\boxed{(I_s)_{1/n} = \sqrt{n}\, I_{s1}}$$

Example - 4.4 Half (1/2) cycle surge current rating.

Solution:

$$(I_s)_{1/2} = \sqrt{2}\, I_{s1}$$

Protection of SCR

***di/dt* Protection**

- When a thyristor is forward biased and is turned on by a gate pulse, conduction of anode current begins. If the rate of rise of anode current (di/dt) is very fast compared with the spreading velocity of a turn-on process, local hot spots will be formed. This localised heating may destroy the thyristor. Therefore, the (di/dt) rate of rise of anode current at the time of turn-on must be kept below the specified limiting value.
- By using a small inductor, called *di/dt* inductor, in series with the anode circuit.

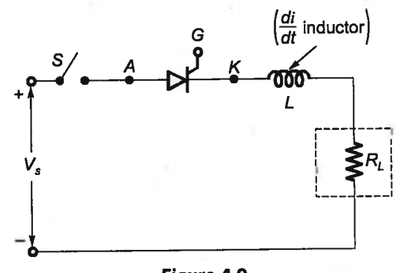


Figure-4.9

dv/dt Protection

- If the rate of rise of suddenly applied voltage across thyristor is high the device may get turned-on. Such phenomena of turning on a thyristor, called *dv/dt* turn-on must be avoided as it leads to false operation.
- False turn-on of a SCR by large *dv/dt*, even with out application of gate signal can be prevented by using a Snubber circuit in parallel with the device.

Design of Snubber Circuit

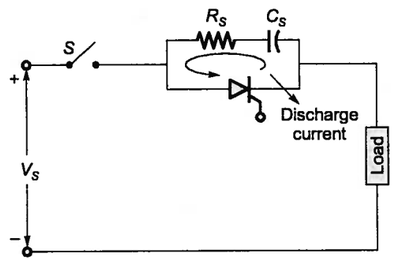


***Figure*-4.10 :** *Snubber circuit across SCR*

- A snubber circuit consists of a series combination of resistance R_s and capacitance C_s in parallel with the thyristor as shown in figure.

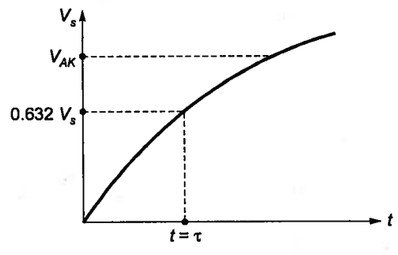


***Figure*-4.11**

- When switch '*s*' is closed, a sudden voltage is appears across the circuit. Capacitor C_s behaves like a short circuit, therefore voltage across SCR is zero. With the passage of time, voltage across C_s builts up at a slow rate such that the *dv/dt* across 'C_s' and therefore across SCR is less than the specified maximum *dv/dt* rating of the device.
- In order to limit the magnitude of discharge current, a resistance R_s is inserted in series with 'C_s'.

Over Voltage Protection

A SCR may be subjected to internal or external over voltages.

Internal Over Voltages

Due to the presence of the series inductance L_s of the SCR circuit, large transient voltages $\left(L\frac{di}{dt} = v_L\right)$ is produced and this internal voltage may be several times the breakover voltage of the SCR, the thyristor may be destroyed permanently.

External Over Voltages

- Over voltages are caused due to the lightning strokes and switching surges.
- For reliable operation, the over voltages must be suppressed by adapting voltage clamping (v.c) device.

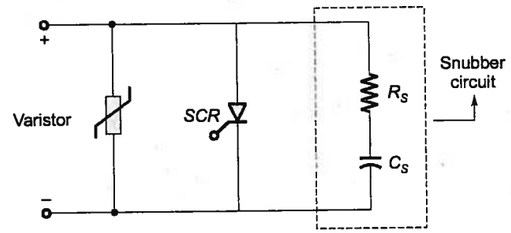


***Figure*-4.12**

- A voltage clamping (v.c) device is a non-linear resistor connected across SCR as shown in figure. The V.C. device has falling resistance characteristics with increasing voltage. Under normal conditions the device has a high resistance and draws only a small leakage current. When a voltage surge appears, the V.C. device operates in low resistance region and produces a short-circuit across SCR. After the surge is dissipated it returns to normal high resistance.

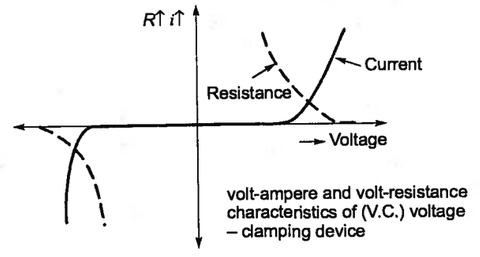


***Figure*-4.13**

Over Current Protection

If a SCR is subjected to over current due to faults, short circuits (or) surge currents, its junction temperature may exceed the rated value and the device may be damaged. There is a need for the over current protection of SCR.

(*i*) Fast acting current limiting fuse (FACLF)
(*ii*) Circuit breakers are used

Gate Protection

- Over voltages and over currents across the gate circuit can cause false triggering of the SCR.
- Protection against over voltages is achieved by connecting a zener diode *ZD* across the gate circuit.
- Protection against the over current is achieved by connecting a resistor 'R_2' in series with gate circuit.
- A capacitor and a resistor are also connected across gate to cathode to by pass the noise signals.

Circuit Components Showing The Thyristor Protection

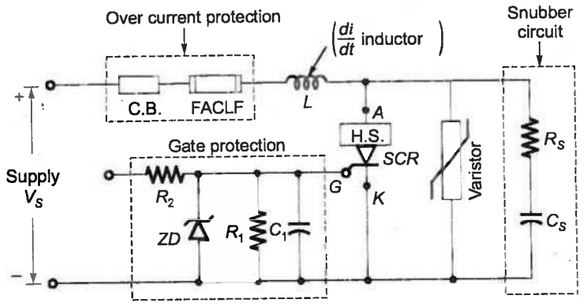


***Figure*-4.14**

Thermal Protection

If temperature increases, insulation is weakened, resulting in leakage currents which interference with the operation. Heat sinks which include aluminium discs are used along with ventilating ducts, increased surface area, coolants are used.

4.3 Structural Modification of the Device

1. Centre Gate Thyristor

In this type of thyristor the n^+ layer is surrounded arround the p-layer.

If injection of gate pulses (or) carriers formed multiconduction area. Due to multi cathode conduction area increase the (di/dt) rating of thyristor.

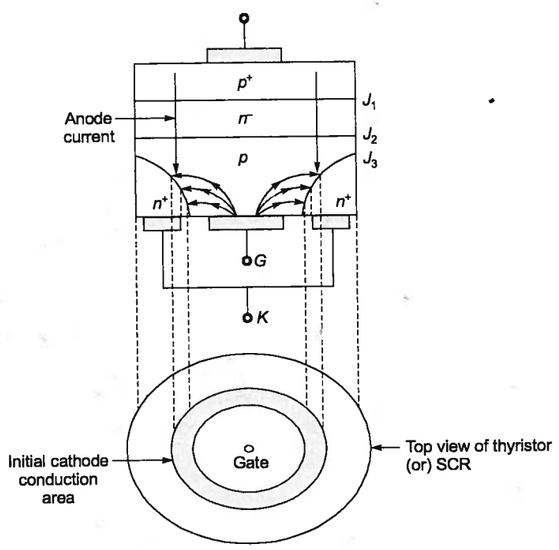


***Figure*-4.15**

2. Interdigation Method

In this method we are mixing the gate and cathode layers in large proportions. This increases the initial conduction area because more cathode surface exposed to the gate layer. Hence (di/dt) rating of SCR is improved to a large extent.

4.4 Heating and Cooling of SCR

- The rate of heat transfer (i.e.) current flow is constant.
- Thermal resistance is denoted by 'θ'. If power loss P_{av} in watts, causes the temperature of two points to be at T_1°C and T_2°C where $T_1 > T_2$, then thermal resistance is given by

$$\theta_{12} = \frac{T_1 - T_2}{P_{av}} \text{ [°C/W]}$$

- Various temperatures and thermal resistance are shown in the below figure.

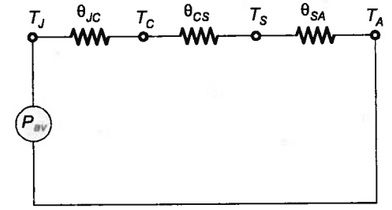


***Figure*-4.16**

- The thermal resistance between the junction temperature T_J and case temperature T_C is 'θ_{JC}'.
- The thermal resistance between the case temperature T_C and sink temperature T_S is 'θ_{CS}'.
- The thermal resistance between the sink temperature T_S and ambient temperature T_A is 'θ_{SA}'.
- P_{av} is the average rate of heat generated at a thyristor junction and it is electrical analogous to constant current source. Here,

$$P_{av} = \frac{T_J - T_C}{\theta_{JC}} = \frac{T_C - T_S}{\theta_{CS}} = \frac{T_S - T_A}{\theta_{SA}}$$

$$P_{av} = \frac{T_J - T_A}{\theta_{JA}}$$

where,

$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$ is the total thermal resistance between junction and ambient.

The difference in temperature between junction and ambient can be written in

$$T_J - T_A = P_{av}(\theta_{JA})$$

this shows that for maximum value of T_J, P_{av} can be increased by reducing 'θ_{JA}'. This means that by providing efficient cooling system to the SCR, the power dissipation capability of the device can be increased.

4.5 Series and Parallel Operation of SCR

For industrial applications, the demand for voltage and current rating is so high that a single SCR cannot fulfil such requirement.

In such cases SCR's are connected:

(*i*) in series in order to meet the high voltage demand.

(*ii*) in parallel for fullfilling the high current demand.

In series or parallel connected SCRs, it should be ensured that each SCR rating is fully utilized and the system operation is satisfactory.

NOTE

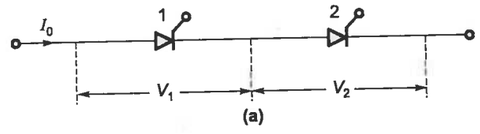
String efficiency is a term that is used for measuring the degree of utilization of SCRs in a string.

$$\text{String efficiency} = \frac{\text{Acting voltage/Current rating of the whole string}}{\text{(Individual voltage/Current rating of one SCR)(Number of SCRs in the string)}}$$

A measure of reliability of string is given by a factor called derating factor (DRF). It is defined as

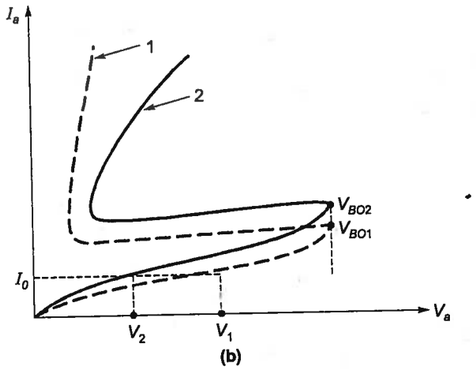
$$\boxed{\text{DRF} = 1 - \text{String efficiency}}$$

Series Operation



(a)

To connect SCR's in series their I-V characteristics should be as close as possible.



(b)

***Figure*-4.17 :** *(a) and (b)*

The string efficiency = $\dfrac{V_1 + V_2}{2 \times V_1}$

$$\boxed{\eta_s = \frac{V_1 + V_2}{2 \times V_1}}$$

- A more practical way of obtaining a reasonable uniform voltage distribution during steady state working of series connected SCRs is to connect the same value of shunt resistance R across each SCR. The shunt resistance 'R' is called the static equalizing circuit.

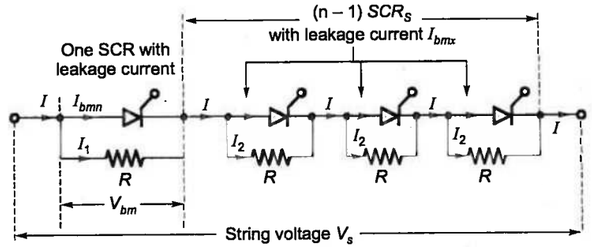


***Figure*-4.18 :** *Static voltage equlization for series connected string*

- Consider n thyristor connected in series as shown in figure. Let SCR1 has minimum leakage current I_{bmn}. SCR with lower leakage current blocks more voltage.
- Remaining $(n-1)$ SCRs have the same leakage current I_{bmx}.

$$I_{bmx} > I_{bmn}$$

Here V_{bm} is the maximum permissible blocking voltage as SCR1.

$$I = I_1 + I_{bmn} \quad ; \quad I = I_2 + I_{bmx}$$
$$I_1 = I - I_{bmn} \quad ; \quad I_2 = I - I_{bmx}$$

where, I = total string current

Voltage across SCR1 is $V_{bm} = I_1 R$

Voltage across $(n-1)$ SCRs = $(n-1)\, I_2 R$

For a string voltage (V_s), the voltage equation for the series circuit is

$$V_s = I_1 R + (n-1)\, I_2 R = V_{bm} + (n-1)\, R\,(I - I_{bmx})$$
$$= V_{bm} + (n-1)\, R\,(I_1 + I_{bmn} - I_{bmx})$$
$$= V_{bm} + (n-1)\, R\,[(I_1 - (I_{bmx} - I_{bmn})]$$
$$V_s = V_{bm} + (n-1)\, R I_1 - (n-1)\, R \Delta I_b \qquad [\because\ \Delta I_b = I_{bmx} - I_{bmn}]$$

As, $R I_1 = V_{bm}$

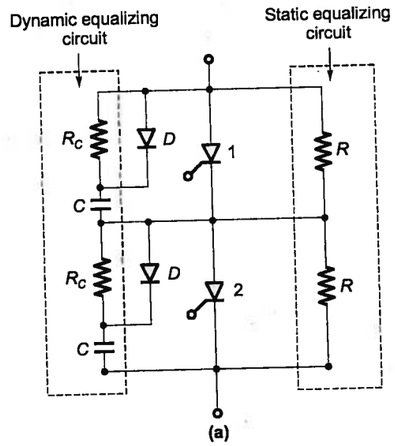
$$V_s = V_{bm} + (n-1)\, V_{bm} - (n-1)\, R \cdot \Delta I_b$$
$$V_s = n\, V_{bm} - (n-1)\, R \cdot \Delta I_b$$

$$\boxed{R_s = \frac{n V_{bm} - V_s}{(n-1) \cdot \Delta I_b}}\ [\Omega]$$

'R_s' is the static equalizing resistance.

Dynamic and Static Equalizing Circuit for Series Connected SCR's

- A simple resistor as shown in static voltage equalization cannot maintain equal voltage distribution under transient condition. The shunt capacitors play a dominant role in equalizing the voltage distribution across the series connected thyristors during turn-on and turn-off process.
- When any SCR in the forward blocking state, the capacitor connected across it get charged to a voltage existing across that SCR. When this SCR is turned-on, capacitor discharges heavy current through this SCR. For limiting this discharge current 'Damping Resistor R_C' is used in series with capacitor C.
- The Resistor R_C also damps out the high frequency oscillations that may arise due to series combination of R_C, shunt capacitor and circuit inductance.



NOTE: Combination of 'R_C' and 'C' is called Dynamic equalizing circuit.

- A diode D is also placed across 'R_C' when forward voltage appears, diode bypasses R_C during charging time of the capacitor C. This makes the capacitor more effective in voltage equilization and for limiting dv/dt across SCR. However, during capacitor discharge, R_C comes in to play for limiting the current.

Value of the Capacitance 'C' can be obtain as under

In series connected SCR's voltage unbalance during turn-off time is more predominant than it is during turn-on time, therefore choice of capacitor 'C' is based on the reverse recovery characteristics of SCR.

- SCR1 is assumed to be recovered first due to short reverse recovery time.
- During turn-off process, the source voltage V_s must reverse to aid to reverse recovery current.
- The transient voltage which each SCR must be able to with stand is 'V_{bm}'.
- Total voltage acting across the circuit consisting of V_s, thyristors n, 3, 2 and top 'C' as per KVL

$V_s + \frac{(n-1)\,\Delta Q}{C}$ and this must be supported by all SCRs stage together which is equal to $n \cdot V_{bm}$.

$\frac{\Delta Q}{C}$ is the voltage induced by ΔQ in the capacitor C.

So,
$$n V_{bm} = V_s + \frac{(n-1)\,\Delta Q}{C}$$

$$V_{bn} = \frac{1}{n}\left[V_s + \frac{(n-1)\,\Delta Q}{C}\right]$$

$$\boxed{C = \frac{(n-1)\cdot \Delta Q}{n \cdot V_{bm} - V_s}}\ [F]$$

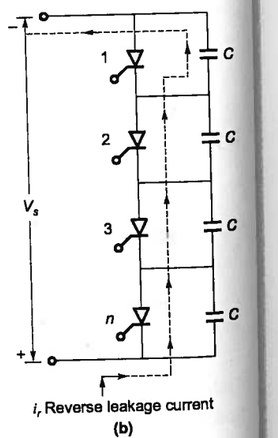


***Figure*-4.19** : *(a) and (b)*

Parallel Operation

When current required by the load is more than the rated current of a single thyristor, SCR's are connected in parallel in a string.

For equal sharing of currents, I-V characteristics of SCR's during forward conduction must be identical as far as possible.

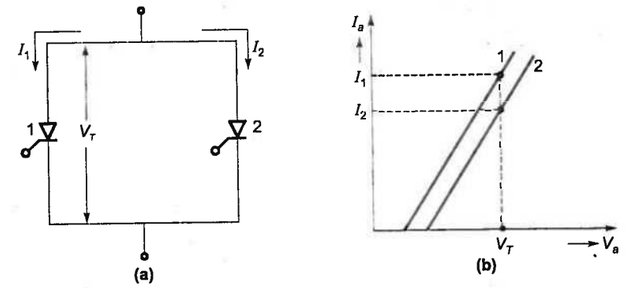


***Figure*-4.20**

***Example*-4.6** A thyristor string is formed by series and parallel connection of thyristors. The voltage and current ratings of the string are 11 kV, 4 kA respectively. The thyristor to be employed has voltage and current ratings of 1.7 kV, 1 kA. The string efficiency is 90% for both series and parallel combinations. If the maximum blocking current is 15 mA and maximum charge storage (Q_{max}) is 24 micro Coulombs (μC), calculate the value of resistance and capacitance of equalizer circuit.

Solution:

$$\text{Number of series branches} = \frac{N \text{ rating}}{n \times \text{rating of a } SCR} = \frac{11\text{kV}}{0.9 \times 1.7\,\text{kV}} = 7.19$$

So, 7 SCRs are not sufficient ⇒ 8 SCRs are required.

$$R = \frac{nV_b - V_s}{(n-1)\Delta I_b} = \frac{8 \times 1.7 - 11}{7 \times 15} = 24.76\ \text{k}\Omega$$

$$C = \frac{(n-1)\,Q_{max}}{nV_b - V_m} = \frac{(7)\,(24 \times 10^{-6})}{8 \times 1.7 - 11} = 64.6\ \text{nF}$$

The unequal current distribution and other operating problems are discussed below:

Simultaneous Turn-on

Consider 'n' parallel connected SCRs. For satisfactory operation of these SCRs, they should get turned-on at the same moment.

Same Temperature Rise

When SCRs are to be operated in parallel, it should be ensured that they operate at the same temperature. This can be achieved by mounting the parallel unit on one common heat sink.

Symmetrical Arrangement

When SCRs are arranged unsymmetrically as shown in the figure (a). The middle conductor will have more inductance because of more flux linkages from two nearby conductors. As a consequence, less current flows through the middle SCR as compared to outer two SCR's. This unequal distribution can be avoided by mounting the SCR's symmetrically on the heat sink as shown in figure (b).

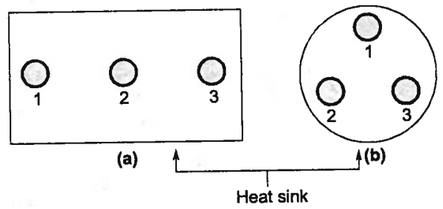


***Figure*-4.21**

Uniform Current Sharing

Current sharing in parallel connected SCRs can be made uniform by connecting a suitable external resistance in series with each SCR.

Where as R_{T1}, R_{T2}, R_{T3}.....

R_{Tn} are Dynamic resistance of SCRs.

R_1, R_2, R_3...R_n are external resistances.

The values of R_1, R_2, R_3...R_n are choosen such that

$$R_{T1} + R_1 = R_{T2} + R_2$$
$$= R_{T3} + R_3 = \ldots = R_{Tn} + R_n$$

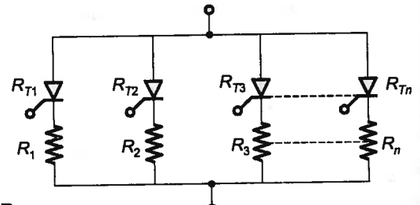


***Figure*-4.22**

Mid-point Reactor

In ac circuit, current distribution can be made more uniform by the magnetic coupling of the parallel patns. If currents I_1 and I_2 are unequal, say $I_1 > I_2$, then resultant flux linkages are not zero. These flux linkages induce emf's in L_1 and L_2.

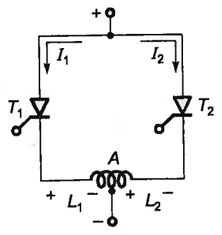


***Figure*-4.23**

The reactor is arranged to completely balance the SCRs.

***Example* - 4.7** **Point out the differences between latching current and hold current for the thyristor. What do you understand by string effciency related to thyristors? For a thyristor, maximum junction temperature is 125°C. The thermal resistances for thyristor-sink combination are θ_{jc} = 0.16 and θ_{cs} = 0.08° C/W. For a heat sink temperature of 70°C compute the total average power loss in the thyristor sink combination. In case the heat sink is brought down to 60°C by forced cooling, find the percentage increase in the device rating.**

Solution:

Latching current: The minimum value of anode current which the thyristor must attain during turn-on process to maintain conduction even after the removal of gate pulse is called latching current.

(*i*) **Holding current:** It is defined as the minimum value of anode current below which it must fall for turning off the thyristor.

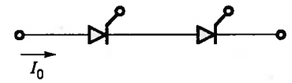
In general latching current > holding current.

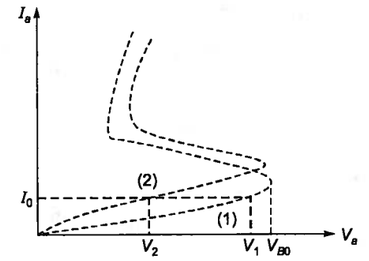
String efficiency is a term that is used for measuring the degree of utilization of SCR in a string.

(*ii*) String efficiency = $\dfrac{\text{Actual voltage (series) or current (parallel) rating of the whole string}}{\text{No. of SCR's in the string} \times \text{voltage or current rating of each SCR}}$

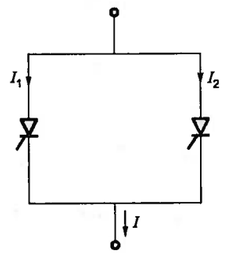
Series operation of SCR's

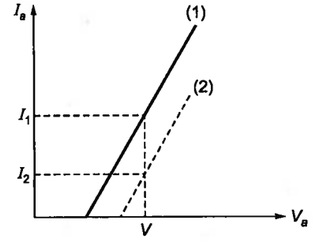
$$\eta_s = \frac{V_1 + V_2}{2\,V_1}$$





Parallel Operation of SCR's



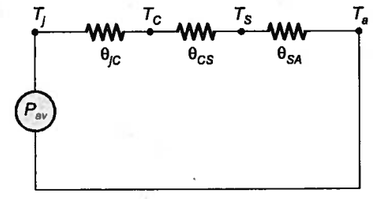


String efficiency = $\dfrac{I_1 + I_2}{2\,I_1}$

(*iii*) From the equivalent circuit,

$$T_j = T_s + P_{av}(\theta_{jC} + \theta_{CS})$$

$$\therefore \quad P_{av1} = \frac{125 - 70}{0.16 + 0.08} = 229.17 \text{ W}$$



Thus total power loss in the thyristor-sink combination is 229.17 ω with improved cooling.

$$P_{av2} = \frac{125 - 60}{0.24} = 270.83 \text{ W}$$

Thyristor rating is proportional to the square root of average power loss.

$$\% \text{ increase in thyristor rating} = \frac{\sqrt{270.83} - \sqrt{229.17}}{\sqrt{229.17}} \times 100 = 8.71$$

4.6 Firing Circuits for Thyristors

The gate control circuit is called firing (or) triggering circuit.

A firing circuit should fulfil the following two functions:

1. If power circuit has more than one SCR, the firing circuit should produce gating pulses for each SCR at the desired instant for proper operation of the power circuit. These pulses must be periodic in nature and the sequence of firing must correspond with the type of thyristorised power controller.
2. The control signal generated by a firing circuit may not be able to turn on an SCR. It is therefore common to feed the voltage pulses to a driver circuit and then to gate cathode circuit. A driver circuit consists of a pulse amplifier and a pulse transformer.

1. Resistance Firing Circuits

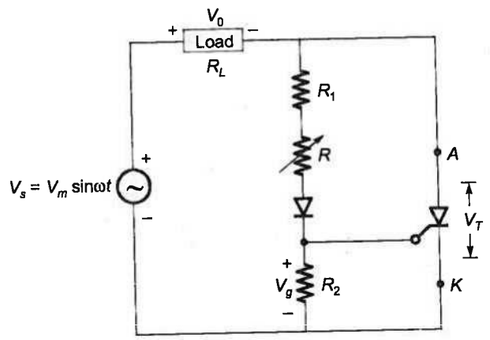


Figure-4.24

The maximum firing angle is limited to 90°. i.e. firing angle (α) is control from 0 to 90°, great dependence on temperature and difference in performance between individual SCRs.

- R is variable resistance, R_2 is stabilizing resistance. Incase R is zero, gate current may flow from source through load, R_1, D and gate to cathode.
- This current should not exceed maximum permissible gate current I_{gmax}

  $I_{g_{min}} \le I_g \le I_{g_{max}}$ and $V_{g_{min}} \le V_g \le V_{g_{max}}$
- Resistance R_1 is used to limit the gate current to a safe value as R is varied.
- For worst situation maximum possible gate voltage

$$= \frac{V_m}{R_1 + R_2} \cdot R_2 \le V_{g_{max}}$$

i.e.
$$R_2 \le \frac{V_{g_{max}} \cdot R_1}{V_m - V_{g_{max}}}$$

- By varing resistance 'R', to vary the firing angle 'α'.
- Diode 'D' is used to avoid the negative gate pulse V_{gt} is gate turn-on voltage. It is voltage at which SCR will be turn-on i.e. $V_g = V_{gt}$; SCR → ON (at $\omega t = \alpha$)

$$V_g = \left(\frac{V_s}{R_1 + R + R_2}\right) \cdot R_2 = \left(\frac{V_m \sin\omega t}{R_1 + R + R_2}\right) \cdot R_2$$

$$V_g = V_{g_{max}} \sin\omega t$$

where, V_{gmax} (peak value of gate voltage) $= \frac{V_m \cdot R_2}{R_1 + R + R_2}$

Resistance Capacitance (RC) Firing Circuit

The limited range of firing angle control of resistance firing circuit can be overcome by RC firing circuit.

1-ϕ Full Wave Rectifier

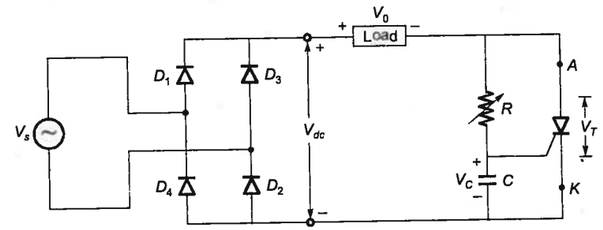


Figure-4.25

Initial voltage from which the capacitor C charges is almost zero. The capacitor C is set to this low positive voltage by clamping action of SCR gate. When capacitor 'C' charges to a voltage equal to V_{gt}, SCR is triggered and rectified voltage 'V_d' appears across load.

$$V_s \ge V_c + R I_{gt} \quad \text{and} \quad V_c = V_{gt}$$

$$R \le \frac{V_s - V_{gt}}{I_{gt}}$$

As varing the vallue of 'R'. α also varies.

Range of firing angle is from 0 to 180° (in ideal case)

In ideal case, $V_{gt} = 0^+$ i.e. $\alpha_{max} = 180°$

But if $V_{gt} = 0$ then SCR behaves as a diode, so $V_{gt} \ne 0$

In practicle $V_{gt} = (1 - 2)$ V

So, $\alpha \rightarrow (5° - 7°)$ to $(165° - 175°)$

NOTE: *R* and *RC* triggering circuit cannot be used for automatic or feedback control systems.

$$V_g = V_{g_{max}} \sin\omega t \qquad \text{...valid only when SCR is off.}$$

$$V_{g_{max}} \sin\omega t = V_{gt}$$

At $\omega t = \alpha$, $\quad V_{g_{max}} \sin\alpha = V_{gt}$

$$\alpha = \sin^{-1}\left(\frac{V_{gt}}{V_{g_{max}}}\right) = \sin^{-1}\left[V_{gt} \cdot \frac{(R_1 + R + R_2)}{V_m \cdot R_2}\right]$$

As V_{gt}, R_1, R_2 and V_m is constant or fixed $\boxed{\alpha \propto \sin^{-1}(R)}$ or $\boxed{\alpha \propto R}$

i.e. as R is increased from small value (i.e. small α) firing angle increases.

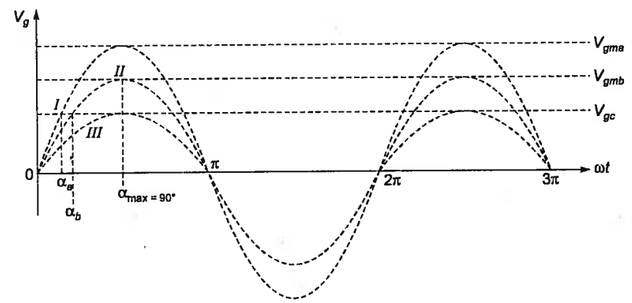


***Figure*-4.26**

Case-I:

Let, $R = R_a$ i.e. $(\alpha = \alpha_a)$

$$V_{gma} = \frac{V_m R_2}{R_1 + R_a + R_2} \Rightarrow V_g = V_{gma} \sin\omega t$$

Case-II:

Let, $R = R_b > R_a$ i.e. $(\alpha = \alpha_b)$

$$V_{gmb} < V_{gma}$$

Case-III:

Let, $R = R_C > R_b$ i.e. $(\alpha = \alpha_c)$

$$V_{gmc} < V_{gmb}$$

UJT (Un-junction Transistor)

In R and RC triggering circuit, the power dissipation in the gate circuit is severe.

At the same time R and RC triggering circuit cannot be used for automatic or feedback control systems. So that, to overcome from these difficulties, UJT triggering circuit is used. A UJT is made up of an n-type silicon base to which p-type is embedded. The n-type is lightly doped whereas p-type is heavily doped. An UJT has three terminal E, B_1 and B_2. Between bases B_1 and B_2, the uni-junction behaves like an ordinary resistance.

R_{B_1} and R_{B_2} are the internal resistance.

B_1, B_2 → Base terminal

E → Emitter terminal

Equivalent Circuit of UJT

$$V_{RB_1} = \frac{V_{BB}}{R_{B_1} + R_{B_2}} \cdot R_{B_1} = \eta V_{BB}$$

$$\boxed{\eta = \frac{R_{B_1}}{R_{B_1} + R_{B_2}}}$$

where η is intrinsic stand off ratio (0.51 – 0.82).

$$V_E = V_{R_{B_1}} + V_D \quad \text{or} \quad \boxed{V_E = V_P}$$

...(Condition to turn-on UJT)

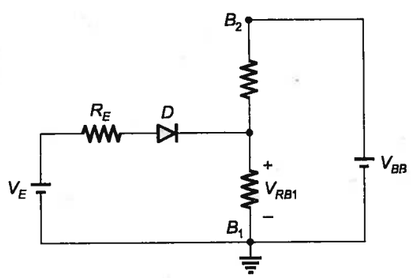


***Figure*-4.27**

Where, V_P(Peak point voltage) = $\eta V_{BB} + V_D$

- When UJT switching from OFF to ON the R_{B_1} change from several kΩ to few Ω.
- i.e. UJT exhibits negative resistance behaviour.
- V_E starts reducing when UJT becomes ON and V_E reduce upto V_V(Valley voltage).

The current is given by V_V / R_{B_1}. Valley point current also called holding current, keeps UJT on.

When emitter current I_e falls below I_V, UJT turn-off.

$$I_e = \frac{V_E - V_D}{R_{B_1} + R_E}$$

UJT Working as Relaxation Oscillator

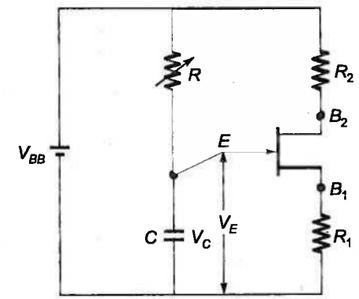


***Figure*-4.28**

Initially capacitor 'C' charge by V_{BB} through R at this time emitter diode is off.

When capacitor voltage 'V_C' reach V_E then emitter diode is ON and capacitor discharge through R_{B_1}

$$V_E = V_{R_{B_1}} + V_D$$

Discharging time of capacitor 'C' is very small in comparison to charging time of capacitor because discharging time constant ($\tau_2 = R_1 C$) is much smaller than τ_1.

$$V_C = V_e = V_{BB}(1 - e^{-t/RC}) = \eta V_{BB}$$

$$(1 - e^{-T/RC})\, V_{BB} = \eta\, V_{BB} \qquad \text{(Consider } V_D = V_v = 0\text{)}$$

$$e^{T/RC} = \frac{1}{1-\eta}$$

$$T = RC\, ln \frac{1}{1-\eta} \quad \text{...(Time period of UJT)}$$

or,

$$F = \frac{1}{RC\, ln\left(\frac{1}{1-\eta}\right)} \quad \text{...(Frequency of oscillator)}$$

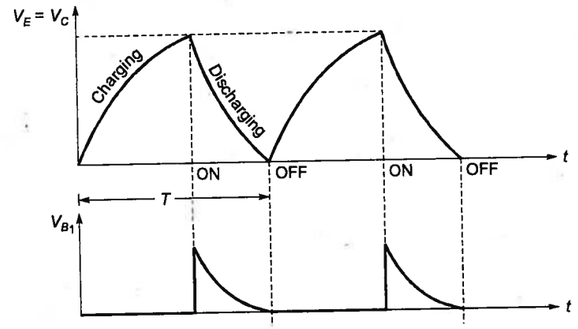


***Figure*-4.29**

$$\alpha_1 \text{ (Firing angle)} = \omega T = \omega RC\, ln \frac{1}{1-\eta}$$

Synchronized UJT Triggering Circuit

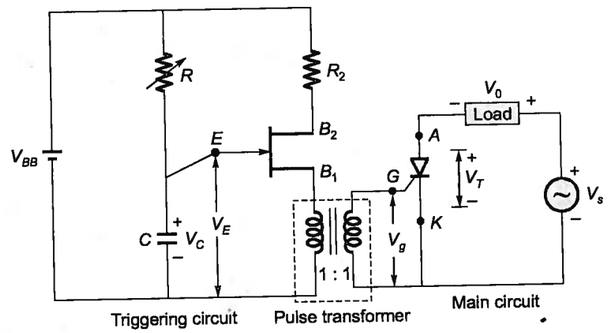


***Figure*-4.30**

- Here firing circuit and main circuit both having different reference voltages so firing angle is not matching with the time, so it required common reference voltage for both circuit.
- To match the gate pulse required to main circuit with the gate pulse produced by gate firing or triggering circuit we must use same power supply in the main circuit as well as firing circuit.
  i.e. we must tune the timing of main circuit power supply with firing circuit. This is known as synchronization.

Pulse Transformer

The function of pulse transformer is to isolate the low voltage gate cathode circuit from the high voltage anode cathode circuit and also triggering of two or more devices from the same trigger source.

- The turns ratio from primary to secondary is 2 : 1 : 1 or 1 : 1 : 1.

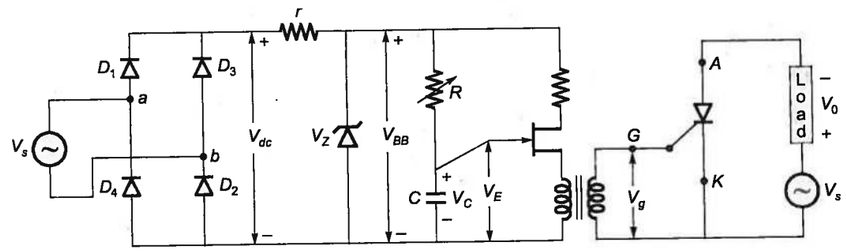


***Figure*-4.31**

Synchronized UJT Triggering Circuit

Here '*r*' is used to limiting the current to protect the zener diode during short circuit.

Zener diode is used for maintain or providing the smooth dc voltage to firing circuits by pulsating dc. i.e. zener diode used to clip the peak of pulsating dc and made a constant or little pulsating dc to firing circuit.

- Useful gate pulse is at α, $(2\pi + \alpha)$.....
- As the first pulse will be able to turn-on the SCR, second pulse in each cycle is redundant.

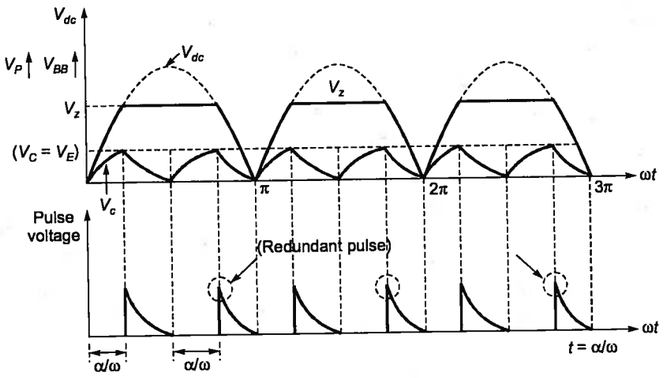


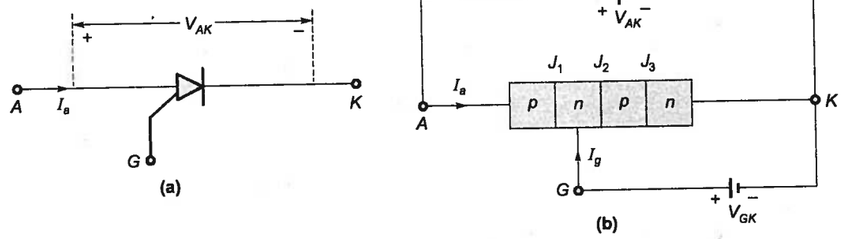
***Figure*-4.32**

4.7 Other Members of Thyristor Family

1. PUT (Programmable Uni-junction Transistor)
2. SUS (Silicon Unilateral Switch)
3. SCS (Silicon Controlled Switch)
4. LASCR (Light Activated Thyristor)
5. SITHs (Static Induction Thyristor)
6. The DIAC (Bidirectional Thyristor Diode)
7. TRIAC
8. ASCR (Asymmetrical Thyristor)
9. RCT (Reverse Conducting Thyristor)
10. GTO (Gate Turn-off Thyristor)
11. MOSFET Controlled Thyristor (MCT)
12. Field Controlled Thyristor (FCT)

1. PUT (Programmable Unijunction Transistor)

It is a *pnpn* device like an SCR. But the major difference is that gate is connected to n-type material near the anode as shown in figure.



- PUT is mainly used in Time delay, Logic and SCR Triggering circuits.
- It's largest rating is about 200 V and 1 A.
- I-V characteristics of a PUT are

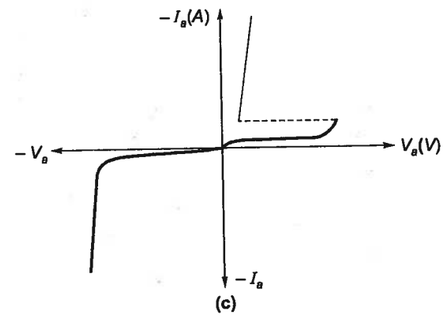
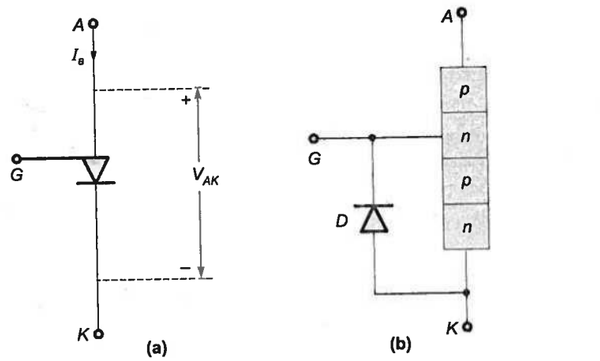


***Figure*-4.33 :** *(a), (b) and (c)*

Gate is always biased positive with respect to cathode.

2. SUS (Silicon Unilateral Switch)

A SUS is similar to a PUT but with an inbuilt low voltage avalanche diode between gate and cathode as shown in figure.



- Because of presence of diode (*D*), SUS turns-on for a fixed anode to cathode voltage.
- Its ratings are about 20 V and 0.5 A.
- I-V characteristics of SUS are

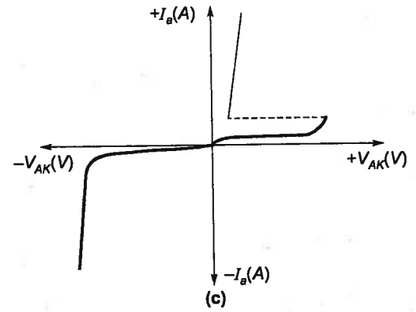
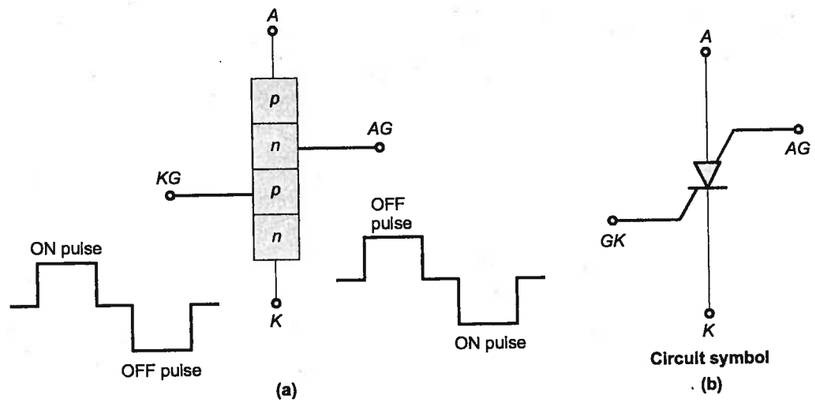


***Figure*-4.34 :** *(a), (b) and (c)*

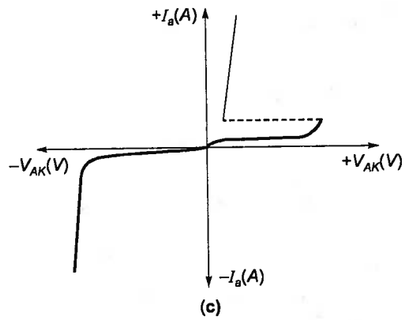
3. SCS (Silicon Controlled Switch)

- SCS is a tetrode i.e. four electrode thyristor. It has two gates, one anode gate (*AG*) like a PUT and controller cathode gate (*KG*) like an SCR.
- SCS is a four layer, four terminal *pnpn* device; with anode *A*, cathode *K*, anode gate *AG* and cathode gate *KG*.

NOTE: SCS can be turned-on by either gate.



- Anode gate is given negative pulse to turn-on. *KG* is given positive pulse to turn-on. Ratings of SCS are 100 V and 200 mA.



(c)

***Figure*-4.35 :** *(a), (b) and (c)*

4. LASCR (Light Activated Thyristor)

- Light activated SCR, it is turned-on by throwing a pulse of light on the silicon wafer of thyristor.
- If the intensity of light exceeds a certain value, excess electron hole pairs are generated due to radiation and forward-biased thyristor gets turned-on.
- The rating of LASCR are upto 6 kV and 3.5 kA with ON state voltage drop of 2 V and with light triggering requirement of 5 mW.

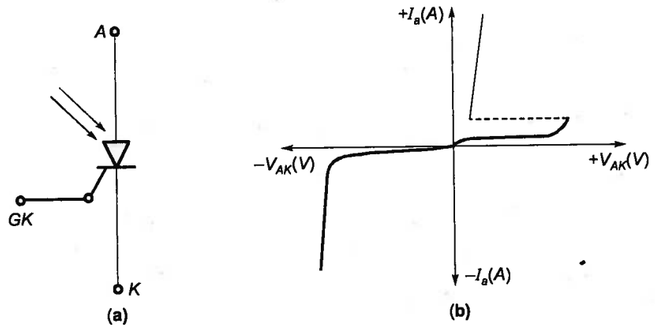


***Figure*-4.36 :** *(a) Circuit symbol (b) I-V characteristics of LASCR*

5. SITHs (Static Induction Thyristor)

- The SITH is also known as Field Controlled Diode (*FCD*).
- The ratings of the device are $V = 2500$ V and $I = 500$ A.

Turn-on of SITHs

- A SITH is normally turned-on by applying a positive gate voltage with respect to cathode. Its the gate cathode *PN* diode turns-on and injects electrons from the N^+ cathode region into the base region between the P^+ gate and N^+ cathode, and into the channel.
- The positive gate voltage reduces the potential barrier in the channel, which gradually becomes conductive. When electrons reach the junction J_1, the P^+ anode begins to inject holes into the base, providing the base current of transistor Q_2. As the base current increases, J_2 is eventually forward biased. The device is then fully turned-on.

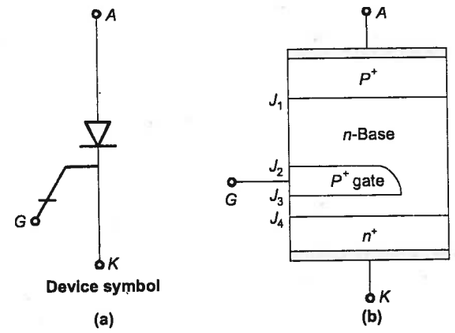


***Figure*-4.37**

Turn-off

An SITH is normally turned-off by applying a negative voltage with respect to the cathode. If a sufficiently negative voltage is applied to the gate, a depletion layer forms around P^+ gate, and eventually the depletion layer fully cuts-off the channel.

6. The DIAC (Bidirectional Thyristor Diode)

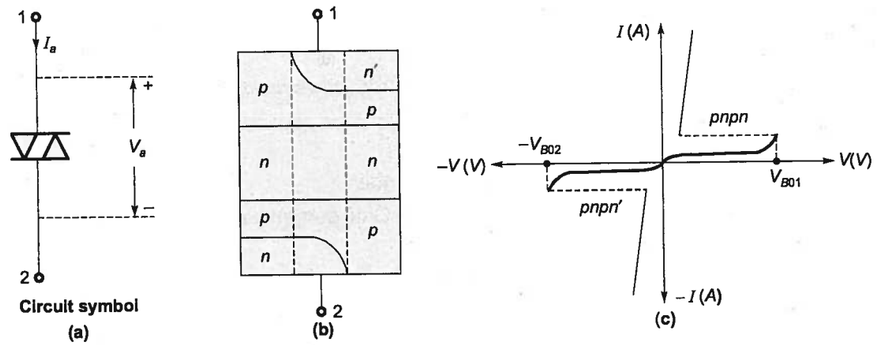


***Figure*-4.38**

- If voltage V_{12}, with terminal 1 positive with respect to terminal 2, exceeds breakover voltage V_{B01}, then structure *pnpn* conducts.
- In case terminals 2 is positive with respect to terminal 1 and when V_{21} exceeds break over voltage V_{B02}, structure *pnpn′* conducts.
- I-V characteristics of a DIAC.

NOTE: The term DIAC is obtained from capital letters, Diode that can work on AC. A diac is some times called a gate less TRIAC

7. TRIAC

A TRIAC is a bidirectional thyristor with three terminals. It is used extensively for the control of power in ac circuits.

Triac is the word derived by combining the capital letters from the word TRIode and AC.

Its three terminals are usually designated as MT_1 (Main terminal 1), MT_2 and the gate.

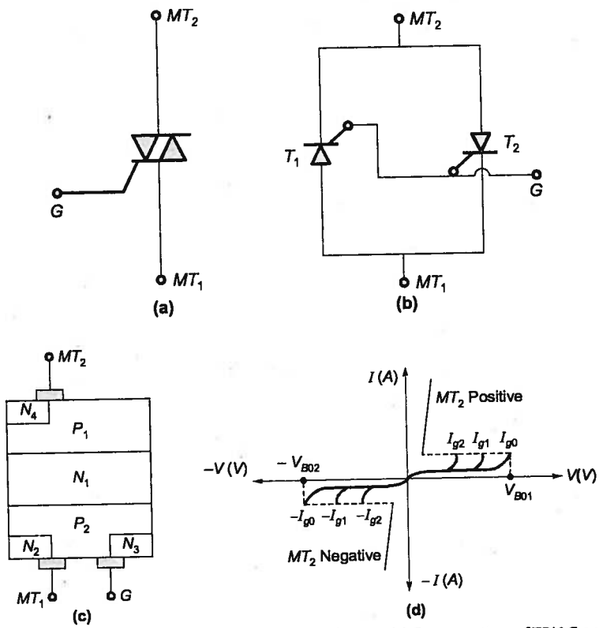


***Figure*-4.39 :** *(a) TRIAC symbol (b) Equivalent of TRIAC (c) Construction of TRIAC and (d)*

The Triac can however be turned on in each half cycle of the applied voltage by applying a positive (or) negative voltage to the gate with respect to terminal MT_1.

The turn-on process of a triac can be explained as under:

MT_2 positive and Gate current is also positive: When Gate current has injected sufficient charge into P_2 layer, reverse biased junction N_1P_2 breaks down.

As a result, triac starts conducting through P_1, N_1, P_2, N_2 layers.

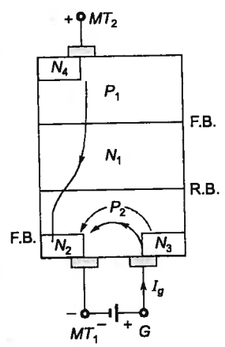


***Figure*-4.40**

MT_2 is positive but Gate is negative: Gate current flows through P_2 N_3 junction.

Reverse biased junction N_1P_2 is forward biased by injecting sufficient charge into P_2.

As a result Triac starts conducting through $P_1N_1P_2N_3$.

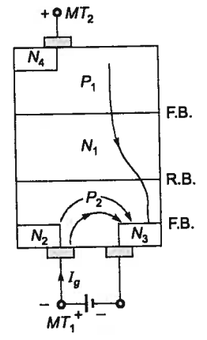


***Figure*-4.41**

MT_2 is negative but Gate current is positive: Gate current I_g forward biases P_2N_2 junction. Layer N_2 injects electrons into P_2 layer. As a reset, reverse biased junction N_1P_1 breaks down.

The path $P_2N_1P_1N_4$ is completely turned-on.

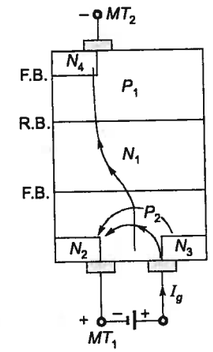


***Figure*-4.42**

Both MT_2 and Gate current are negative:

The gate current Ig flows from P_2 to N_3.

Reverse biased junction N_1P_1 is broken, and finally, the structure $P_2N_1P_1N_4$.

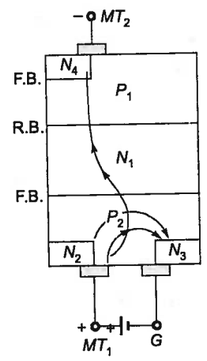
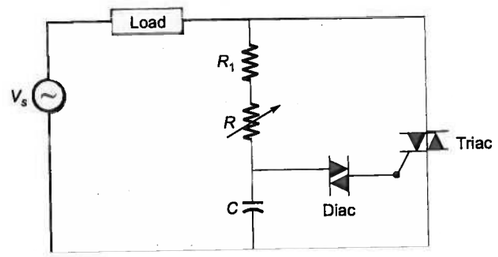


***Figure*-4.43**

Example - 4.8 A triac-diac used for a stepless fan regulator.

Solution:

This is the circuit diagram of the simplest fan regulator. The circuit is based on the principle of power control using a Triac. The circuit works by varying the firing angle of the Triac. The firing angle can be varied by varying the resistance R. By varying the value of R, the firing angle of Triac changes. This directly varies the load power, since load is driven by Triac. The firing pulses are given to the gate of Triac using Diac.



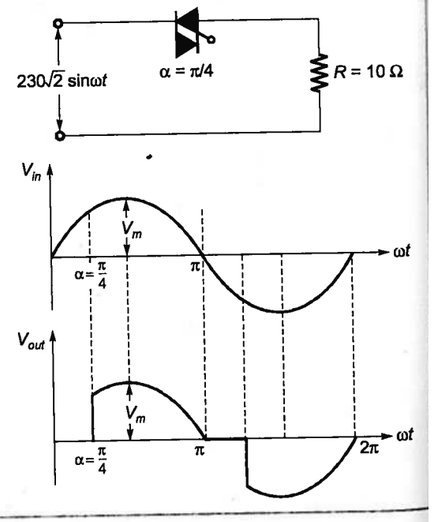
Example - 4.9 The Triac can be used in

(a) inverter (b) rectifier
(c) multiquadrant chopper (d) ac voltage regulator

Solution: (d)

Example - 4.10 The triac circuit shown in figure controls the ac output power to the resistive load. The peak power dissipation in the load is

(a) 3968 W (b) 5290 W
(c) 7935 W (d) 10580 W



Solution: (d)

Let V_m is the peak value of input voltage

$$V_m = 230\sqrt{2}\,\text{V}$$

As firing angle = $\alpha = \frac{\pi}{4}$, so peak voltage across resistance load is also V_m.

Peak power dissipation in the load,

$$P = \frac{V_m^2}{R}$$

$$= \frac{\left(230\sqrt{2}\right)^2}{10} = 10580\ \text{W}$$

8. ASCR (Asymmetrical Thyristor)

- An asymmetrical thyristor, is specially fabricated to have limited reverse voltage capability.
- This permits a reduction in turn-on, turn-off time and on state voltage drop in ASCR.
- Fast turn-off ASCRs minimize the size, weight and cost of commutating components and permit high frequency operation (20 kHz or more) with improved efficiency.
- A typical ASCR may have reverse blocking capability of 20 to 30 V and forward blocking voltage of 400 V to 2000 V.

9. Reverse Conducting Thyristors (RCT)

- It may be consider as a thyristor with a built in antiparallel diode.
- This construction reduces to zero the reverse blocking capability of RCT.
- RCTs with 2000 V and 500 A rating are available.

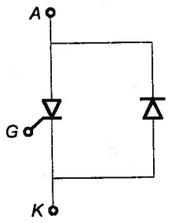


Figure-4.44

10. GTO (Gate Turn-off Thyristor)

- A GTO is a more versatile power semiconductor device. It is like a conventional thyristor but with added features in it.
- A GTO can be easily turned-off by a negative gate pulse of appropriate amplitude. Thus a GTO is a device that can be turned-on by a positive gate current and turned-off by a negative gate current at its gate cathode terminals.
- Self turn-off capability of GTO makes it the most suitable device for inverter and chopper applications.

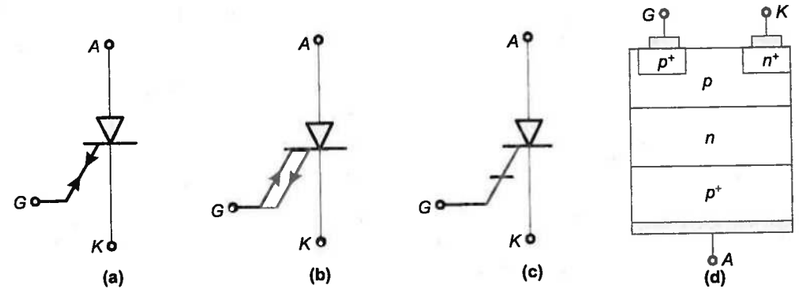


Figure-4.45 : *(a) Circuit symbols, (b), (c) and (d)*

- The four layers of GTO have different doping levels indicated by $p^+np^+n^+$.
- Transistor Q_1 is $p^+\,np^+$ type and Q_2 is $np^+\,n^+$. Emitter of Q_1 as anode and Emitter of Q_2 as cathode.

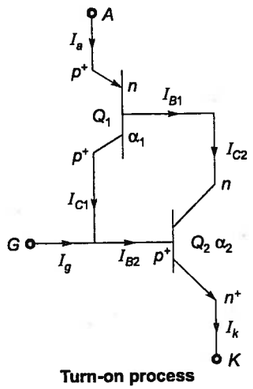
Turn-on Process

- A GTO is turned-on by applying a positive gate current I_g in the direction shown.
- Current gains α_1 and α_2 begins to rise and when $\alpha_1 + \alpha_2 = 1$, saturation level is reached and GTO is turned-on.

Turn-off Process

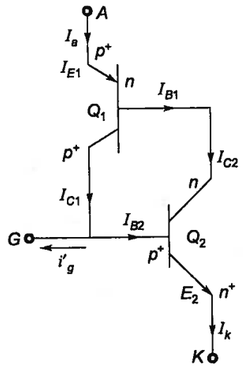
- For initiating the turn-off processor Q_2 must be brought out of saturation.
- The gate current I'_g is given in opposite side.

So when negative gate current I'_g flows between gate-cathode terminals. Net gate current is reversed and excess carriers are drawn from base p^+ region of Q_2 and collector current I_{C1} of Q_1 is diverted into the external gate circuit. This removes base drive of transistor Q_2. This further removes base current I_{B1} of transistor Q_1 and the GTO is eventually turned-off.



Turn-on process

Figure-4.46



Turn-off process

Figure-4.47

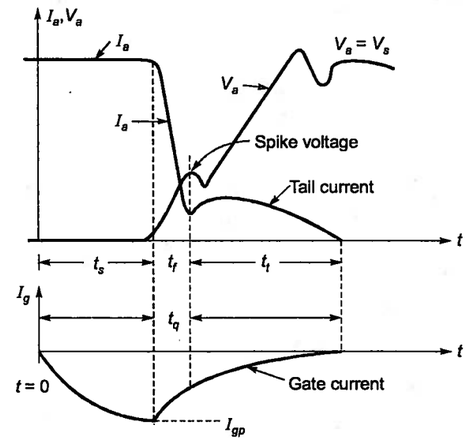
Example - 4.11 **Describe the turn-off process in a GTO with relevant voltage and current waveforms. Enumerate the advantages and disadvantages of a GTO as compared to a conventional thyristor.**

Solution:

Before the initiation of turn-off process, a GTO carries a steady current I_a. This figure shows a typical turn-off dynamic characteristic for a GTO. The total turn off time t_q is subdivided into three different periods ; namely the storage period (t_s), the fall period (t_f) and the tail period (t_t). In other words,

$$t_q = t_s + t_f + t_t$$

Initiation of turn-off process starts as soon as negative gate current begins to flow after $t = 0$. The rate of rise of this gate current depends upon the gate circuit inductance and the gate voltage applied. During the storage period, anode current I_a and anode voltage (equal to on-state voltage drop) remain constant. Termination of the storage period is indicated by a fall in I_a and rise in V_a.



During t_s, excess charges, i.e. holes in p-base are removed by negative gate current and the centre junction comes out of saturation. In other words, during storage time t_s, the negative gate current rises to a particular value and prepares the GTO for turning-off (or commutation) by flushing out of the stored carriers. After t_s, anode current begins to fall rapidly and anode voltage starts rising. As shown in figure, the anode current falls to a certain value and then abruptly changes its rate of fall. Interval during which anode current falls rapidly is the fall time t_f, figure and is of the order of 1 μsec [4]. The fall period t_t is measured from the instant gate current is maximum negative to the instant anode current falls to its tail current.

At the time $t = t_s + t_f$, there is a spike in voltage due to abrupt current change. After t_f, anode current I_a and anode voltage V_a keep moving towards their turn-off values for a time t_t called tail time. After t_t, anode current reaches zero value.

A GTO has the following disadvantage as compared to a conventional thyristor:

1. Magnitude of latching and holding currents is more in a GTO.
2. On state voltage drop and the associated loss is more in a GTO.
3. Due to the multicathode structure of GTO, triggering gate current is higher than that required for a conventional SCR.
4. Gate drive circuit losses are more
5. Its reverse-voltage blocking capability is less than its forward-voltage blocking capability. But this is no disadvantage so far as inverter circuits are concerned.

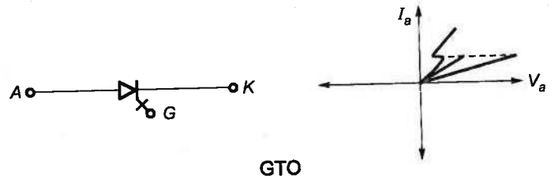
Inspite of all these demerits, GTO has the following advantages over an SCR:

1. GTO has faster switching speed.
2. Its surge current capability is comparable with an-SCR.
3. It has more di/dt rating at turn-on.
4. GTO circuit configuration has lower size and weight as compared to SCR circuit unit.
5. GTO unit has higher efficiency because an increase gate-drive power loss and on-state loss is more than compensated by the elimination of forced commutation losses.
6. GTO unit has reduced acoustical electromagnetic noise due to elimination of commutation chokes.

Example - 4.12 What is a GTO? Discuss its advantages over a normal thyristor. Discuss the advantage of a GTO over bipolar transistor in low power applications.

Solution:

GTO is pnpn device, can be turned on like an ordinary thyristor by a pulse of positive gate current, but it can be turned off easily by a negative gate pulse of appropriate amplitude.



GTO

1. GTO has faster switching speed.
2. Its surge current capability is comparable with an SCR.
3. It has more di/dt rating at turn-on.
4. GTO unit has higher efficiency due to the elimination of forced commutation losses.
5. GTO has reduced acoustical and electromagnetic noise due to elimination of commutation chokes.
6. GTO circuit configuration has lower size and weight as compared to thyristor circuit unit.
   (*i*) In BJT switching, lateral current flow is the basic limiting factor in BJT performance. It cuases lateral voltage drop which leads to emitter current crowding, which causes decrease in current gain. Excessive curernt crowding causes second breakdown and destruction of the device.
   (*ii*) Turning off of BJT should be done in a controlled manner of negative base current to avoid excessive stored charge which may cause long turn off time and large power dissipation. These problems are avoided in a GTO in low power applications.

Example - 4.13 Compare GTO thyristor with conventional thyristor and give merits and demerits. Why is a GTO thyristor preferred over SCR in chopper and inverter circuits?

Solution:

Disadvantage of GTO compared to conventional thyristor:

1. Magnitude of latching and holding currents is more in a GTO.
2. On state voltage drop and the associated loss is more in a GTO.
3. Due to multi cathode structure of GTO, Gate current is higher.
4. GTO has its reverse blocking capability less than its forward voltage blocking capability.
5. Gate drive circuit losses are more.

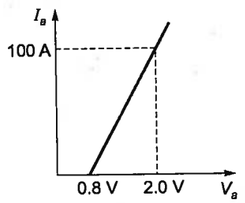
Advantage of GTO over conventional thyristor:

1. GTO has faster switching speed.
2. Its surge current capability is comparable with an SCR
3. It has more di/dt rating at turn-on.
4. Its circuit configuration has lower size and weight.
5. It has higher efficiency due to the elimination of forced commutation losses.
6. GTO unit has reduced electromagnetic noise due to elimination of commutation chokes.

Due to its faster switching speed and its elimination of forced commutation losses, mainly we use it in inverter and chopper circuits.

Example - 4.14 During forward conduction, a thyristor has static I-V characteristic a shown by a straight line in figure. Find the average power loss in the thyristor and its rms current rating for the following load conditions:

(*i*) A constant current of 80 A for one-half cycle.
(*ii*) A constant current of 80 A for one-third cycle.
(*iii*) A half-sine wave of peak value 80 A.



Solution:

It is seen from figure that for any current i_a, the voltage drop across thyristor is

$$v_T = 0.8 + \frac{2.0 - 0.8}{100} \times i_a = 0.8 + 0.012 i_a$$

(*i*) Constant current of 80 A for one-half cycle. For i_a = 80 A, the voltage drop across thyristor is $v_T = 0.8 + 0.012 \times 80 = 1.76$ V. The average on-state power loss in thyristor is

$$P_{av} = \frac{1}{T}\int_0^{T/2} v_T \cdot i_a \cdot dt = \frac{1}{T}\int_0^{T/2} 1.76 \times 80\, dt = \frac{1.76 \times 80 \times T}{2T} = 70.4 \text{ W}$$

Waveform of i_a gives the rms current rating of thyristor as

$$\sqrt{\frac{80^2 \times T}{2T}} = 56.568 \text{ A}$$

(*ii*) Here, $v_T = 0.8 + 0.012 \times 30 = 1.16$ V

$\therefore$ $$P_{av} = \frac{1.16 \times 30 \times T}{3T} = 11.6 \text{ W}$$

$$\text{Rms current rating} = 30 \times \frac{1}{\sqrt{3}} = 17.321 \text{ A}$$

(*iii*) Half-sine wave of peak value of 80 A,

$$i_a = 80 \sin\omega t$$

$\therefore$ $$v_T = 0.8 + 0.012 \times 80 \sin\omega t = 0.8 + 0.96 \sin\omega t$$

From the waveforms for i_a and v_T shown in figure, the average on-state power loss is given by

$$P_{av} = \frac{1}{2\pi}\int_0^{\pi} (0.8 + 0.96 \sin\omega t)\,(80 \sin\omega t)\, d(\omega t)$$

$$= \frac{1}{2\pi}\int_0^{\pi} 64 \sin\omega t \cdot d(\omega t) + \frac{1}{2\pi}\int_0^{\pi} 76.8 \sin^2\omega t \cdot d(\omega t)$$

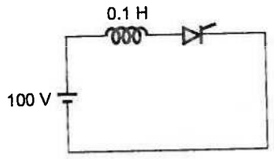
$$= \frac{1}{2\pi} \times 64 \left| -\cos\omega t \right|_0^{\pi} + \frac{76.8}{4\pi}\left| \omega t - \frac{\sin 2\omega t}{2} \right|_0^{\pi}$$

$$= 20.372 + 19.2 = 39.572 \text{ W}$$

$$\text{Rms current rating} = \frac{I_{max}}{2} = \frac{80}{2} = 40 \text{ A}$$

Student's Assignments 1

Q.1 The latching current in the below circuit is 4 mA. The minimum width of the gate pulse required to turn on the thyristor is



(a) 6 μs (b) 4 μs
(c) 2 μs (d) 1 μs

Q.2 Triac cannot be used in
(a) ac voltage regulators
(b) cycloconverters
(c) solid state type of switch
(d) inverter

Q.3 The snubber circuit is used in thyristor circuits for
(a) triggering (b) dv/dt protection
(c) di/dt protection (d) phase shifting

Q.4 It is preferable to use a train of pulse of high frequency for gate triggering of SCR in order to reduce
(a) dv/dt problem
(b) di/dt problem
(c) the size of the pulse transformer
(d) the complexity of the firing circuit

Q.5 Which one of the following is NOT the advantage of solid state switching of ac capacitors into ac supply over relay-based switching?
(a) low transients (b) low losses
(c) fast response (d) long life

Q.6 The sharing of the voltages between thyristors operating in series is influenced by the
(a) di/dt capabilities
(b) dv/dt capabilities
(c) junction temperatures
(d) static v-i characteristics and leakage currents

Q.7 R-C snubber is used in parallel with the thyristor to
(a) reduce dv/dt across it
(b) reduce di/dt through it
(c) limit current through the thyristor
(d) ensure its conduction after gate signal is removed

Q.8 Which one of the following statements is correct? The turn off times of converter grade SCRs are normally in the range of
(a) 1 to 2 microseconds
(b) 50 to 200 microseconds
(c) 500 to 1000 microseconds
(d) 1 to 2 milliseconds

Q.9 Which one of the following statements is correct? In a thyristor, the holding current I_H is
(a) more than the latching current I_L
(b) less than I_L
(c) equal to I_L
(d) equal to zero

Q.10 Which one of the following is used as the main switching element in a switched mode power supply operating in 20 kHz to 100 kHz range?
(a) Thyristor (b) MOSFET
(c) Triac (d) UJT

Q.11 Snubber circuits are used to protect thyristor from which of the following?
(a) High $\frac{di}{dt}$ and low $\frac{dv}{dt}$
(b) High $\frac{dv}{dt}$ and low $\frac{di}{dt}$
(c) Low $\frac{dv}{dt}$ and low $\frac{di}{dt}$
(d) High $\frac{dv}{dt}$ and high $\frac{di}{dt}$

Q.12 Number of thyristors, each with a rating of 500 V, 75 A, required in each branch of a series-parallel combination for a circuit with a total voltage and current ratings of 7.5 kV and 1 kA respectively. If the device derating factor is 14%, then what is the number of thyristors in series and parallel branch respectively?

	No of thyristors in series branch	No of thyristors in parallel branch
(a)	18	16
(b)	15	14
(c)	12	12
(d)	16	18

Q.13 The anode current through a conducting SCR is 10 A. If its gate current is made one-fourth, then what will be the anode current?
(a) 0 A (b) 5 A
(c) 10 A (d) 20 A

Q.14 In a power circuit of 3 kV, four thyristors each of rating 800 V are connected in series. What is the percentage series derating factor?
(a) 50 (b) 25
(c) 12.5 (d) 6.25

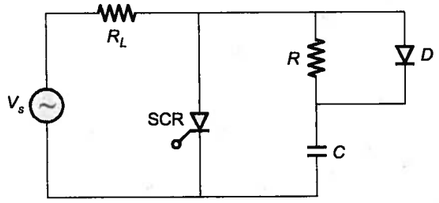
Q.15 For an SCR, the gate cathode characteristic has a straight line slope of 140. For trigger source voltage of 20 V and allowable gate power dissipation of 0.5 Watts, what is the gate source resistance?
(a) 200 Ω (b) 255 Ω
(c) 195 Ω (d) 185 Ω

Q.16 An SCR is rated for 650 V PIV. What is the voltage for which the device can be operated if the voltage safety factor is 2?
(a) 325 V_{rms} (b) 230 V_{rms}
(c) 459 V_{rms} (d) 650 V_{rms}

Q.17 DIAC is combination of
(a) two antiparallel diode
(b) two antiparallel SCR
(c) two antiparallel SCR with no gate terminal
(d) none of these

Q.18 Which semiconductor power device out of the following is not a current triggered device?
(a) Thyristor (b) G.T.O
(c) Triac (d) MOSFET

Q.19 In figure the voltage source is 200 V the load resistance is 20 Ω. The SCR can with stand a dV/dt value 75 V/μs. If the snubber discharge current must be limited to 4 A.



(a) 70.71 Ω, 0.178 μF
(b) 70.71 Ω, 0.119 μF
(c) 50 Ω, 0.178 μF
(d) 50 Ω, 0.119 μF

Q.20 Surge current rating of an SCR specifies the maximum
(a) repetitive current with rectangular wave
(b) non-repetitive current with rectangular wave
(c) repetitive current with sinusoidal wave
(d) non-repetitive current with sinusoidal wave

Q.21 Gate characteristic of a thyristor
(a) is of the type $V_g = a + bI_g$
(b) has a spread between two curves of $V_g - I_g$
(c) is a straight line passing through origin
(d) is a curve between V_g and I_g

Q.22 A metal oxide varistor is used for protecting
(a) gate circuit against overcurrents
(b) anode circuit against overcurrents
(c) gate circuit against overcurrents
(d) anode circuit against overvoltages

Q.23 For an SCR, Gate source voltage is a rectangular pulse of 20 V with 10 msec duration. For an average gate power dissipation of 0.4 W and a peak gate drive power 8 W. Find the tiriggering pulse.
(a) 5 kHz, 0.05 (b) 3 kHz, 0.05
(c) 5 kHz, 0.06 (d) 3 kHz, 0.06

Q.24 A thyristor is triggered by a pulse train of 3 kHz. The duty ratio is 0.6. If the allowable average power is 60 W, the maximum allowable gate drive power is
(a) $100\sqrt{2}$ W (b) 100 W
(c) 200 W (d) 180 W

Q.25 A GTO with anode fingers has

(a) reduced tail current

(b) reduec turn-off gain

(c) less reverse blocking capability

(d) high turn-off time

Q.26 A Triac is not preferred for

(a) High inductive load

(b) Low inductive load

(c) High resistive load

(d) None of these

Answer Key:

1. (b)	**2.** (d)	**3.** (b)	**4.** (c)
5. (a)	**6.** (d)	**7.** (a)	**8.** (b)
9. (b)	**10.** (b)	**11.** (d)	**12.** (a)
13. (c)	**14.** (d)	**15.** (c)	**16.** (b)
17. (c)	**18.** (d)	**19.** (b)	**20.** (d)
21. (b)	**22.** (d)	**23.** (a)	**24.** (b)
25. (c)	**26.** (a)		