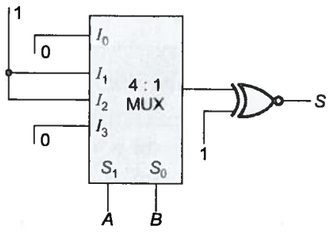
3 Combinational Logic Circuits

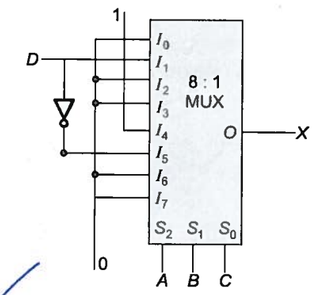
Multiple Choice Questions

Q.1 The circuit shown below does not represent



(a) $S(A, B) = \Sigma(1, 2)$
(b) EXOR gate with A and B as inputs
(c) $S(A, B) = \Pi(0, 3)$
(d) Equality function

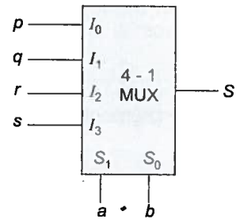
Q.2 The circuit below represents function $X(A, B, C, D)$ as:



(a) $\Sigma(3, 8, 9, 10)$
(b) $\Sigma(3, 8, 10, 14)$
(c) $\Pi(0, 1, 2, 4, 5, 6, 7, 11, 12, 13, 15)$
(d) $\Pi(0, 1, 2, 4, 5, 6, 7, 10, 12, 13, 15)$

Q.3 If half adders and full adders are implemented using gates, then for the addition of two 17 bit numbers (using minimum gates) the number of half adders and full adders required will be
(a) 0, 17 (b) 16, 1
(c) 1, 16 (d) 8, 8

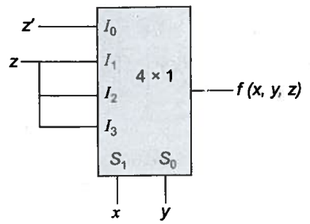
Q.4 Consider the function $F(a, b, c) = \bar{b}\,\bar{c} + bc + a\bar{b}$. If you implement F by means of 4-to-1 multiplexer then what will be the values of p, q, r, s, in the following figure.



(a) $\bar{C}$, C, 1, C
(b) C, $\bar{C}$, C, 0
(c) 1, 0, C, $\bar{C}$,
(d) C, $\bar{C}$, 1, $\bar{C}$

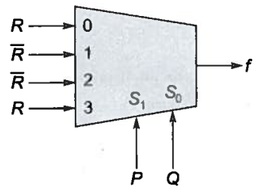
Q.5 x and y are two n-bit numbers. These numbers are added by a n-bit carry-lookahed adder, which uses k logic-levels. If the average gate delay of carry-lookahead adder is d then what will be the maximum delay of carry-lookahead adder circuit?
(a) n^2 (b) kd
(c) nkd (d) nd

Q.6 Consider the following circuit



If f (x, y, z) is $\Sigma(0, 3, 5, 7)$ then what will be the value of at I_0 and I_2 (respectively)?
(a) $\bar{Z}, Z$ (b) $\bar{Z}, \bar{Z}$
(c) Z, Z (d) $Z, \bar{Z}$

Q.7 The Boolean expression for the output f of the multiplexer shown below is



(a) $\overline{P \oplus Q \oplus R}$ (b) $P \oplus Q \oplus R$
(c) $P + Q + R$ (d) $\overline{P + Q + R}$
[GATE-2010]

Q.8 In a look-ahead carry generator, the carry generate function G_i and the carry propagate function P_i for inputs, A_i and B_i are given by

$$P_i = A_i \oplus B_i \text{ and } G_i = A_i B_i$$

The expressions for the sum bit S_i and carry bit C_{i+1} of the look-ahead carry adder are given by $S_i = P_i \oplus C_i$ and $C_{i+1} = G_i + P_i C_i$, where C_0 is the input carry.

Consider a two-level logic implementation of the look-ahead carry generator. Assume that all P_i and G_i are available for the carry generator circuit and that the AND and OR gates can have any number of inputs. The number of AND gates and OR gates needed to implement the look-ahead carry generator for a 4-bit adder with S_3, S_2, S_1, S_0 and C_4 as its outputs are respectively
(a) 6, 3 (b) 10, 4
(c) 6, 4 (d) 10, 5

Q.9 Suppose only one multiplexer and one inverter are allowed to be used to implement any Boolean function of n variables. What is the minimum size of the multiplexer needed?
(a) 2^n line to 1 line
(b) 2^{n+1} line to 1 line
(c) 2^{n-1} line to 1 line
(d) 2^{n-2} line to 1 line **[GATE-2007]**

Q.10 Consider two 4-bit numers $A = A_3 A_2 A_1 A_0$ and $B = B_3 B_2 B_1 B_0$ and the expression $x_i = A_i B_i + \overline{A_i}\,\overline{B_i}$ for $i = 0, 1, 2, 3$. The expression

$$A_3\overline{B_3} + x_3 A_2\overline{B_2} + x_3 x_2 A_1\overline{B_1} + x_3 x_2 x_1 A_0\overline{B_0}$$

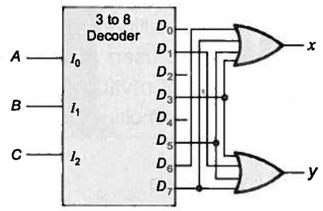
evaluates to 1 if
(a) $A = B$ (b) $A \neq B$
(c) $A > B$ (d) $A < B$
[DRDO-2009]

Q.11 Consider the multiplexer with X and Y as data inputs and Z as control input. $Z = 0$ selects input X and $Z = 1$ selects input Y. What are the connections required to realize the 2-variable Boolean function $f = T + R$, without using any additional hardware?
(a) R to X, 1 to Y, T to Z
(b) T to X, R to Y, T to Z
(c) T to X, R to Y, 0 to Z
(d) R to X, 0 to Y, T to Z **[ESE-2009]**

Q.12 Consider the following statements:
A multiplexer
1. selects one of the several inputs and transmits it to a single output
2. routes the data from a single input to one of many output
3. converts parallel data into serial data
4. is a combinational circuit

Which of these statements are correct?
(a) 1, 2 and 4 (b) 2, 3, and 4
(c) 1, 3 and 4 (d) 1, 2 and 3
[ESE-2000]

Q.13 The builiding block shown in figure is a active high output decoder

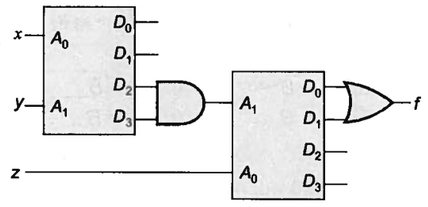


The output X is

(a) $AB + BC + CA$ (b) $A + B + C$

(c) ABC (d) None of these

Q.14 A logic circuit consist of two 2 ×4 decoders as shown in the figure. The output of decoder are as follow:



$D_0 = 1$ when $A_0 = 0, A_1 = 0$

$D_1 = 1$ when $A_0 = 1, A_1 = 0$

$D_2 = 1$ when $A_0 = 0, A_1 = 1$

$D_3 = 1$ when $A_0 = 1, A_1 = 1$

The value of $f(x, y, z)$ is

(a) 0 (b) z

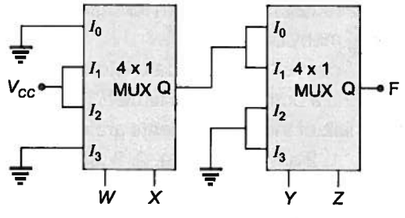
(c) $\bar{z}$ (d) 1

Q.15 Minimum number of NOR gates required to implement Sum in half-adder circuit is:

(a) 2 (b) 3

(c) 4 (d) 5

Q.16 In the circuit shown, W and Y are MSBs of the control inputs. The output is given by



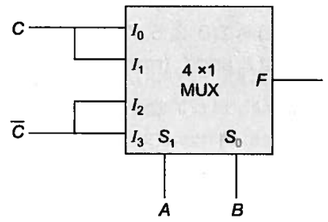
(a) $F = W\bar{X} + \bar{W}X + \bar{Y}\bar{Z}$

(b) $F = W\bar{X} + \bar{W}X + \bar{Y}Z$

(c) $F = W\bar{X}\bar{Y} + \bar{W}X\bar{Y}$

(d) $F = (\bar{W} + \bar{X})\bar{Y}\bar{Z}$

Q.17 The logic circuit realized by the circuit shown in the given figure will be

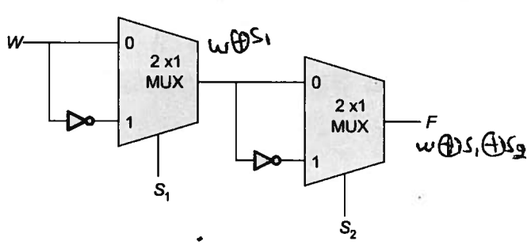


(a) $B \odot C$ (b) $F = B \oplus C$

(c) $A \odot C$ (d) $F = A \oplus C$

[ESE-1999]

Q.18 Consider the multiplexer based logic circuit shown in the figure.



Which one of the following Boolean functions is realized by the circuit?

(a) $F = W\bar{S}_1\bar{S}_2$

(b) $F = WS_1 + WS_2 + S_1S_2$

(c) $F = \bar{W} + S_1 + S_2$

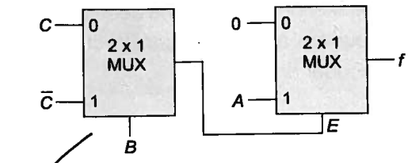
(d) $F = W \oplus S_1 \oplus S_2$ **[GATE-2014]**

Q.19 The minimum number of 2 × 1 multiplexers required to implement a half adder circuit are [when only basic inputs are available, compliments are not available].

(a) 4 (b) 2

(c) 3 (d) 5

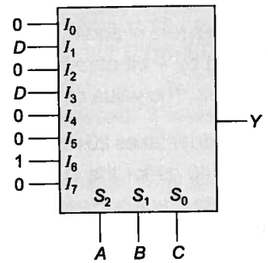
Q.20 The Boolean function 'f' implemented as shown in the figure using two input multiplexers is



(a) $A\bar{B}C + AB\bar{C}$ (b) $ABC + A\bar{B}\bar{C}$

(c) $\bar{A}BC + AB\bar{C}$ (d) $\bar{A}\bar{B}C + \bar{A}B\bar{C}$

Q.21 An 8-to-1 multiplexer is used to implement a logical function Y as shown in the figure. The output

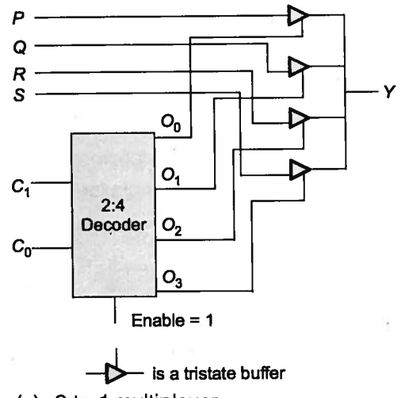


(a) $Y = A\bar{B}C + A\bar{C}D$ (b) $Y = \bar{A}BC + A\bar{B}D$

(c) $Y = AB\bar{C} + \bar{A}CD$ (d) $Y = \bar{A}\bar{B}D + A\bar{B}C$

[GATE-2014]

Q.22 The functionality implemented by the circuit below is



(a) 2-to-1 multiplexer

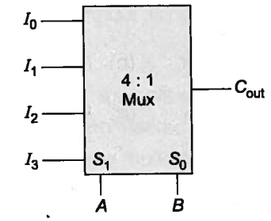
(b) 4-to-1 multiplexer

(c) 7-to-1 multiplexer

(d) 6-to-1 multiplexer

[GATE-2016]

Q.23 A 4:1 multiplexer is to be used for generating the output carry of a full adder. A and B are the bits to be added while C_{in} is the input carry and C_{out} is the output carry. A and B are to be used as the select bits with A being the more significant select bit.



Which one of the following statements correctly describes the choice of signals to be connected to the inputs I_0, I_1, I_2 and I_3 so that the output is C_{out}?

(a) $I_0 = 0, I_1 = C_{in}, I_2 = C_{in}$ and $I_3 = 1$

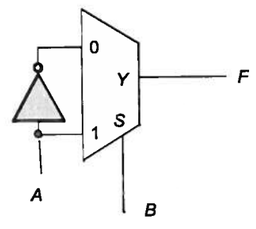
(b) $I_0 = 1, I_1 = C_{in}, I_2 = C_{in}$ and $I_3 = 1$

(c) $I_0 = C_{in}, I_1 = 0, I_2 = 1$ and $I_3 = C_{in}$

(d) $I_0 = 0, I_1 = C_{in}, I_2 = 1$ and $I_3 = C_{in}$

[GATE-2016]

Q.24 Consider the following circuit which uses a 2-to-1 multiplexer as shown in the figure below. The Boolean expression for output F in terms of A and B is?

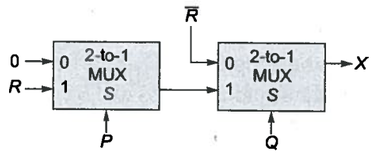


(a) $A \oplus B$ (b) $\overline{A+B}$

(c) $A + B$ (d) $\overline{A \oplus B}$

[GATE-2016]

Q.25 Consider the two cascaded 2-to-1 multiplexers as shown in the figure.



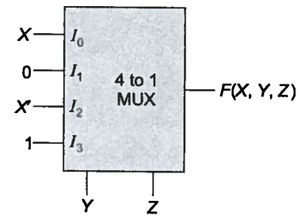
The minimal sum of products form of the output X is

(a) $\bar{P}\bar{Q}+PQR$ (b) $\bar{P}Q+QR$

(c) $PQ+\bar{P}\bar{Q}\bar{R}$ (d) $\bar{R}\bar{Q}+PQR$

[GATE-2016]

Q.26 A 4 to 1 multiplexer to realize a Boolean function $F(X, Y, Z)$ is shown in the figure below. The inputs Y and Z are connected to the selectors of the MUX (Y is more significant). The canonical sum-of-product expression for $F(X, Y, Z)$ is



(a) $\Sigma m(2, 3, 4, 7)$ (b) $\Sigma m(1, 3, 5, 7)$

(c) $\Sigma m(0, 2, 4, 6$ (d) $\Sigma m(2, 3, 5, 6)$

[GATE-2016]

Numerical Data Type Questions

Q.27 Minimum number of NAND gates required to implement Sum in half-adder circuit is _____.

Q.28 Minimum number of 2 × 1 multiplexers required to realize the following function is _____.

$$f(A,B,C) = \bar{A}\bar{B}C + \bar{A}B\bar{C}$$

(Assume that inputs are available only in true form and Boolean constants 1 and 0 are available.)

Q.29 The number of 2-to-4-line decodes with enable input are needed to construct a 4-to-16-line decoder are _____.

[DRDO-2009]

Q.30 A person wants to design a 4 × 1 multiplexer using only NAND gates. If NAND gates with any number of inputs are available, then total number of NAND gates required are _____.

Q.31 A one bit full adder takes 75 nsec to produce sum and 50 nsec to produce carry. A 4 bit parallel adder is designed using this type of full adder. The maximum rate of additions per second can be provided by 4 bit parallel adder is $A \times 10^6$ additions/sec. The value of A is _____.

Q.32 A 1 bit full adder takes 20 ns to generate carry-out bit and 40 ns for the sum bit. What is the maximum rate of addition per second, when four 1 bit full address are cascade?

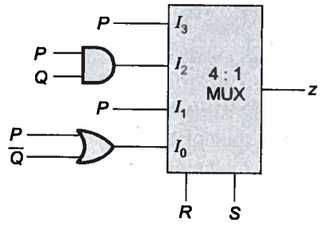
[ESE-2005]

Try Yourself

T1. Design a logic circuit for detecting equality of 2-bit binary numbers.

T2. Design a combination circuit that accepts a 2 bit number as input and generate binary number equal to square of the input number.

T3. For the circuit shown in the following figure, $I_0 - I_3$ are inputs to the 4 : 1 multiplexer. R (MSB) and S are control bits.



The output Z can be represented by

(a) $PQ+P\bar{Q}S+\bar{Q}\bar{R}\bar{S}$

(b) $P\bar{Q}+PQ\bar{R}+\bar{P}\bar{Q}\bar{S}$

(c) $P\bar{Q}\bar{R}+\bar{P}QR+PQRS+\bar{Q}\bar{R}\bar{S}$

(d) $PQ\bar{R}+PQR\bar{S}+P\bar{Q}\bar{R}S+\bar{Q}\bar{R}\bar{S}$

[GATE-2008]

Statement for Linked Answer Question (4 and 5):
Two products are sold from a vending machine, which has two push buttons P_1 and P_2. When a button is pressed, the price of the corresponding product is displayed in a 7-segment display.

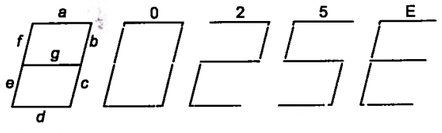
If no buttons are pressed, '0' is displayed, signifying 'Rs. 0'

If only P_1 is pressed, '2' is displayed, signifying 'Rs.2'

If only P_2 is pressed, '5' is displayed, signifying 'Rs.5'

If both P_1 and P_2 are pressed, 'E' is displayed, signifying 'Error'

The names of the segments in the 7-segment display, and the glow of the display for '0', '2', '5' and 'E' are shown below.



Consider:

(i) push button pressed/not pressed in equivalent to logic 1/0 respectively,

(ii) a segment glowing/not glowing in the display is equivalent to logic 1/0 respectively

T4. If segments a to g are considered as functions of P_1 and P_2, then which of the following is correct?

(a) $g = \bar{P}_1 + P_2, d = c + e$

(b) $g = P_1 + P_2, d = c + e$

(c) $g = \bar{P}_1 + P_2, e = b + c$

(d) $g = P_1 + P_2, e = b + c$

T5. What are the minimum numbers of NOT gates and 2-input OR gates required to design the logic of the driver for this 7-segment display?

(a) 3 NOT and 4 OR

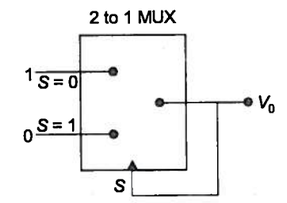
(b) 2 NOT and 4 OR

(c) 1 NOT and 3 OR

(d) 2 NOT and 3 OR

T6. The number of 3-to-8 line decoders with an enable input are needed to construct a 6-to-64 line decoder without using any other logic gates are _____.

T7. A 2-to-1 digital multiplexer having a switching delay of 1 μs is connected as shown in the figure. The output of the multiplexer is tied to its own select input S. The input which gets selected when $S = 0$ is tied to 1 and the input that gets selected when $S = 1$ is tied to 0. The output V_0 will be



(a) 0

(b) 1

(c) Pulse train of frequency 0.5 MHz

(d) Pulse train of frequency 1.0 MHz

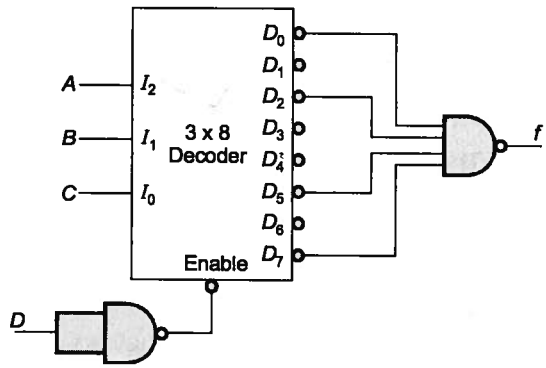
T8. A 4-bit carry lookahead adder, which adds two 4-bit numbers, is designed using AND, OR, NOT, NAND, NOR gates only. Assuming that all the inputs are available in both complemented and uncomplemented forms and the dealy of each gate is1 time unit, what is the overall propagation delay of the adder? Assume that the carry network has been implemented using two-level AND-OR logic.

(a) 4 time units (b) 6 times units

(c) 10 times units (d) 12 times units

[GATE-2004]

T9. The logic function $f(A, B, C, D)$ implemented by the circuit shown below is



(a) $\bar{D}(A \oplus C)$ (b) $D(A \odot C)$

(c) $\bar{D}(A \oplus B)$ (d) $D(A \odot B)$

T10. Without any additional circuitry, an 8 :1 MUX can be used to obtain

(a) some but not all Boolean functions of 3 variables

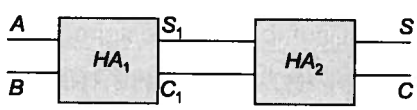
(b) all functions of 3 variables but none of 4 variables

(c) all functions of 3 variables and some but not all of 4 variables

(d) all functions of 4 variables

[GATE-EC:2003]

T11. Two Half Adders are connected in cascade as shown in figure below. The output "S" and "C" are



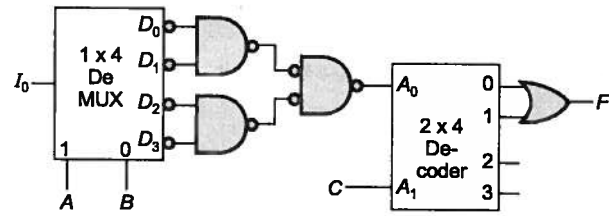
(a) $S = A \oplus B,\ C = AB$

(b) $S = A \odot B, C = 0$

(c) $S = A + B,\ C = 0$

(d) $S = AB,\ C = 0$

T12. Consider the logic circuit given below



The minimized expression for F is

(a) $\bar{C}$ (b) I_0

(c) C (d) $\bar{I}_0$

T13. A 4 bit binary adder is adding two *BCD* numbers and producing the sum output $S_3S_2S_1S_0$ along with the carry output C_0. It is required to design a checking circuit such that the checking circuit output must be zero, whenever the binary adder output is invalid *BCD*, the boolean expression of checking circuit is

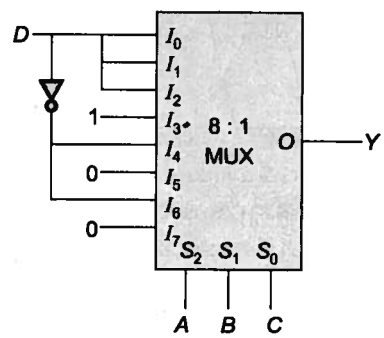
(a) $\bar{C}_0\bar{S}_3 + \bar{C}_0\bar{S}_2\bar{S}_1$

(b) $C_0 + S_3S_2 + S_2S_1$

(c) $(\bar{C}_0 + \bar{S}_3)\cdot(\bar{C}_0 + \bar{S}_2 + \bar{S}_1)$

(d) None of the above

T14. For the given multiplexer, Y is equal to



(a) $A\bar{C}\bar{D} + \bar{A}BC + \bar{A}D$

(b) $A\bar{B}\bar{C} + A\bar{C}\bar{D} + \bar{A}D$

(c) $\bar{A}\bar{B}\bar{C} + AC\bar{D} + \bar{A}\bar{D}$

(d) $A\bar{C}\bar{D} + \bar{A}\bar{B}D + A\bar{D}$