Interfacing with Microprocessor

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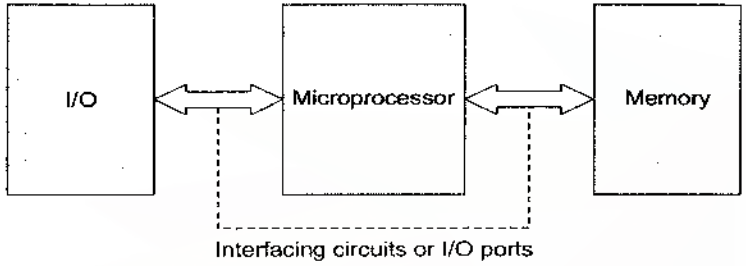
Interfacing



- Designing logic circuits and writing program to make the processor communicated either with memory or I/O is known as interfacing.
- The logic circuits used are known as interfacing circuits or I/O ports.

Characteristics of Memory

- **Capacity**

Memory capacity depends upon the amount of data that can be stored.

- **Memory size** $= 2^A \times D$

  where $A \rightarrow$ Address lines

  $D \rightarrow$ Data lines

- **Number of chips required**

$$n = \frac{\text{Size of } M_2}{\text{Size of } M_1}$$

where, n = Number of chips required

M_1 = Available capacity

M_2 = Memory to be designed

- If initial address and memory size is given then formulae for last address

  last address = [Initial address in hexadecimal + hexadecimal equivalent of memory size $- (1)_H$]

- If memory range is given then formulae for calculating memory size

  Memory size = $[(\text{last address})_H - (\text{Initial address})_H + (1)_H]$ byte

Remember:

- 8085 microprocessor internally divide the crystal oscillator frequency by 2 so crystal oscillator frequency is always 2 times the microprocessor frequency of operation.
- Data bus reflects the bit of microprocessor.
- Address bus reflects maximum memory that can be interfaced to microprocessor.

Interfacing with I/O Ports

There are two ways by which I/O port can be connected to the microprocessor:

1. Memory mapped I/O scheme
2. I/O mapped I/O scheme

Comparison between Memory Mapped I/O and I/O Mapped I/O Scheme

Characteristic	Memory-mapped I/O	I/O Mapped I/O
• Device Address	16-bit	8-bit
• Control signals for Input/Output	$\overline{MEMR}$ / $\overline{MEMW}$	$\overline{IOR}$ / $\overline{IOW}$
• Instruction available	Memory-related instructions such as LDA; STA; LDAX; STAX; MOV M, R; ADD M, SUB M; ANA M; etc.	IN and OUT
• Data Transfer	Between any register and I/O	Only between I/O and the accumulator.
• Maximum number of input/output devices possible	The memory map (64 K) is shared between I/O devices and system memory.	The I/O map is independent of the memory map; 256 input devices and 256 output devices can be connected.
• Execution speed	13 T-states (STA, LDA) 7 T-states (MOV M,R)	10 T-states
• Hardware requirements	More hardware is needed to decode 16-bit address.	Less-hardware is needed to decode 8-bit address.
• Other features	Arithmetic or logical operations can be directly performed with I/O data.	Not available

Interfacing Devices

Intel 8155 : Programmable Peripheral Interface

The 8155 includes 256 bytes of RD/WR memory i.e. RAM, 3 I/O ports and a 16-bit timer.

ormat of 8155 Timer

LSB Timer =	T_7	T_6	T_5	T_4	T_3	T_2	T_1	T_0
MSB Timer =	M_2	M_1	T_{13}	T_{12}	T_{11}	T_{10}	T_9	T_8

Where,

M_2	M_1	Modes		
0	0	Mode 0	⇒	Single square wave cycle
0	1	Mode 1	⇒	Square wave
1	0	Mode 2	⇒	Single pulse after terminal count
1	1	Mode 3	⇒	Pulse every terminal count

ıtel 8255 : Programmable Peripheral Interface/Adopter

The 8285 is widely used programmable parallel I/O device. It can be program to transfer data under various conditions from I/O to interrupt I/O.

Operating modes of 8255

1. Mode 0 ⇒ Simple input/output
2. Mode 1 ⇒ Strob input/output
3. Mode 2 ⇒ Bidirectional port

ıtel 8251 : Programmable Communication Interface

Intel 8251 is also known as universal synchronous/asynchronous receiver/transmitter (USART) used to transmit serial data.

ıtel 8253 : Programmable Interval Timer

The programmable counter/interval time is used in real time application of timing and counting such as BCD/binary counting, generation of time delay etc.

The 8253 uses NMOS technology and operates any of the following six modes:

1. Mode 0 ⇒ Interrupt on terminal count
2. Mode 1 ⇒ Programmable one shot
3. Mode 2 ⇒ Rate generator
4. Mode 3 ⇒ Square wave generator
5. Mode 4 ⇒ Software trigger strobe
6. Mode 5 ⇒ Hardware trigger strobe

tel 8257 : Progammable DMA Controller

In DMA data transfer scheme, data are directly transferred from an I/O device to RAM or from RAM to an I/O device thus it is capable of performing three operations i.e. read, write and verify.

Intel 8259 : Progammable Interrupt Controller

The programmable interrupt controller is used when several I/O devices transfer data using interrupt and they are to be connected to the same interrupt level of the microprocessor.

Intel 8272 : Floppy Disk Controller

The function of floppy disk controller is to interface a floppy disk system to a microprocessor.

Intel 8275 : Progammable CRT Controller

The Intel 8275 is a single chip device. Its function is to interface CRT raster scan display with the microcomputer.

Intel 8279 : Progammable Keyboard/Display Interface

The Intel 8279 is a programmable to keyboard interfacing device. It has two sections namely keyboard section and display section. The function of keyboard section is to interface the keyboard and the function of the display section is to drive alphanumeric displays or indicator lights.

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