Chapter 2

Bipolar Junction Transistor (BJT) Biasing

One mark questions (knowledge)

1. Define operating point.
2. What is DC load line?
3. Define quiescent point.
4. What is leakage current in BJT?
5. Write the relation between I_{CBO} and I_{CEO}.
6. What is thermal run away?
7. Define stability factor in BJT.
8. What is heat sink?

One mark questions (understanding)

1. What is meant by transistor biasing?
2. Why transistor is called as a current controlled device?
3. Name the two end points of the DC load line.
4. What is the value of V_{CE} at saturation point?
5. What is the value of I_C at cut off point?
6. Where should the Q point be located for the transistor to be operated as an amplifier?
7. Write the expression for DC load line of a transistor in CE configuration?
8. For the BJT to work as a closed switch where should the operating point be located on the DC load line?
9. For the BJT to work as an open switch where should the operating point be located on the DC load line?
10. Mention the transistor parameter that is temperature dependent.
11. Mention any one leakage current in a transistor.
12. Name any one biasing method for a transistor.
13. Name the biasing circuit which gives excellent stabilization.

Two mark questions (knowledge)

1. What are the biasing conditions for a transistor to be used as an amplifier?
2. Mention any two types of biasing methods.
3. What is leakage current? Mention different types of leakage currents.

Two mark questions (understanding)

1. What is the need for biasing a transistor?
2. Write the advantages of voltage divider bias circuit.
3. What is a heat sink? Mention its importance.

Two mark questions (skill)

1. Sketch the transistor output characteristics in CE mode. Indicate different regions of the characteristics.
2. Draw the biasing arrangement for an npn transistor in CE configuration with two sources.
3. Draw the DC load line on the output characteristics of a CE amplifier.

4. Draw the circuit diagram of a Voltage divider bias circuit.

Three mark questions (knowledge)

1. What is Q point? Explain its significance.
2. What is meant by stability factor? Mention the factors affecting it.

Three mark questions (understanding)

1. What is transistor biasing? Explain the need for biasing.
2. Derive an expression for the DC load line for a transistor in CE mode biased with two sources.
3. What is voltage divider bias? Mention its advantages.
4. Explain the leakage currents in CE and CB configurations.

Problems:

1. A transistor connected in CE mode in which collector supply is 8V and voltage drop across R_C = 800Ω connected in the collector circuit is 0.5V. If α = 0.96 determine V_{CE} and I_B.
2. A transistor has β = 100 and I_{CBO} = 5μA when it is connected in a circuit as a CE stage with zero load resistance, the collector current I_C = 1mA. Calculate the values of I_B, I_E and α.
3. For the given parameters values of voltage divider biasing circuit, determine the end points of the dc load line and draw the DC load line R_1=56KΩ, R_2=10KΩ, R_C=2.2KΩ, R_E=1KΩ and V_{CC}=12V.