



## Multiple Choice Questions

Q.1 The resolution of a 12 bit Analog to Digital converter in percent is

- (a) 0.01220 (b) 0.02441  
(c) 0.04882 (d) 0.09760

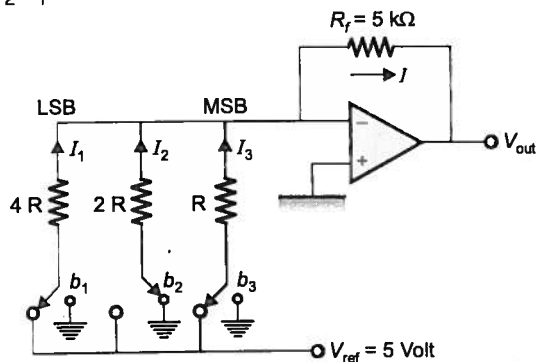
[ESE-2002(EE)]

Q.2 Consider a 6-bit D/A converter having full scale output of 3 mA and a full-scale error of  $\pm 0.4\%$  FS. For a binary input sequence of 1 0 1 1 1 1, the range of possible outputs will be

- (a) (2220–2240)  $\mu\text{A}$  (b) (492–512)  $\mu\text{A}$   
(c) (2226–2250)  $\mu\text{A}$  (d) (1295–1325)  $\mu\text{A}$

**Linked Data for Questions (3 and 4):**

A 3-bit weighted resistor D/A converter with MSB resistance  $R = 10\text{ k}\Omega$  having input bit stream  $b_3 b_2 b_1 = 1\ 0\ 1$  is shown in figure below:



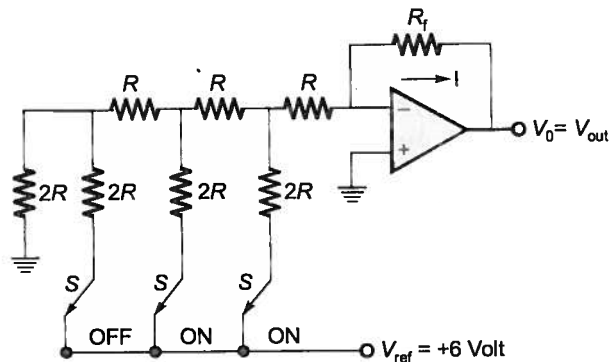
Q.3 The total input current ' $I$ ' in the circuit will be

- (a) 0.125 mA (b) 0.5 mA  
(c) 0.625 mA (d) 1.0 mA

Q.4 What is the analog output voltage by this DAC?

- (a) -3.125 volt (b) -0.625 volt  
(c) -2.5 volt (d) -5.0 volt

Q.5 The circuit shown below is a R-2R ladder type DAC with reference voltage +6 V and  $R_f = 9\text{ k}\Omega$  and  $R = 1\text{ k}\Omega$ .



As above figure-2 switches are ON and 1 is OFF, the output voltage will be

- (a) -6.75 V (b) -13.5 V  
(c) -20.25 V (d) -40.5 V

Q.6 The output voltage of a 5-bit D/A binary ladder that has a digital input of 11010 (Assuming 0 = 0 V and 1 = +10 V) is

- (a) 3.4375 V (b) 6.0 V  
(c) 8.125 V (d) 9.6875 V

[ESE-2001]

Q.7 Which one of the following D/A converters has the resolution of approximately 0.4% of its full scale range?

- (a) 8-bit (b) 10-bit  
(c) 12-bit (d) 16-bit

[ESE-2006]

Q.8 An 8 bit successive approximation analog to digital converter has full scale reading of 2.55 V and its conversion time for an analog input of 1 V is 20  $\mu\text{s}$ . The conversion time for a 2 V input will be

- (a)  $10\ \mu\text{s}$  (b)  $20\ \mu\text{s}$   
(c)  $40\ \mu\text{s}$  (d)  $50\ \mu\text{s}$

[GATE-2000]

Q.9 The minimum number of comparators required to build an 8 bit flash ADC is

- (a) 8 (b) 63  
(c) 255 (d) 256

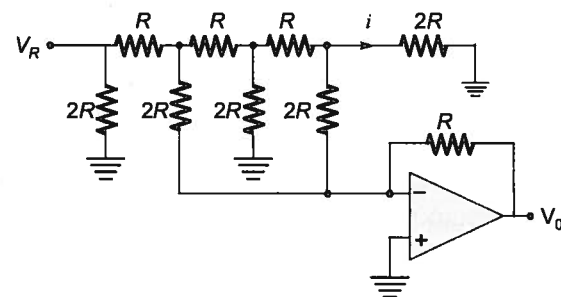
[GATE-2002]

Q.10 4 bit binary weighted resistor DAC has LSB resistance of  $32\ \text{k}\Omega$ . The corresponding MSB resistance is

- (a)  $2\ \text{k}\Omega$  (b)  $4\ \text{k}\Omega$   
(c)  $8\ \text{k}\Omega$  (d)  $32\ \text{k}\Omega$

**Statement for Linked Answer Questions (11 and 12):**

In the Digital-to-Analog converter circuit shown in the figure below,  $V_R = 10\ \text{V}$  and  $R = 10\ \text{k}\Omega$ .



[GATE-EC:2007]

Q.11 The current  $i$  is

- (a)  $31.25\ \mu\text{A}$  (b)  $62.5\ \mu\text{A}$   
(c)  $125\ \mu\text{A}$  (d)  $250\ \mu\text{A}$

[GATE-EC:2007]

Q.12 The voltage  $V_o$  is

- (a)  $-0.781\ \text{V}$  (b)  $-1.562\ \text{V}$   
(c)  $-3.125\ \text{V}$  (d)  $-6.250\ \text{V}$

[GATE-EC:2007]

Q.13 A 4-bit successive approximation type ADC has a full scale value of  $15\ \text{V}$ . The sequence of the states, the SAR will traverse, for the conversion of an input of  $8.15\ \text{V}$  is

- (a) Start Conversion  $\rightarrow 1000 \rightarrow 1100 \rightarrow 1010 \rightarrow 1001 \rightarrow 1000 \rightarrow$  End Conversion  
(b) Start Conversion  $\rightarrow 1000 \rightarrow 0100 \rightarrow 0010 \rightarrow 0001 \rightarrow 0000 \rightarrow$  End Conversion

(c) Start Conversion  $\rightarrow 1000 \rightarrow 0100 \rightarrow 0110 \rightarrow 0111 \rightarrow 1000 \rightarrow$  End Conversion

(d) Start Conversion  $\rightarrow 1000 \rightarrow 1100 \rightarrow 1110 \rightarrow 1111 \rightarrow 1111 \rightarrow$  End Conversion

[GATE-IN:2010]

Q.14 Which of the following statements is/are correct about Analog to Digital converters (ADCs).

- (i) Flash type ADCs are fastest  
(ii) In successive approximation type ADCs conversion time depends on magnitude of analog voltage.  
(iii) Counter type ADCs has fixed conversion time  
(iv) Dual-slope type ADCs are slowest

- (a) All of these (b) (ii) and (iii)  
(c) (i) and (iv) (d) (i) only

Q.15 For a 4-bit digital to analog convertor, analog voltage varies from 0 to  $1.5\ \text{volts}$ . The resolution of DAC is

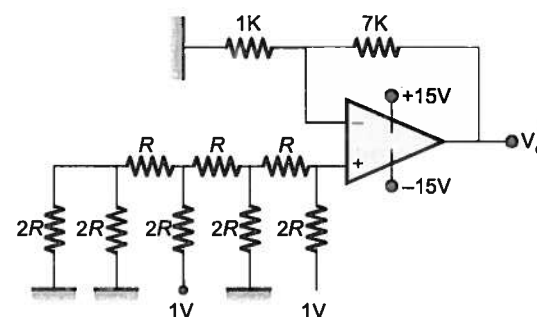
- (a) 10 % (b) 6.25 %  
(c) 6.67 % (d) 9.375 %

### Numerical Data Type Questions

Q.16 An 8-bit D/A converter has a full scale output voltage of  $20\ \text{V}$ . The output voltage when the input is  $11011011$ , is \_\_\_\_\_ V.

[ESE-2001]

Q.17 For the 4 bit DAC shown in the figure, the output voltage  $V_o$  is \_\_\_\_\_ V.



[GATE-2000]

Q.18 A 10-bit DAC provides an analog output which has a maximum value of  $10.23\ \text{volts}$ . Resolution of the DAC is \_\_\_\_\_ mV.

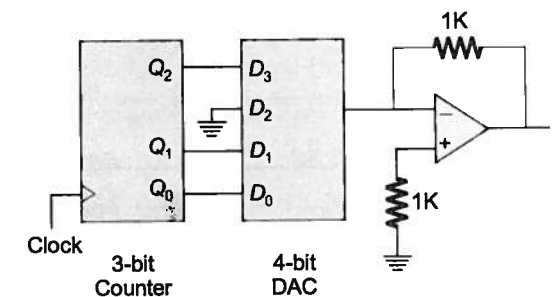
[ESE-2012]

Q.19 The analog output voltage of a 6 bit DAC with reference voltage as  $20\ \text{V}$  for the digital input  $011101$  is \_\_\_\_\_ Volts.

Q.20 A 5 bit D/A converter has a current output. If an output current  $I_{\text{out}} = 10\ \text{mA}$  is product for a digital input of  $10100$ , the value of  $I_{\text{out}}$  for a digital input of  $11101$  will be \_\_\_\_\_ mA.

### Try Yourself

T1. A 4-bit D/A converter is connected to a free-running 3-bit UP counter, as shown in the following figure. Which of the following waveforms will be observed at  $V_o$ ?



In the figure shown above, the ground has been shown by the symbol  $\nabla$ .

- (a) (b)   
(c) (d)

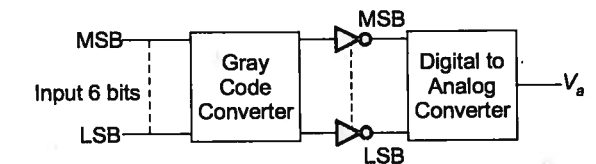
[GATE-2006]

T2. A 8-bit A/D converter is used over a span of zero to  $2.56\ \text{V}$ . The binary representation of  $1.0\ \text{V}$  signal is

- (a)  $01100100$  (b)  $01110001$   
(c)  $10100101$  (d)  $10100010$

[ESE-2013]

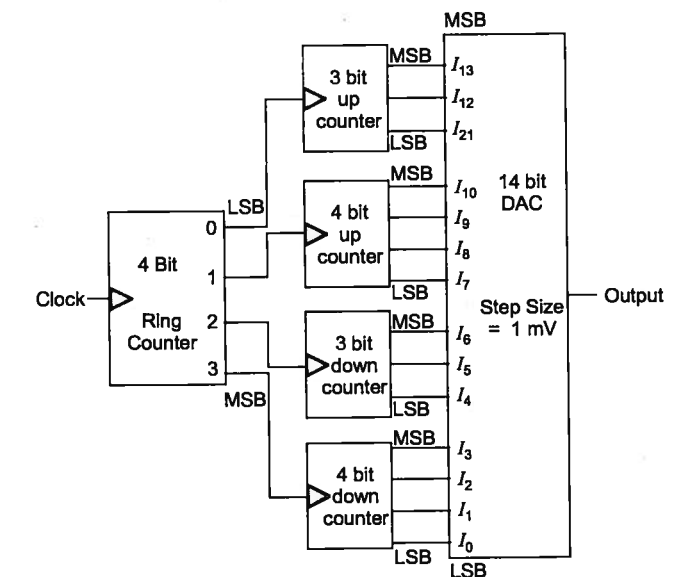
T3. Consider the circuit given below.



The full scale reading of Digital to Analog converter is  $10.5\ \text{V}$ . Each bit of Gray code converter output is given to digital to analog converter through an inverter. If input to the circuit is  $110011$ , then corresponding output voltage  $V_a$  is \_\_\_\_\_ Volts.

[Ans: 3.45 V]

T4. Consider the system given below:



The clock input is connected to the 4 bit ring counter. The output of the ring counter acts as the clock for the other counters. All the counters shown in figure are positive edge triggered. The output of all counters act as input to a 14 bit DAC with step size (D) equal to  $1\ \text{mV}$ . If initially all counter are cleared then find the output of DAC after 20 clock pulses.

[Ans: 10.96 V]