✡ Digital to Analog Converter (DAC).

(a) Binary weighted Resistor DAC.

(b) R-2R Ladder DAC.

✡ Analog to Digital Converter (ADC)

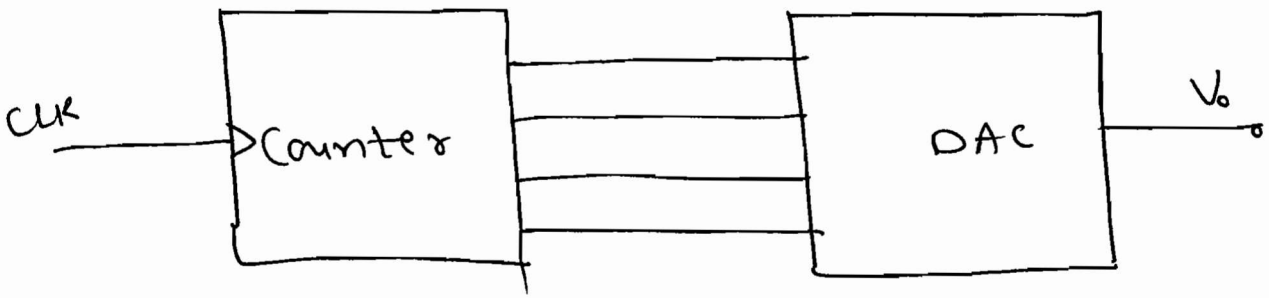
(a) Counter Type ADC

(b) Successive Approx ADC.

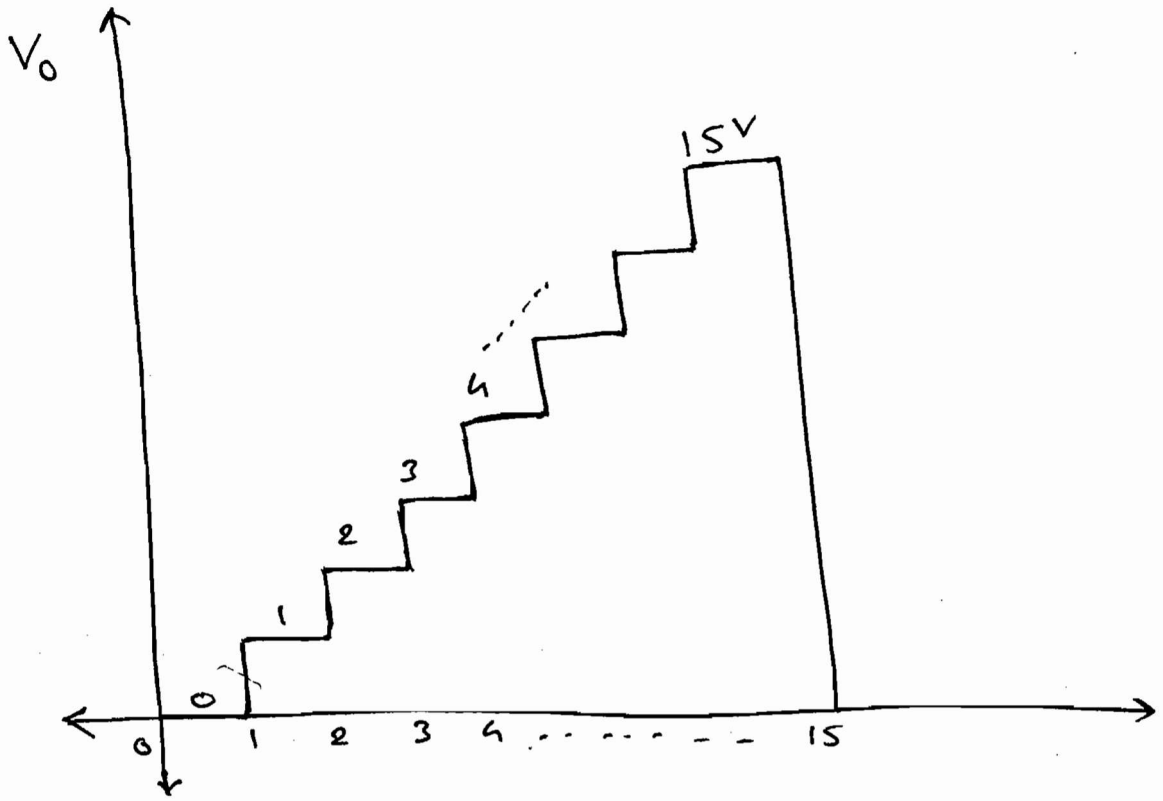
(c) Flash (or) Parallel ADC.

(d) Dual Slope (or) Integrating ADC.

(e) signal - delta ADC (Σ-Δ ADC).



CLK	Counter	V_o
0	0 0 0 0	0V
1	0 0 0 1	(let) 1V
2	0 0 1 0	2V
3		
⋮		⋮
15	1 1 1 1	15V



(1) FSO (Full Scale O/P) = 15V

→ N-Bit DAC: $= (2^N - 1) \times$ Stepsize.

(2) (a) Resolution:

→ It is the minimum Change possible at the O/P of the DAC for any change in the digital input.

ⓐ Resolution = Stepsize (Volts).

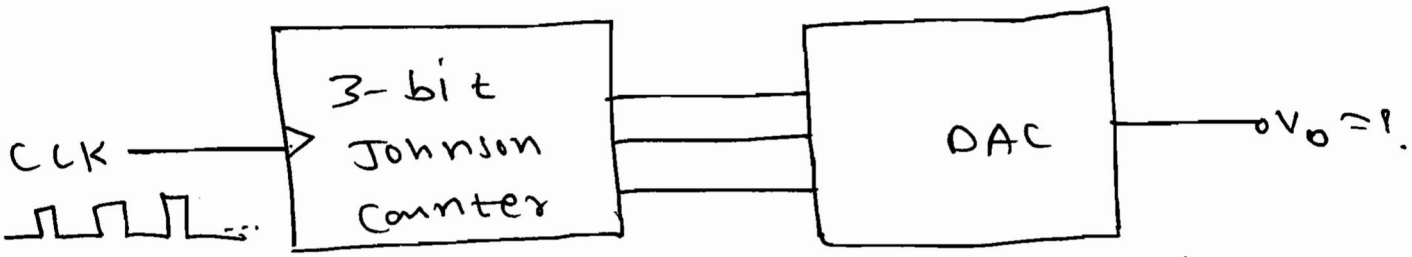
ⓑ % Resolution = $\frac{\text{Stepsize}}{\text{FSO}} \times 100$

$= \frac{\text{stepsize}}{(2^N - 1) \times \text{stepsize}} \times 100$

$= \frac{100}{2^N - 1}$.

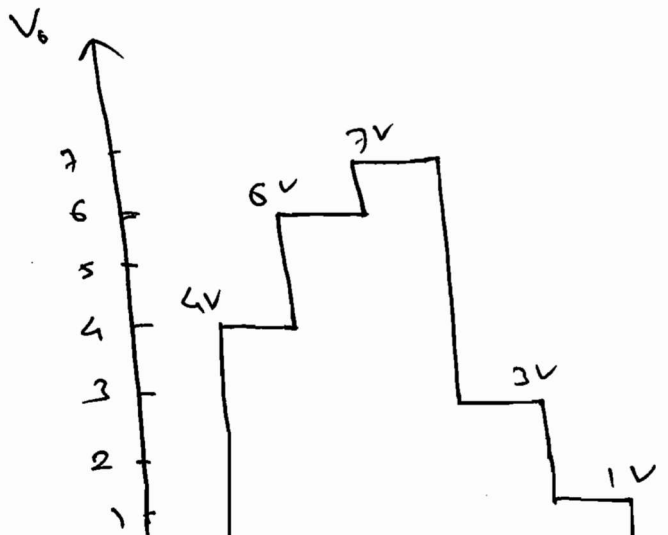
DAC	DAC
0.1 V	8-Bit
0.5 V	16-Bit
1.0 V	32-Bit.

Ex:1

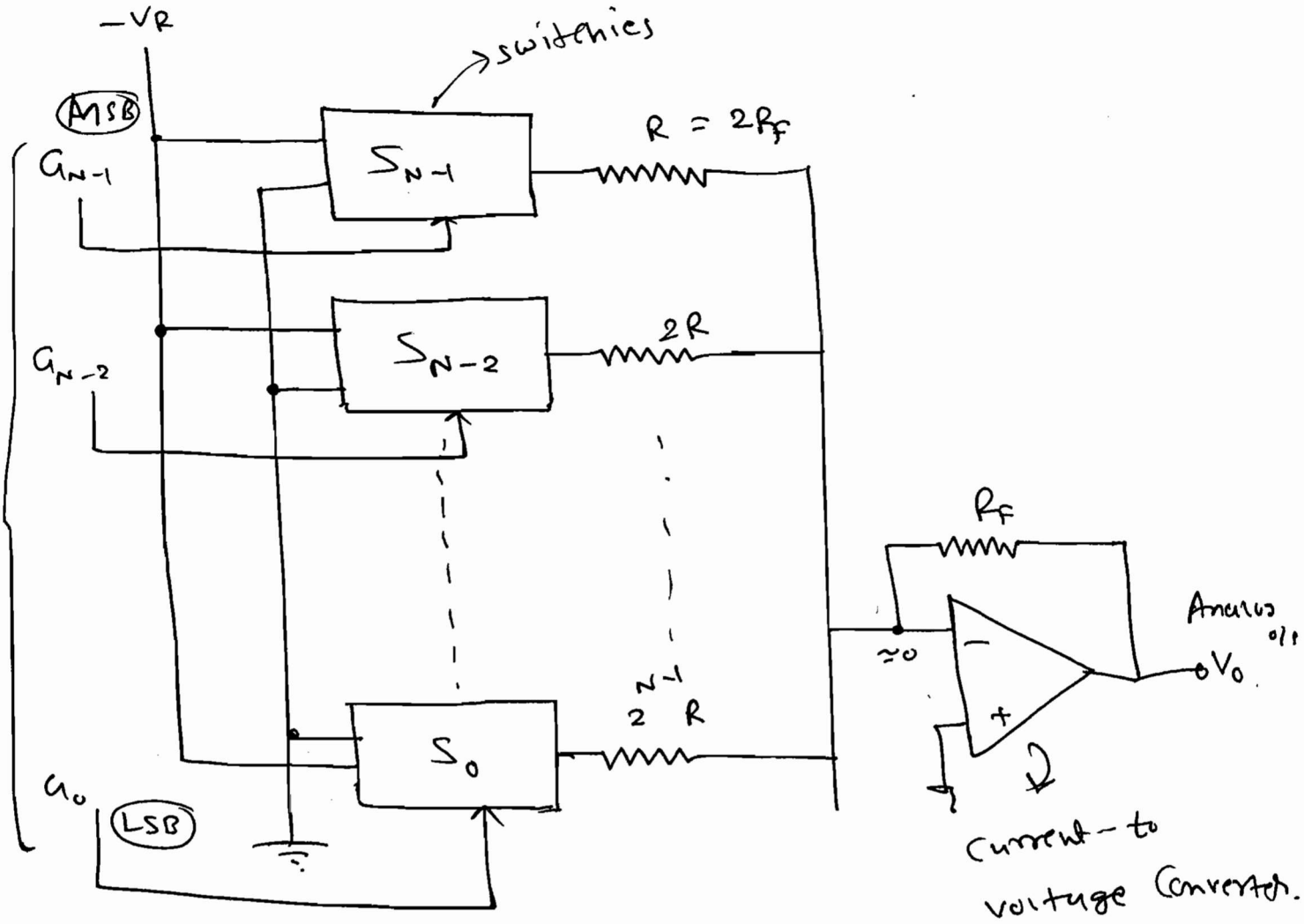


CLK | Counter | V_o.

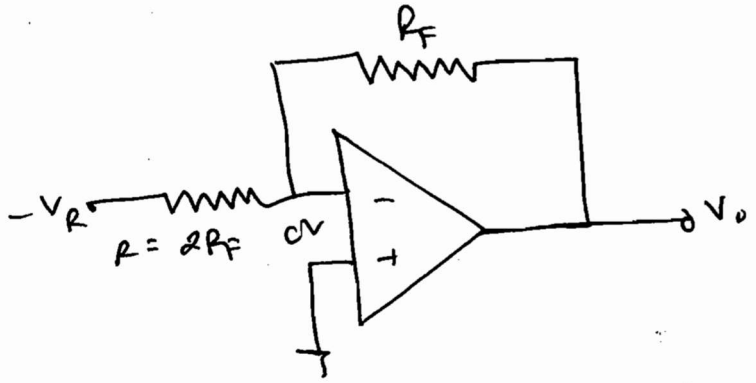
CLK	Counter	V (V)
0	0 0 0	0
1	1 0 0	4
2	1 1 0	6
3	1 1 1	7
4	0 1 1	3
5	0 0 1	1
6	0 0 0	0



(1) Binary Weighted Resistor DAC:



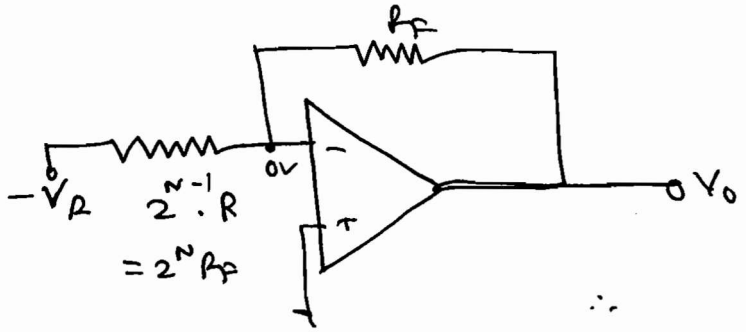
① Let, $a_{N-1} = 1$; other Input bits = 0 $\Rightarrow V_0 = ?$



$$\therefore \quad V_0 = (-V_R)\left(-\frac{R_F}{2R_F}\right)$$

$$\therefore \boxed{V_0 = +\frac{V_R}{2}}$$

② Let $a_0 = 1$; other Input bits = 0 ⇒ $V_0 = ?$



$$V_0 = (-V_R)\left(-\frac{R_F}{2^N \cdot R_F}\right)$$

$$\therefore \boxed{V_0 = \frac{V_R}{2^N}} \text{ Volts.}$$

Resolution = stepsize.

Disadvantages:

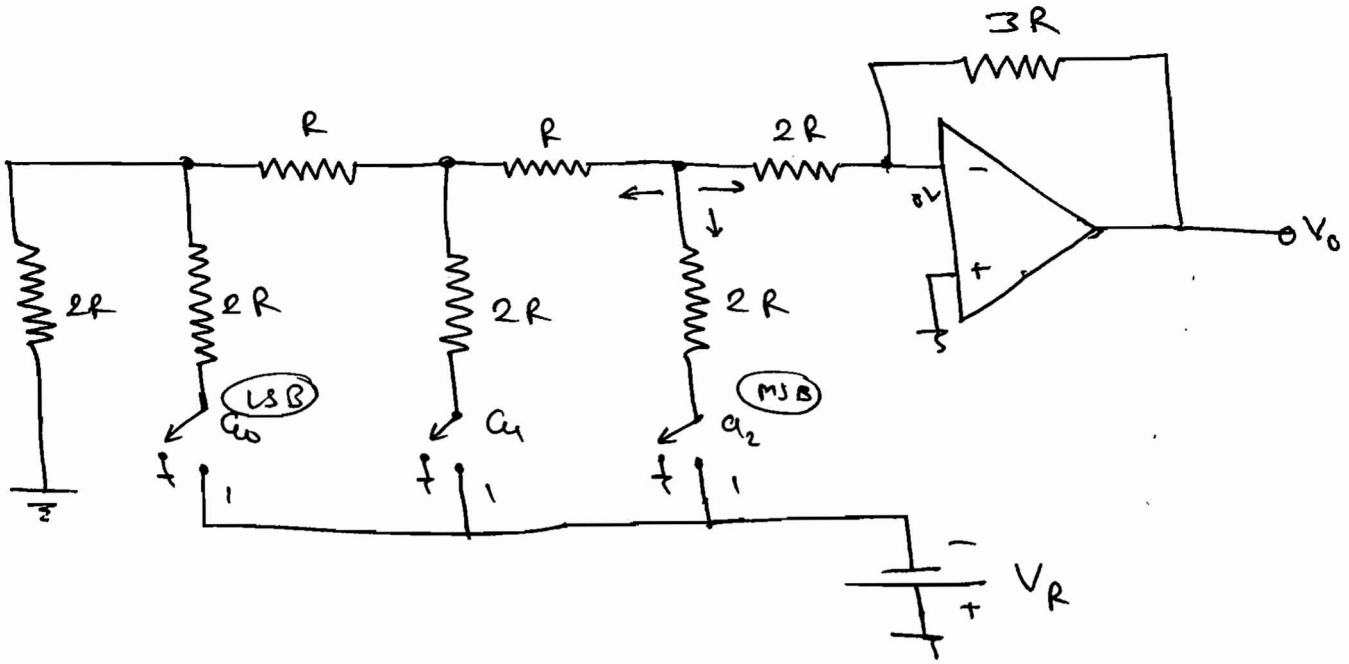
① It requires wide range of resistors.

② Using this DAC the stepsize may not be constant because it is difficult to maintain the ratio of two consecutive resistor equal to constant practically.

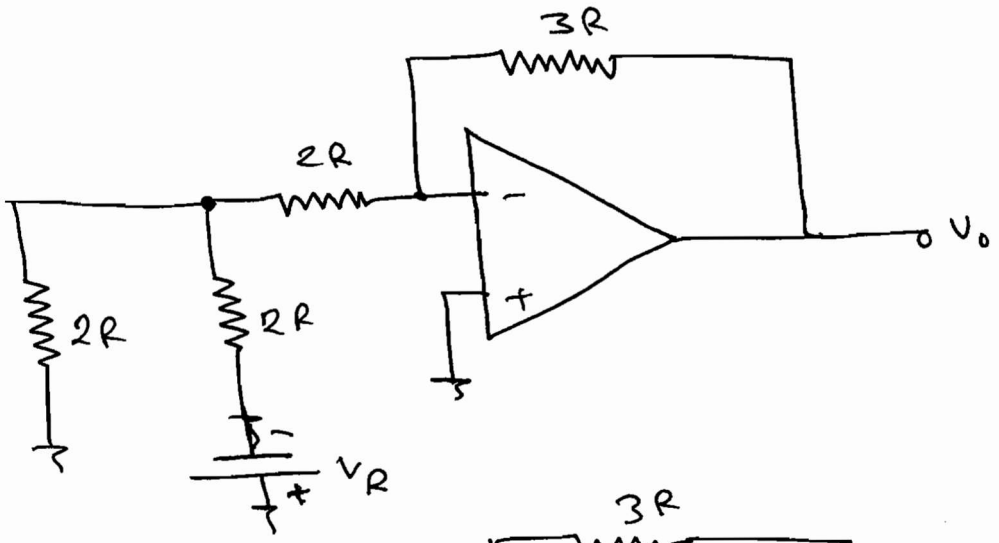
In general,

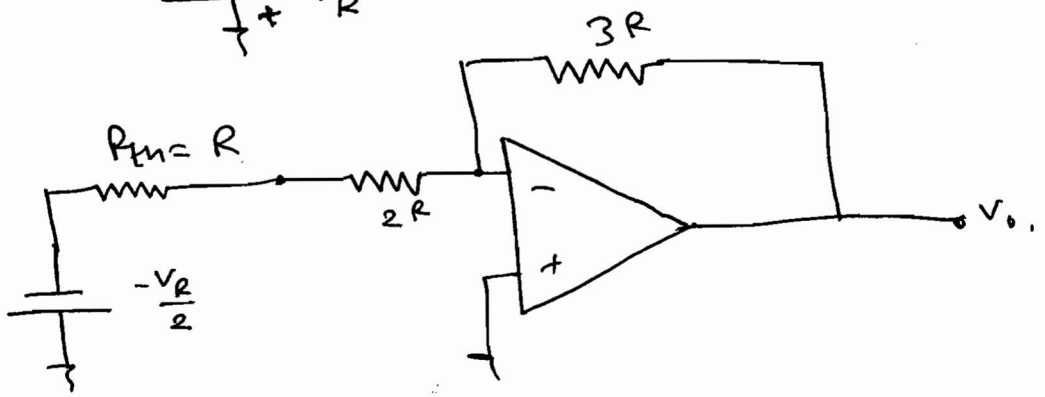
$$\therefore \boxed{V_0 = V_R\left[\frac{a_0}{2^N} + \frac{a_1}{2^{N-1}} + \cdots + \frac{a_{N-1}}{2}\right].}$$

(2) 2-Bit R-2R Ladder DAC (Voltage Switched)



(1) Let $a_2 = 1$; $a_1 = a_0 = 0$ $\Rightarrow V_0 = ?$

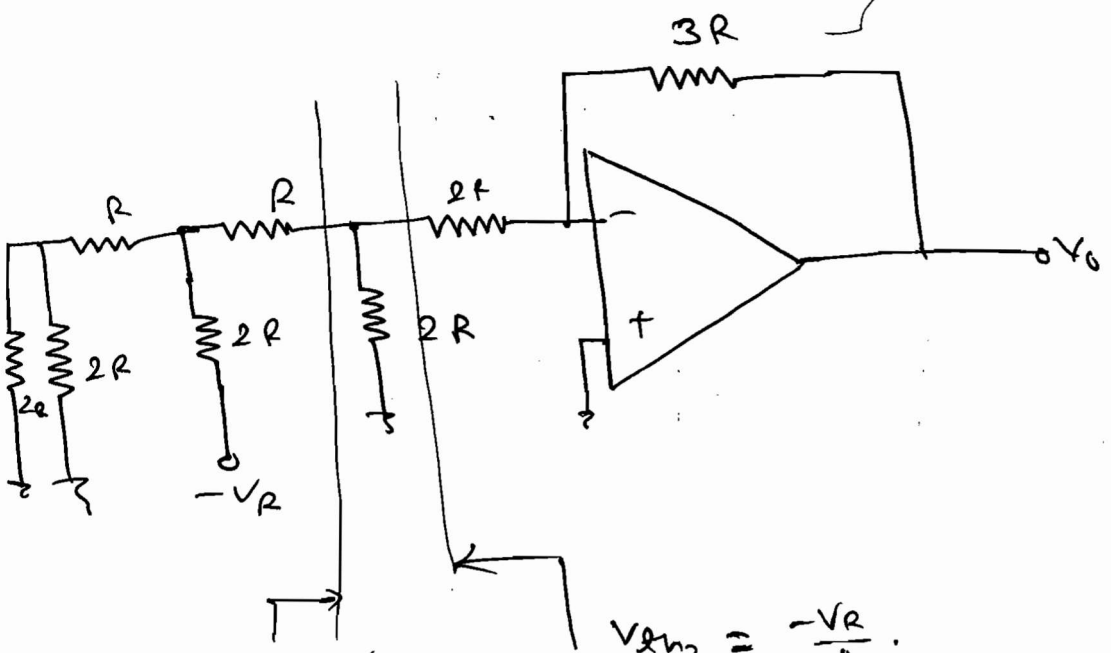




$$\therefore \quad V_0 = \left(-\frac{V_R}{2}\right)\left(-\frac{3R}{3R}\right).$$

$$\therefore \boxed{V_0 = \frac{V_R}{2}}$$

② Let $a_1 = 1$ } $a_2 = a_0 = 0 \rightarrow V_0 = ?$

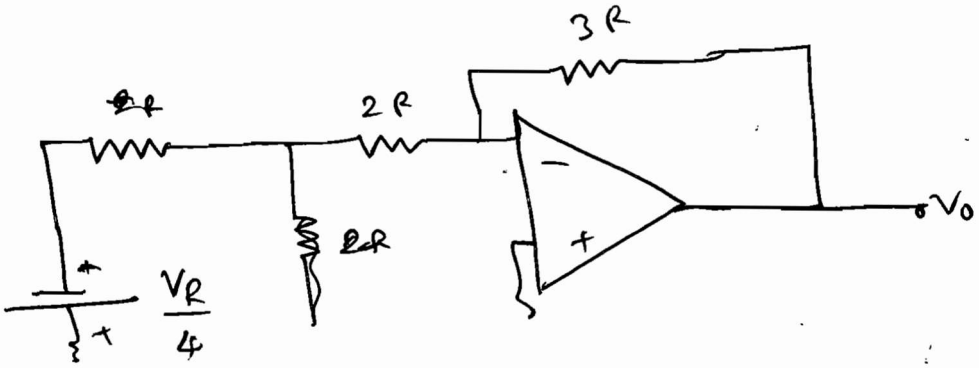


$V_{th_1} = -\frac{V_R}{2}$.

$R_{th_1} = 4R$.

$V_{th_2} = -\frac{V_R}{4}$.

$R_{th_2} = 2R$.



$$\therefore \quad V_0 = \left(-\frac{V_R}{4}\right)\left(-\frac{3R}{3R}\right).$$

$$\therefore \quad \boxed{V_0 = \frac{V_R}{4}}.$$

$$\therefore \quad \boxed{V_0 = \left[\frac{a_2}{2} + \frac{a_1}{4} + \frac{a_0}{8}\right] V_R}$$

a_2 → MSB, a_0 → LSB

① FSO

V_o = FSO when $a_2 = a_1 = a_0 = 1$

i.e. FSO = $\frac{V_R}{2} + \frac{V_R}{4} + \frac{V_R}{8} = \frac{7V_R}{8}$

$= V_R - \frac{V_R}{8}$.

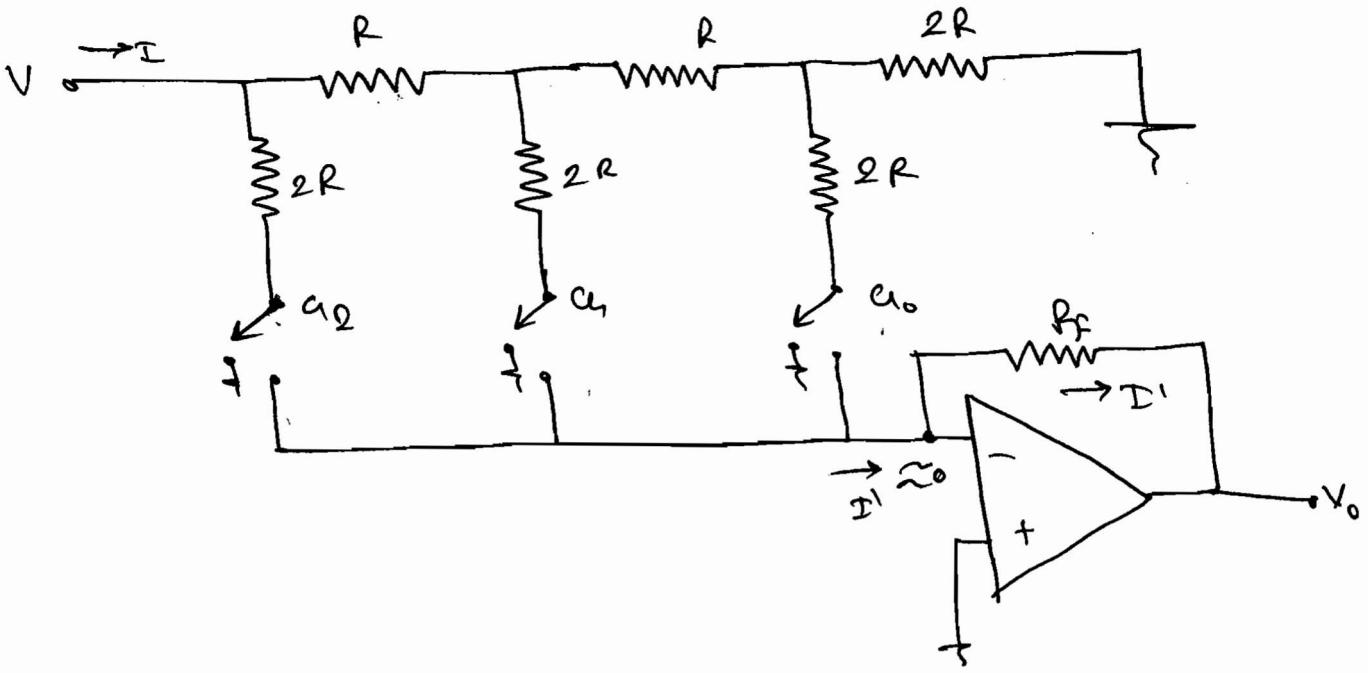
FSO = V_R − weight of LSB.

∴ ② Stepsize = Resolution = $\frac{a_0}{8} V_R = \frac{V_R}{8}$.

* Disadvantage of voltage switched Ladder DAC is: it produces unwanted spikes at the input while switching. To overcome this we use current switched DAC.

(3) 3-Bit R-2R Ladder DAC (Current Switched).

⇒



→ Duty of Op-Amp:

→ It is acting as Current to Voltage Amp.

→ $I = \frac{V}{R_{eq}} = \frac{V}{R}$ → (1)

$V_0 = -I' R_f$ → (2)

P) Let $V = 10V$. ∴ $R = 1k\Omega$. ~~$2R = R_f$~~

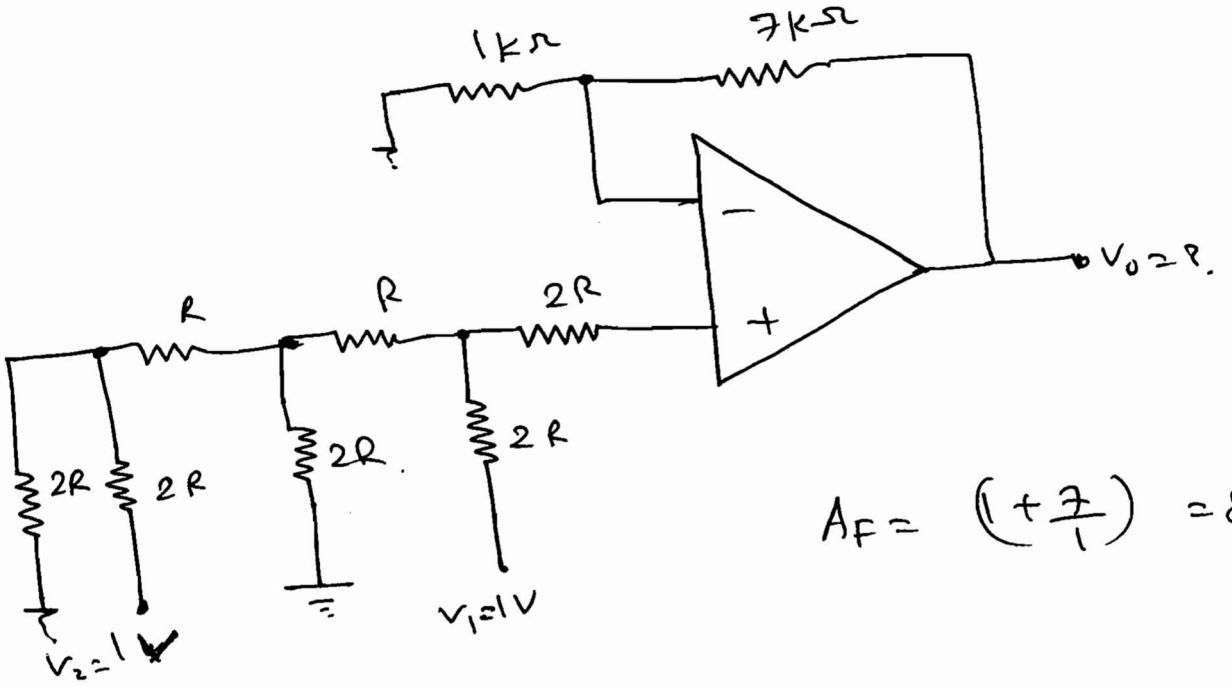
Dig. I/P $a_2 a_1 a_0 = 101$ ⇒ Analog O/P = ?

∴ $I = \frac{V}{R} = 10mA$.

∴ $I' = \frac{I}{2} + \frac{I}{8} = 10\left[\frac{1}{2} + \frac{1}{8}\right] = \frac{5 \times 10}{8} = \frac{25}{4}$.

∴ $V_0 = -\frac{25}{4} \cdot (1)$.

P-2) Determine the O/P of the following Ckt.45



$$A_F = \left(1 + \frac{7}{1}\right) = 8.$$

$$\therefore \quad V_0 = A_F\left(\frac{1}{8} + \frac{1}{2}\right).$$

$$V_0 = 8 \times \frac{5}{8}$$

$$\therefore \boxed{V_0 = 5V}$$

$\therefore$ Contribution of V_1 at Input $= \frac{V_R}{2} = \frac{1}{2}.$

" " V_2 at Input $= \frac{V_R}{8} = 1/8.$

$\therefore$ output = Input x Gain

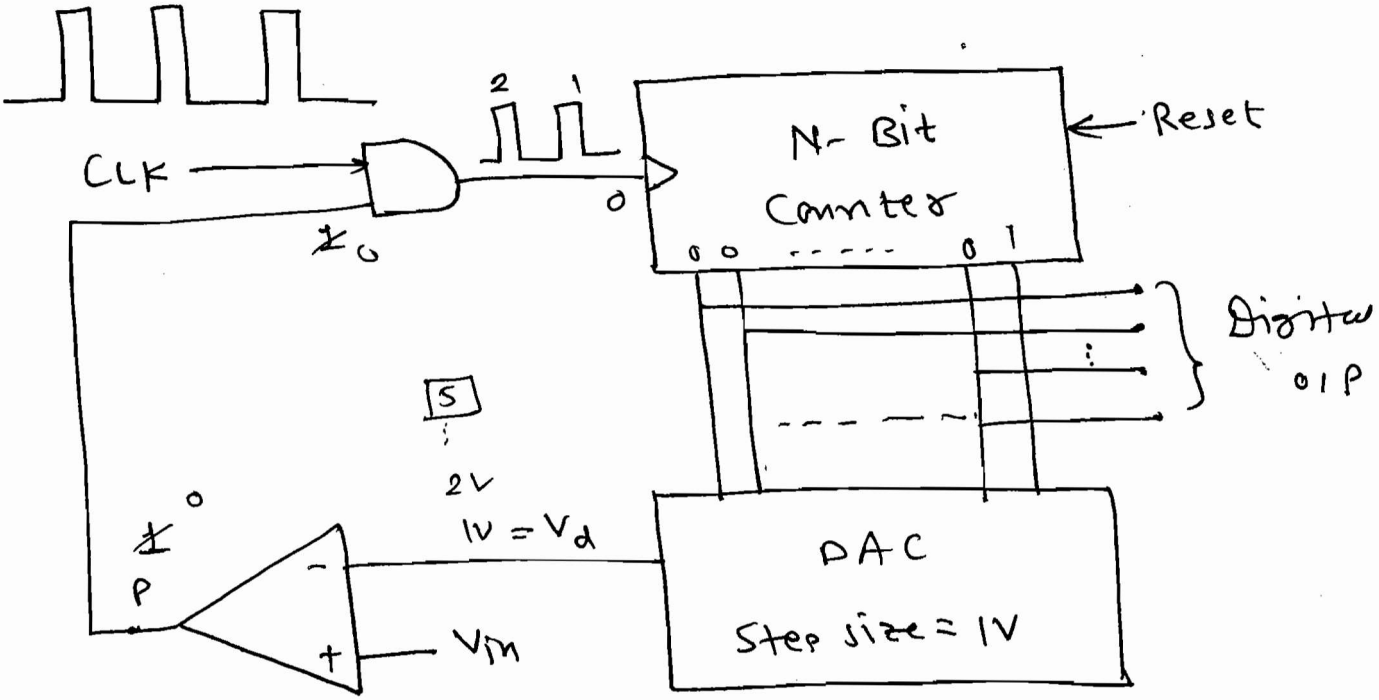
$$= \left[\frac{1}{2} + \frac{1}{8}\right] \times 8.$$

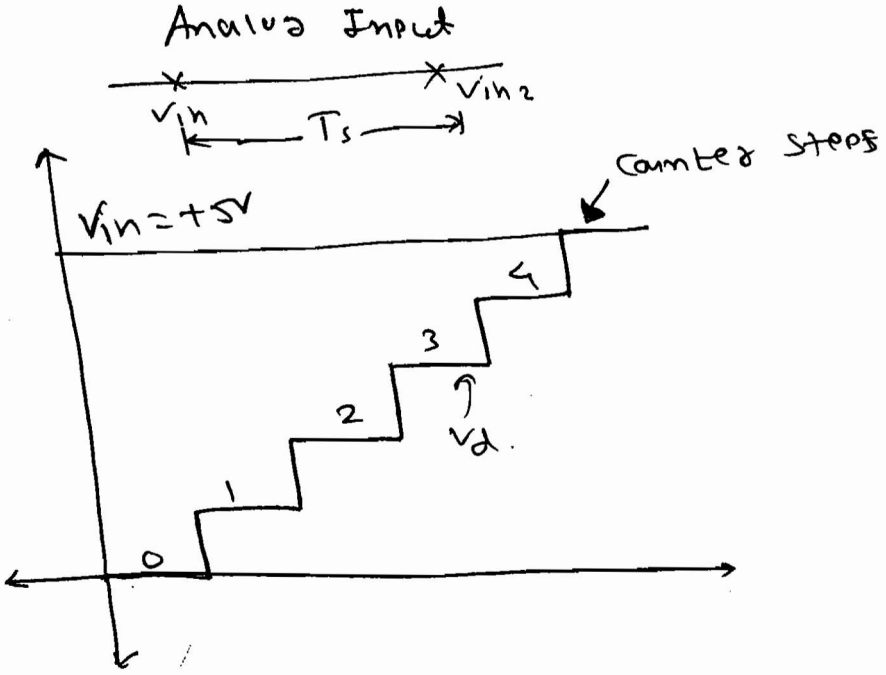
$$= 8 \frac{5}{8} \times 8$$

$$\therefore \boxed{V_0 = 5V}$$

* Analog to Digital Converter:

(1) Counter Type ADC:





→ Value of Counter = (ceiling ~~Voltage~~ value (Input voltage / step size).

* Two Features

① Conversion time depends on the input magnitude.

② Maximum Conversion time.

$$= \underline{\underline{2^N - 1}}.$$

Sampling period :

$$T_s \geq \text{max Conv. time.}$$

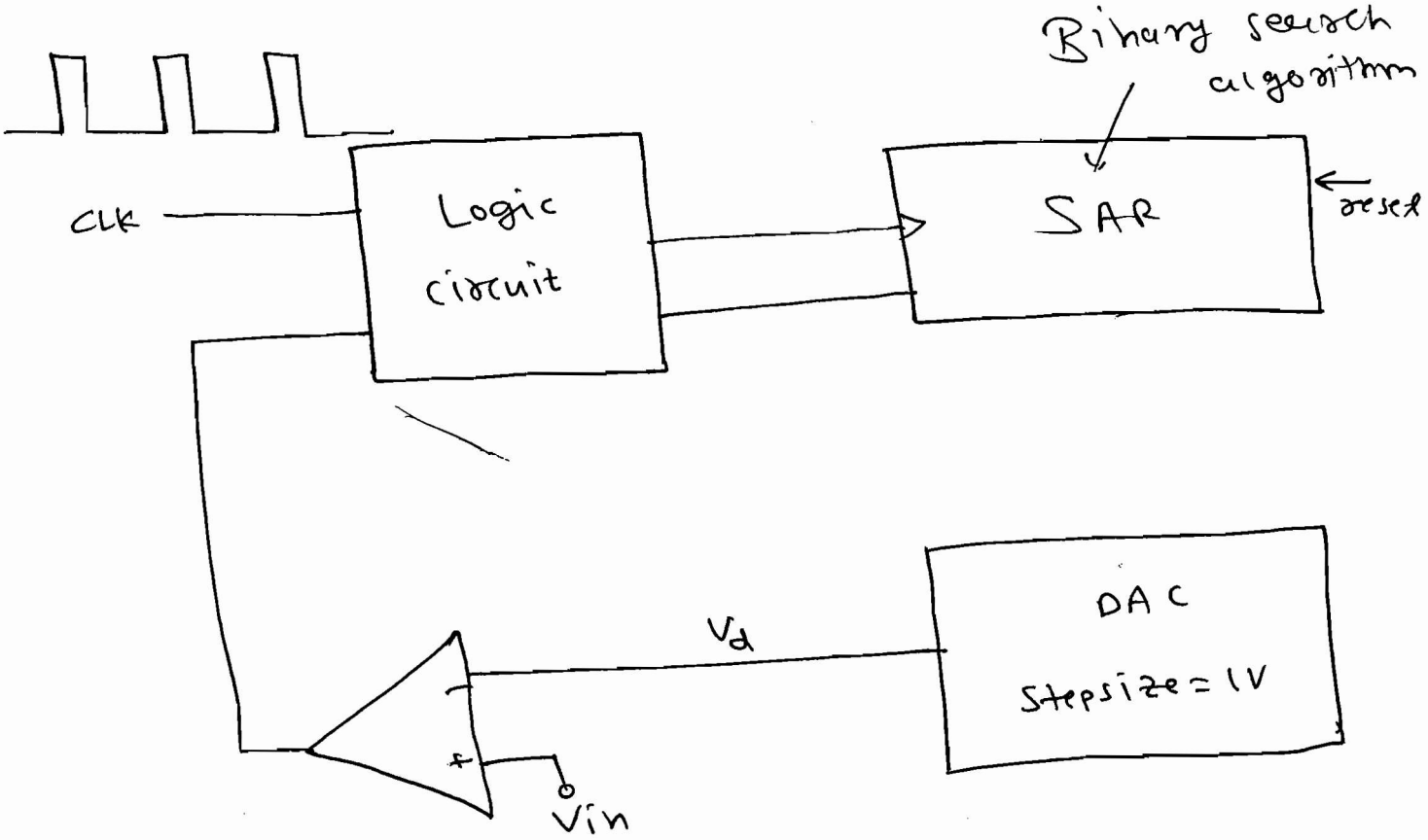
i.e $\boxed{T_s \geq (2^N - 1)\, T}$

Sampling rate $f_s \uparrow = \frac{1}{T_s \downarrow} = \frac{1}{(2^N - 1)\, T}$ Hz.

NOTE:

→ In Counter type A to D converter the conversion time doubles for every 1 bit increase in size.

② Successive Approxi ADC:



→ $V_d > V_{in} \Rightarrow V_d \downarrow \Rightarrow$ SAR ↓.

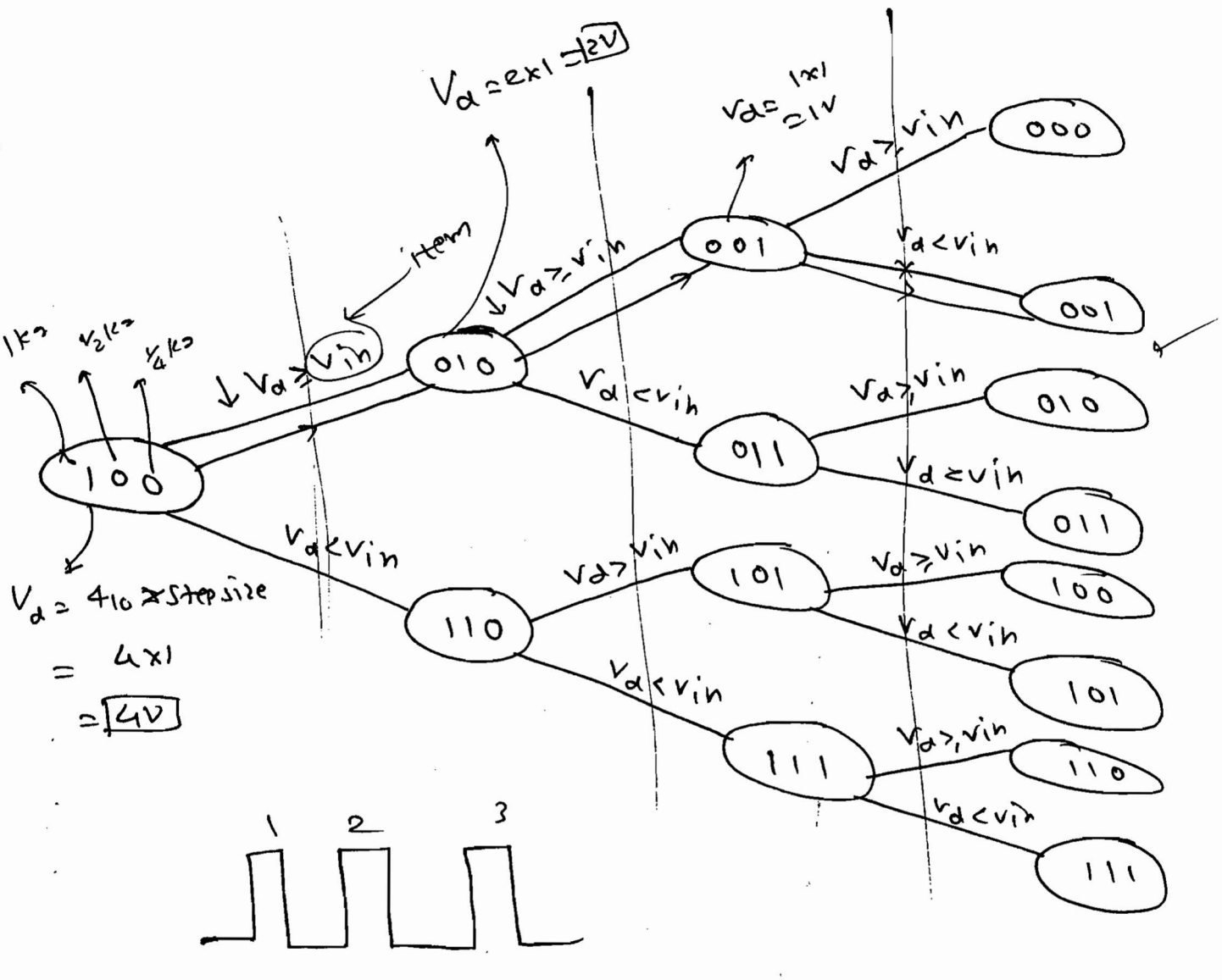
→ $V_d < V_{in} \Rightarrow V_d \uparrow \Rightarrow$ SAR ↑.

$V_d > V_{in} \Rightarrow P=0.$

$V_d = V_{in} \Rightarrow P=0$

$V_d < V_{in} \Rightarrow P=1.$

* 3 - Bit SAR



Time = 3T.

→ In successive approximation AtoD converter the digital O/P is always less than the analog input.

P) $V_{in} = 2V$. $V_d = 4V$.

DAC stepsize = 1V.

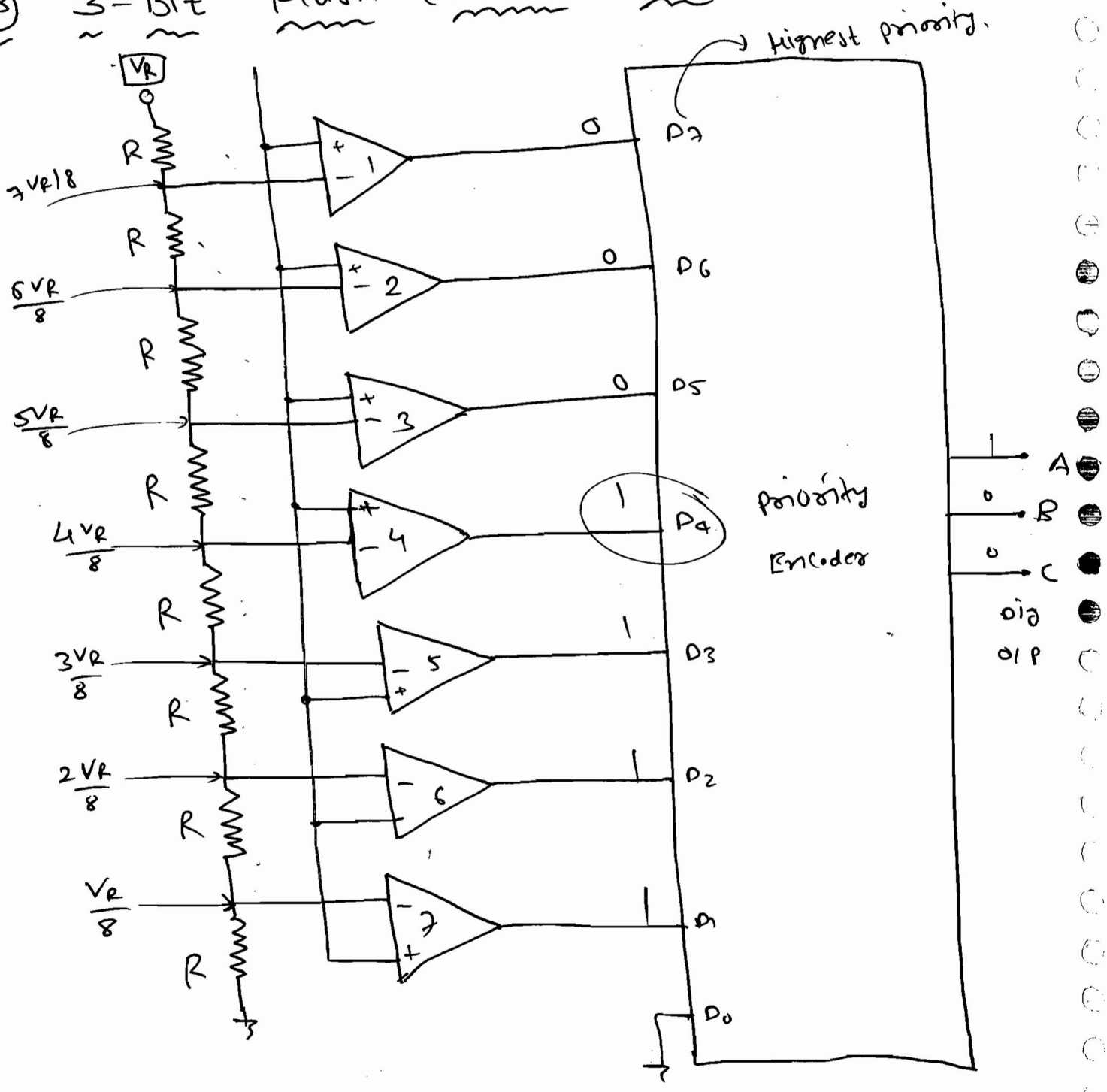
Dig output = 001.

→ In successive approximation ADC,

① conversion time doesn't depend on input magnitude.

② Maximum conversion time = NT.

③ 3-Bit Flash (parallel) ADC:



V_{in}	D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	outputs A B C
(4) $\frac{4V_R}{8} \le V_{in} \le \frac{5V_R}{8}$	0 0 0 1 1 1 1 0	1 0 0
(3) $\frac{3V_R}{8} \le V_{in} \le \frac{4V_R}{8}$	0 0 0 0 0 1 1 0	0 1 0

→ In flash time ADC

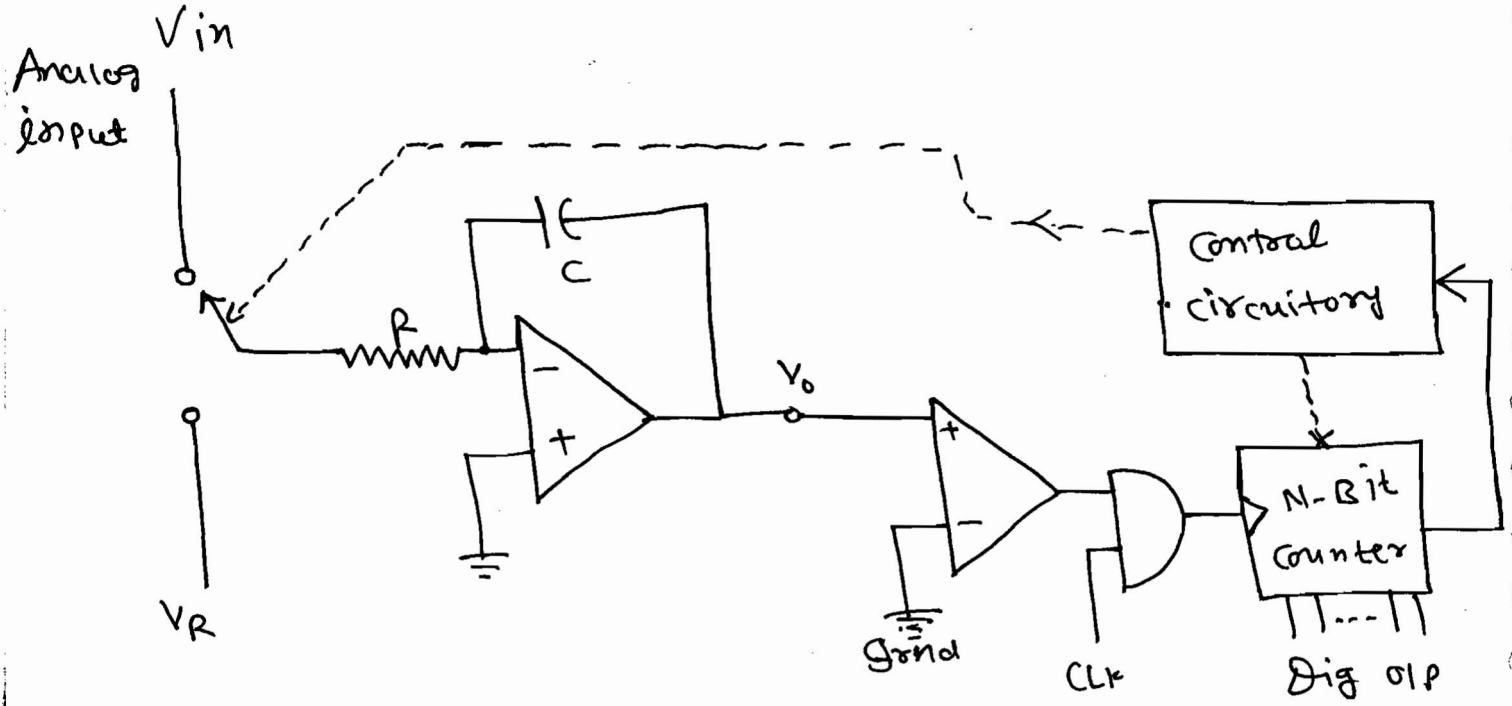
① Conversion time doesn't depend on input magnitude.

② Maximum conversion time is very less it deeem and hence it is the fastest ADC.

* Disadvantage

→ N-Bit flash ADC requires $(2^N - 1)$ Comparators.

(4) Dual slope (or) Integrating ADC:



* V_{in}, V_R polarities must be opposite.

1) $V_o > 0$ ⇒ CLCK Pulses reach the Counter.

2) $V_o \leq 0$ ⇒ Counter Stops.

2) $V_o = \frac{-1}{RC} \int v\,dt$.

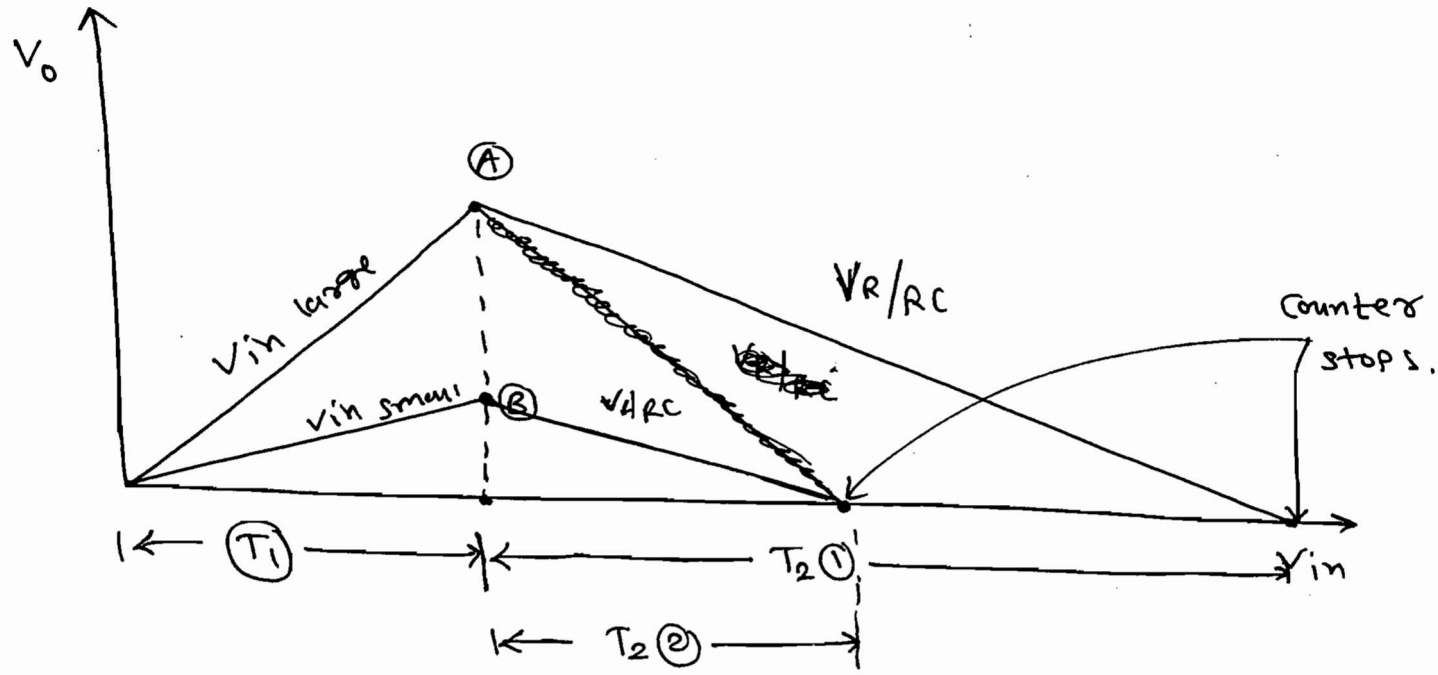
If V is constant

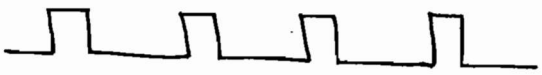
$\therefore$ $\boxed{V_o = -\frac{V}{RC} \cdot t}$

3) Control circuitary.

→ For fixed time "T_1" ⇒ { "S" ⟶ V_{in}" and Counter is Reset

(b) After "T_1" $\Rightarrow$ { "S $\longrightarrow$ V_A" and Counter is started.



CLOCK:  $\Rightarrow T = 2\ \mu s$.

T_2 ① : 100μs. $\rightarrow$ Counter value: $\frac{100}{2} = 50$, 50 CP require

T_2 ② : 20μs. $\rightarrow$ Counter value: $\frac{20}{2} = 10$, 20 CP require.

If clock Period = 2μs.

Case-(i) Value of Counter = $\frac{100}{2} = 50 = (000\ldots110010)_2$.

Case-(ii) Value of Counter = $\frac{20}{2} = 10$

$= (000\ldots1010)_2$.

* Discharging time "T_2".

Voltage change during T_1 = Voltage change during "T_2".

$$\therefore \boxed{T_2 = \frac{|V_{in}| T_1}{|V_R|}}$$

* Advantages:

① It is very accurate because the same capacitor is used for charging and discharging. so, that if any deviation exist the system will not be affected. Hence, it is used in all digital voltmeters.

② The integrator at the input eliminates the effect of power supply noise called as "50 Hz hum" (interferance).

* Disadvantage:

→ It is speed of operation is very less.

In,
⇒ Dual slope ADC,

(i) Conversion time depends on input magnitude,

(ii) Max. conversion time

$$\therefore \boxed{T_{max} = T_1 + \left(2^N - 1\right) T}$$

N = size of ADC (No. of bits).

But, $T_{1,max} = (2^N - 1)\,T$.

$\therefore T_{max} = (2^N - 1)\,T + (2^N - 1)\,T$

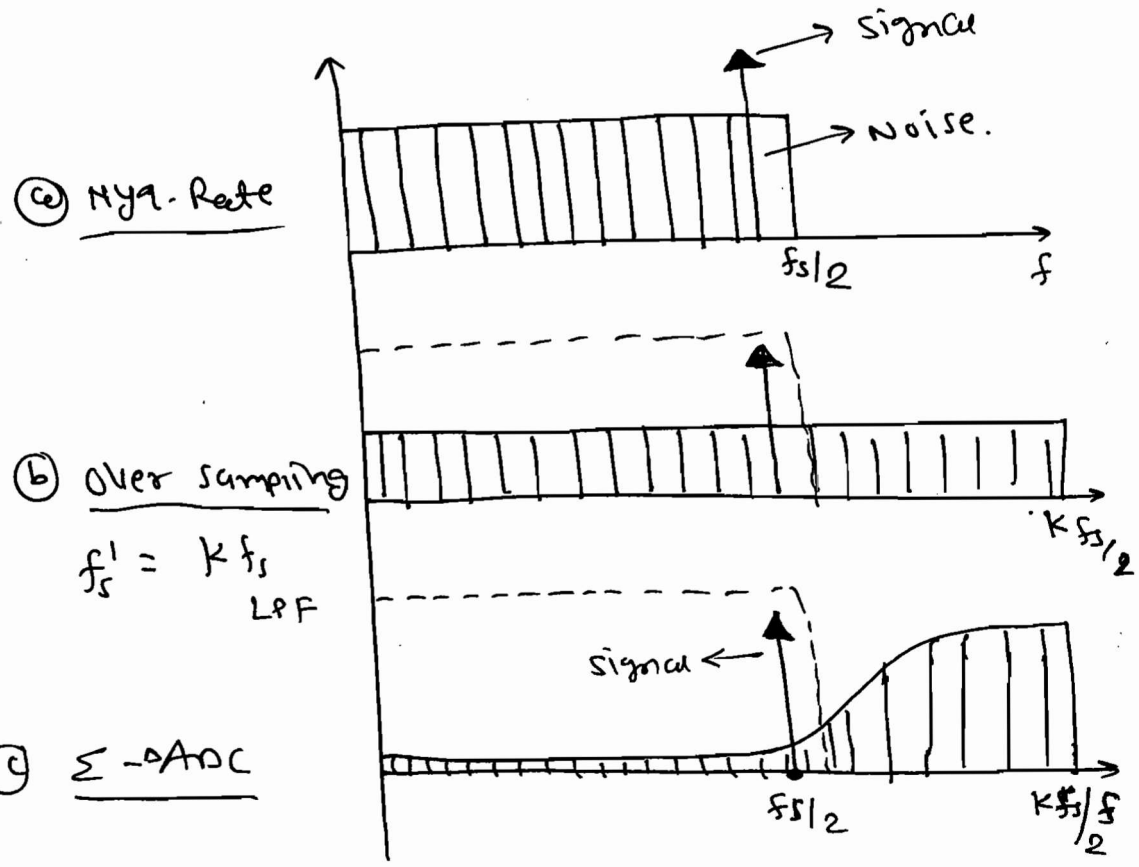
$\therefore \boxed{T_{max} \approx 2^{N+1} \cdot T}$

→ In Dual slop ADC the conversion time doubles for every 1 bit increase in size.

5) Σ-Δ ADC (Sigma-Delta ADC).

↳ 1 Bit DPCM.

Concept:

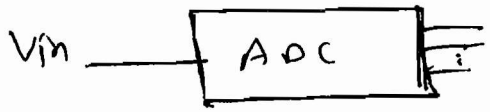


In Σ-Δ ADC

signal → LPF $\left(\frac{1}{s+1}\right)$.

* Resolution of ADC:

→ It is the minimum change required at the input to obtained 1-Bit change at the output.



0V ⟶ 000 --- 000

Resolution 10mv ⟶ 000 .... 00.

15mv ⟶ 000 ---01.

$$\text{Resolution} = \frac{\text{Input Voltage Range}}{(2^N - 1)}$$

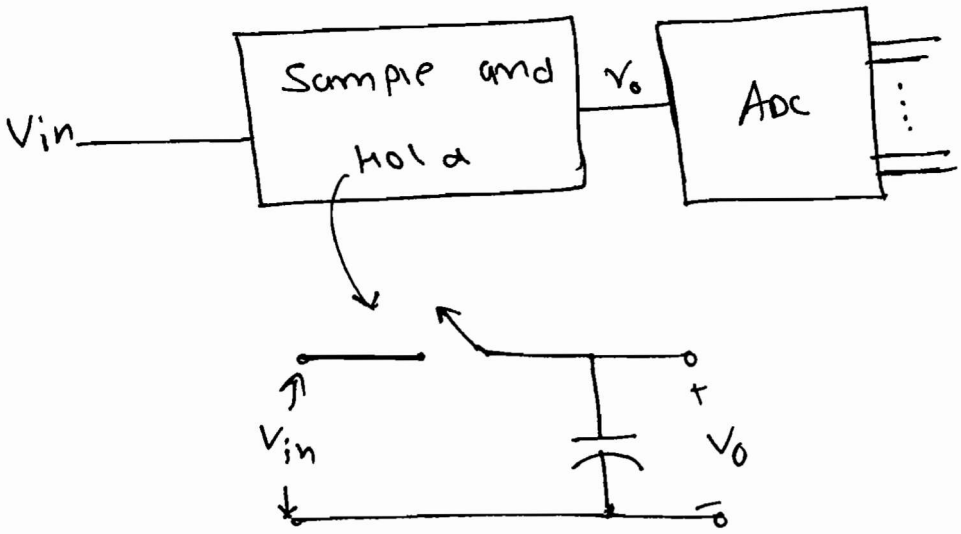
* For Proper ADC operation.

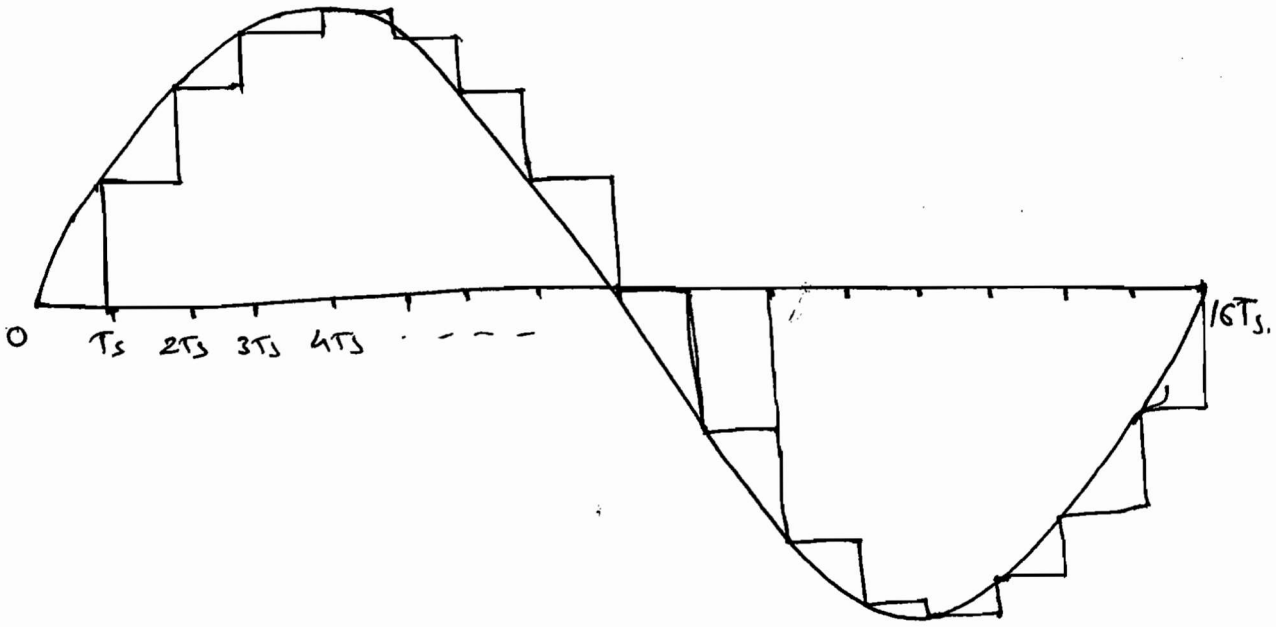
⇒ Ripple voltage at Input < Resolution of ADC.

* Continous signal can't be Apply to the ADC. ADC can not convert continous analog signal into digital signal directly. we require some circuity for that. i.e. Sample and Hold Ckt.

*

→





→ Acquisition time:

→ It is the time taken for the switch to close and capacitor charge to the input voltage.

→ Aperture time:

Ex-9 Page-29 CR

→ $T_1 = 300ms$ $V_R = 100mV$

$T_2 = 370.2ms$

$\therefore |V_{in}|T_1 = |V_R| T_2$

$\therefore V_{in} = \frac{370.2}{300} \times 100mV$

$$\boxed{V_{in} = 123.4 mV}$$

Q-10

Hint: In ADC,

Quantization error $= \pm \frac{\text{stepsize}}{2}$

$\text{Stepsize} = \frac{1.275}{2^{8-1}} = 5mV.$

$\therefore$ Quantization error $= \pm \frac{5}{2}$

$= \pm 2.5 mV.$

Q-11 Maximum Conversion time

$T_{max} = 2^{N+1} \cdot T$

$= 2^{11} \cdot 1\mu s$

$T_{max} = 2048 \mu s.$

$\therefore T_s \geq T_{max}.$

$\therefore T_s = 2048 \mu s.$

$\therefore$ $\boxed{f_s \leq 500\ Hz.}$

Let, $\boxed{f_s = 500\ Hz.}$

$\therefore$ Input BW $= \frac{f_s}{2}$

$= \frac{500}{2}$

$\therefore$ $\boxed{BW = 250\ Hz.}$

Q-5

$FSO = (2^N - 1) \times \text{Stepsize}.$

$\therefore 20 = (2^8 - 1) \times \text{Stepsize}.$

$\therefore$ Stepsize $= \frac{20}{255}$ volts.

$\therefore V_{in} = (219)_{10} \times \frac{20}{255}$

$\therefore$ $\boxed{V_{in} = 17.1\ V}$

Q-3

8-bit ADC $\rightarrow$ 0-5V.

0V $\longrightarrow$ 0000 0000 = 00H.

$\vdots$

2.5V $\longrightarrow$ 1000 0000 = 80H

$\vdots$

5V $\longrightarrow$ 1111 1111 = FFH.

P) 8-bit ADC $\rightarrow$ -5 to +5

-5 $\longrightarrow$ 0000 0000 = 00H.

$\vdots$

0 $\longrightarrow$ 1000 0000 = 80H