1 Intel 8085 and Intel 8086

Multiple Choice Questions

Q.1 INTEL 8085 is
(a) 16 bit microprocessor
(b) 32 bit microprocessor
(c) 8 bit microprocessor
(d) 4 bit microprocessor

Q.2 In an 8 bit microcomputer, maximum memory can be connected is 32 K bytes, the length of stack pointer, program counter and number of data lines are respectively
(a) 16, 16, 8 (b) 15, 16, 7
(c) 15, 15, 8 (d) 16, 15, 8

Q.3 For the purpose of data processing an efficient assembly language programmer makes use of the general purpose registers rather than memory. The reason is
(a) The set of instruction for data processing with memory is limited
(b) Data processing becomes easier when register are used
(c) More memory related instructions are required in the program for data processing
(d) Data processing with registers takes fewer cycles than that with memory
[IES-2011]

Q.4 Consider the following statements in 8085 microprocessor data-bus and address bus are multiplexed in order to
1. Increase the speed of microprocessor
2. Reduce the number of pins
3. Connect more peripheral chips

Which of these statements is/are correct ?
(a) 1 only (b) 2 only
(c) 2 and 3 (d) 1, 2 and 3
[IES-2009]

Q.5 The content of the program counter of an 8085 microprocessor is
(a) The total number of instructions in the program already executed
(b) The total number of times a subroutine is called
(c) The memory address of the instruction that is being currently executed
(d) The memory address of the instruction that is to be executed next.
[IES-2010]

Q.6 In an INTEL 8085A microprocessor, why is READY signal used?
(a) To indicate to user that the microprocessor is working and is ready for use
(b) To provide proper WAIT states when the microprocessor is communicating with a slow peripheral device
(c) To slow down a fast peripheral device so as to communicate at the microprocessors device
(d) None of the above **[IES 2008]**

Q.7 In DMA operation, the processor is interfered more in
(a) Cycle stealing technique
(b) Burst mode
(c) Interleaved DMA
(d) None

Q.8 In an 8085 microprocessor, the shift registers which store the result of an addition and the overflow bit are, respectively
(a) B and F (b) A and F
(c) H and F (d) A and C

Q.9 After an arithmetic operation, the flag register of a 8085 microprocessor has the following look :

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	X	1	X	0	X	1

The arithmetic operation has resulted in
(a) A carry and odd parity number having 1 as the MSB
(b) Zero and the auxiliary carry flag being set
(c) A number with even parity and 1 as the MSB
(d) A number with odd parity and 0 as the MSB
[IES-2003]

Q.10 The number of output pins of a 8085 microprocessor are
(a) 40 (b) 27
(c) 21 (d) 19
[IES-2002]

Q.11 Match **List-I(Interrupt)** with **List-II (Property)** and select the correct answer using the code given below the lists:

List-I	List-II
A. RST 7.5	1. Non-maskable
B. RST 5.5	2. Edge sensitive
C. INTR	3. Level sensitive
D. TRAP	4. Non-vectored

Codes :

	A	B	C	D
(a)	1	3	4	2
(b)	2	4	3	1
(c)	1	4	3	2
(d)	2	3	4	1

Q.12 $\overline{\text{INTA}}$ is requried only for
(a) RST 5.5 & RST 6.5
(b) RST 7.5
(c) INTR
(d) TRAP

Q.13 Output of the assembler in machine codes is referred to as
(a) Object program
(b) Source program
(c) Macro instruction
(d) Symbolic addressing **[IES-2003]**

Q.14 The correct sequence of steps in the instruction cycle of a basic computer is
(a) Fetch, Execute, Decode and Read effective address
(b) Read effective address, Decode, Fetch and Execute
(c) Fetch, Decode, Read effective address and Execute
(d) Fetch, Read effective address, Decode and Execute
[IES-2012]

Q.15 Which one of the following cycle is required to fetch and execute an instruction in a 8085 microprocessor ?
(a) Clock cycle (b) Memory cycle
(c) Machine cycle (d) Instruction cycle

Q.16 With referennce to 8085 microprocessor, which of the following statements are correct?
1. INR is 1 byte instruction
2. OUT is 2 byte instruction
3. STA is 3 byte instruction

(a) 1 and 2 only (b) 2 and 3 only
(c) 1 and 3 only (d) 1, 2 and 3

Q.17 For INTEL 8085, match **List-I(Addressing Mode)** with **List-II (Instruction)** and select the correct answer using the code given below the lists:

List-I	List-II
A. Implicit addressing	1. JMP 3FAD H
B. Register-Indirect	2. MOV A, M
C. Immediate	3. LDA 03FC H
D. Direct addressing	4. RAL

Codes:

	A	B	C	D
(a)	4	1	2	3
(b)	4	2	1	3
(c)	3	2	1	4
(d)	3	1	2	4
[IES-2004]

Q.18 Which of the following statements is/are correct?
In INTEL 8085 the interrupt enable flip-flop can be reset by
(*i*) DI instruction.
(*ii*) System RESET.
(*iii*) Interrupt acknowledgment.
(*iv*) SIM instruction.
(a) (*ii*), (*iii*) and (*iv*)
(b) (*ii*) and (*iv*)
(c) (*i*), (*ii*) and (*iii*)
(d) All of these

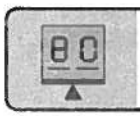
Q.19 Content of accumulator is 8E H, If SIM instruction is executed, the which of the following statement is true
(a) Serial output data is 1
(b) RST 6.5, 7.5 are enable
(c) RST 5.5 is enable
(d) None of these

Q.20 To have the multiprocessing capabilities of the 8086 microprocessor, the pin connected to the ground is
(a) $\overline{DEN}$ (b) ALE
(c) INTR (d) MN/$\overline{MX}$

Q.21 Effective address is calculated by adding or subtracting displacement value to
(a) immediate address
(b) relative address
(c) absolute address
(d) base address

[IES-2001]

Q.22 In 8086, CS : 907E H, IP : 0FFF H find effective or physical address
(a) 90FFF H (b) 917DF H
(c) FFF09 H (d) None



Numerical Data Type Questions

Q.23 The total number of memory access involved (inclusive of opcode fetch) when an 8085 processor executes the instruction LDA 2016 H is_____.

Q.24 If the clock frequency of a microprocessor is 5 MHz. Then the time required to execute PUSH B instruction is _____ μsec.

Q.25 Consider the execution of the following instruction by a 8085 microprocessor :
LXI H, 01FF H
SHLD 2050 H
After execution the contents of memory locations 2050 H and 2051 H and the registers H and L, will be _____H,_____H,_____H and____H respectively.

Q.26 If the accumulator of the INTEL 8085A microprocessor contians 37 H and the previous operation has set the carry flag, the instruction ACI 56 H will result _____ Hex.

Q.27 If the content of accumulator after execution of RIM is A9H, then interrupt pending is_____ and serial data received is _____.

Conventional Questions

Q.28 Draw and explain architecture and pin diagram of 8085 microprocessor.

Q.29 Draw the timing diagram of OUT 80 H instruction if [A] = 50 H and f_{CLK} = 5 MHz.

Q.30 Explain the sequence of steps involved in CALL and RETURN instruction in 8085.

Q.31 Draw and explain architecture of 8086.

Try Yourself

T1. Explain flag register in 8085 with suitable example.

T2. Explain DMA (Direct memory access) operation in 8085.

T3. The following program starts at locations 0100 H.
LXI SP, 00FF H
LXI H, 0107 H
MVI A, 20 H
SUB M
Find the content of accumulator when the program counter reaches 0109 H is.

[Ans: 00H]

■■■■