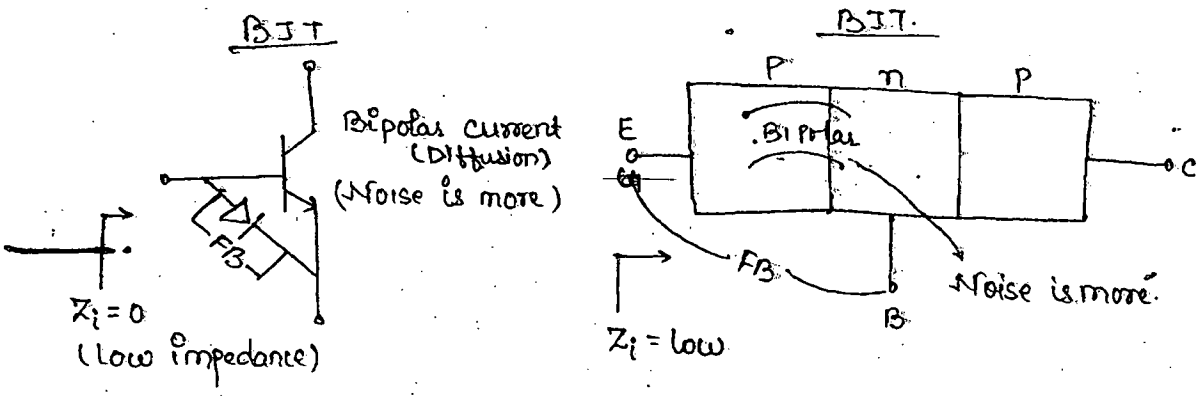
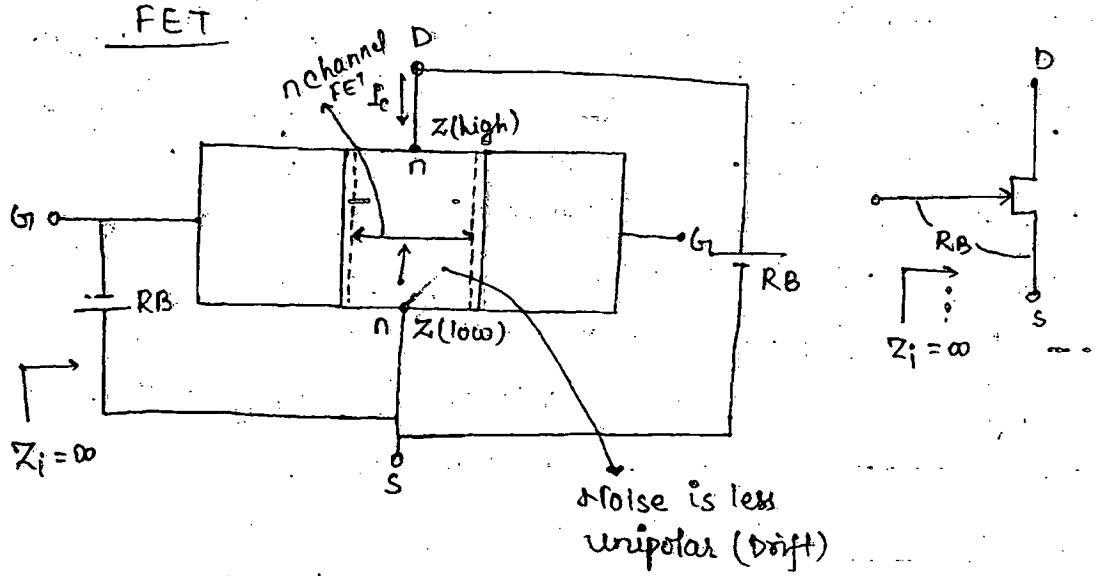
FIELD EFFECT TRANSISTORS. (FET)





INTRODUCTION :-

→ BJT is having following disadvantages :-

1. The i/p impedances is low.
2. The noise level is compairatively high because BJT is a bipolar.
3. BJT is a current controlled devices.

→ FET is having following advantages :-

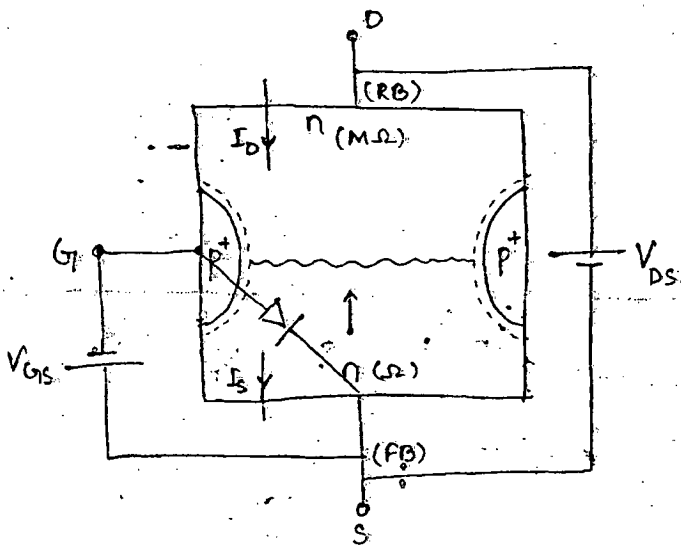
1. The i/p impedance is high.

2. The noise is comparatively less because FET is a unipolar device.

3. FET is a voltage controlled device.

03/11/14

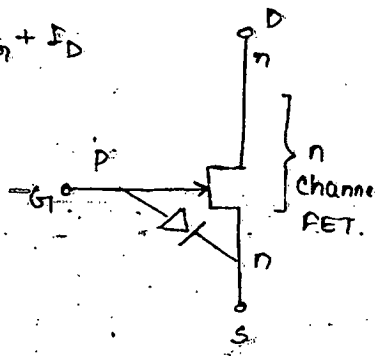
N- CHANNEL FET



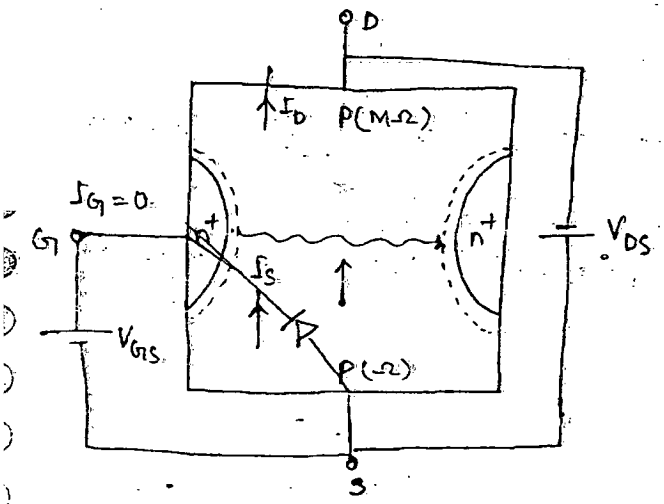
$I_g = I_G + I_D$

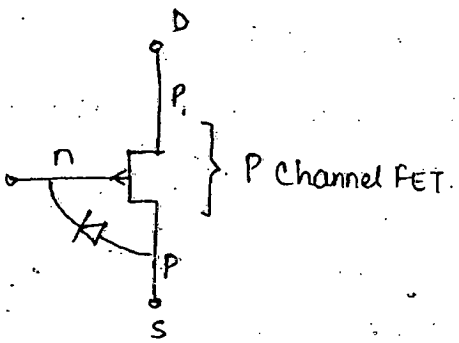
$I_G = 0$

$I_S = I_D$



P. CHANNEL FET.





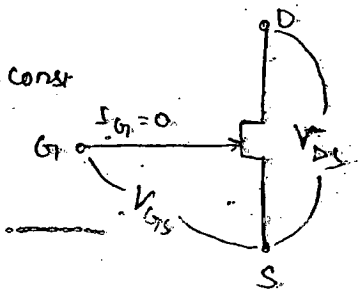
FET PARAMETER DESIGN.

1. ac drain resistance, $r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS} = \text{const}}$

2. Trans conductance, $g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS}=\text{const}}$

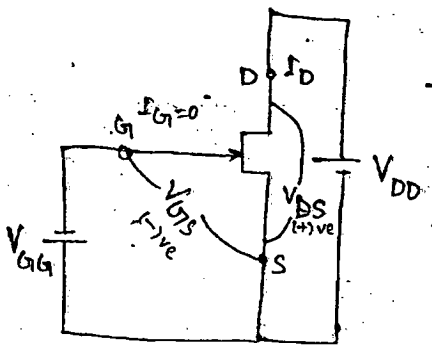
3. Amplification Ratio, $\mu = \left.\frac{\Delta V_{DS}}{\Delta V_{GS}}\right|_{I_D=\text{const}}$

$$\boxed{\mu = g_m r_d}$$



⊡ IMPORTANT POINTS IN FET.

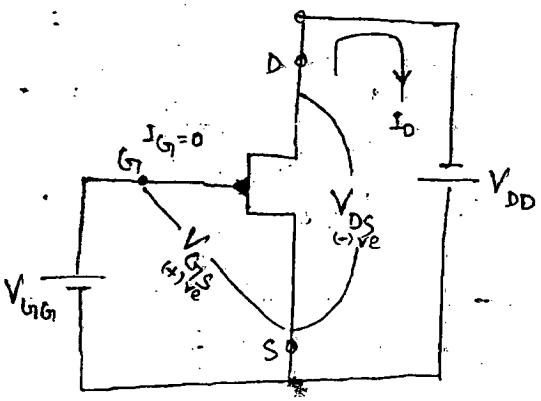
n-Channel FET



I/P parameter
V_{GS}, I_G

O/P parameter
V_{DS}, I_D

P Channel FET



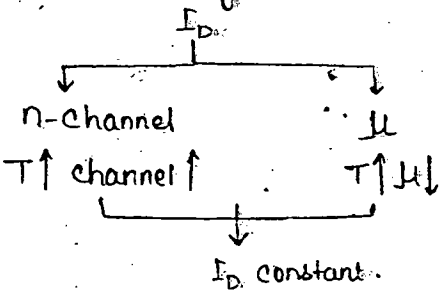
1. I_G is called as leakage current or reverse saturation current $I_G \simeq 0$.
2. There will no I/p characteristics study in FET because I/p is open device.
3. There are two graphs in FET → (i) drain characteristics V_{DS} Vs $I_D\big|_{V_{GS}=\text{constant}}$

   (ii) Transfer characteristics V_{GS} Vs $I_D\big|_{V_{DS}=\text{constant}}$
4. For FET analysis transfer characteristics are more dominant than drain characteristics.

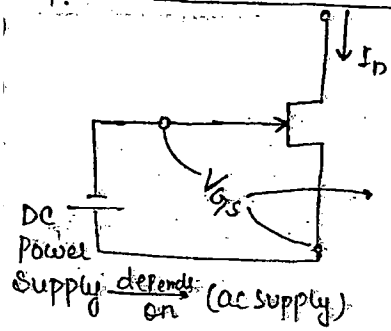
5. The Q point in FET is defined as $Q(I_{DQ}, V_{GSQ})$ → transfe graph.

6. FET is always thermally stable because I_D is independen of temperature.

Thermally stable.



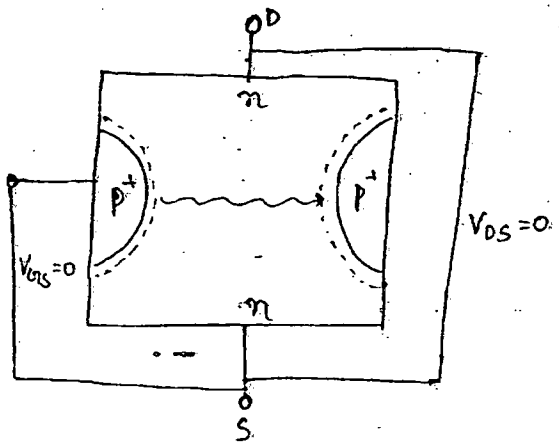
7. FET BIASING.



In FET biasing we have to fix the V_{GS} voltage independent of DC battery therefore I_D will be constant.

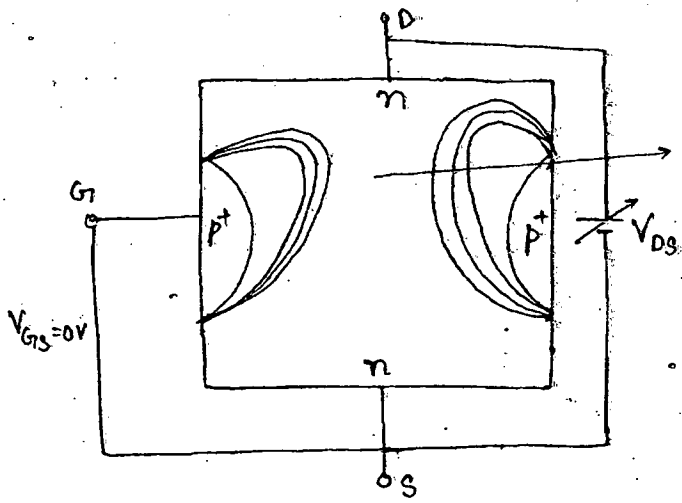
☐ WORKING PRINCIPLE OF FET.

Case I:- $V_{GS} = 0V$ & $V_{DS} = 0V$.



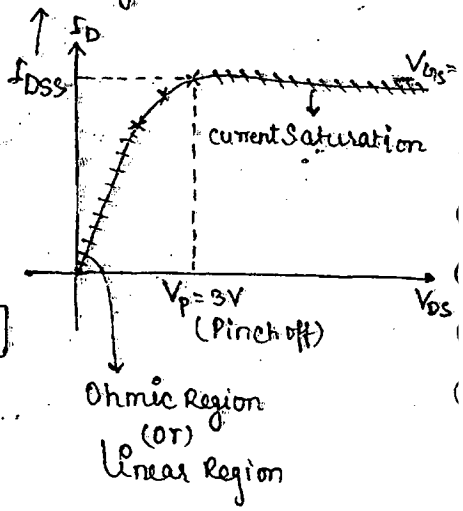
1. As $V_{GS} = 0V$ max^m channel can b formed.
2. As $V_{DS} = 0V$ the drain current I_D becomes zero.

Case i :- $V_{GS} = 0V$; $V_{DS} \neq 0V$.

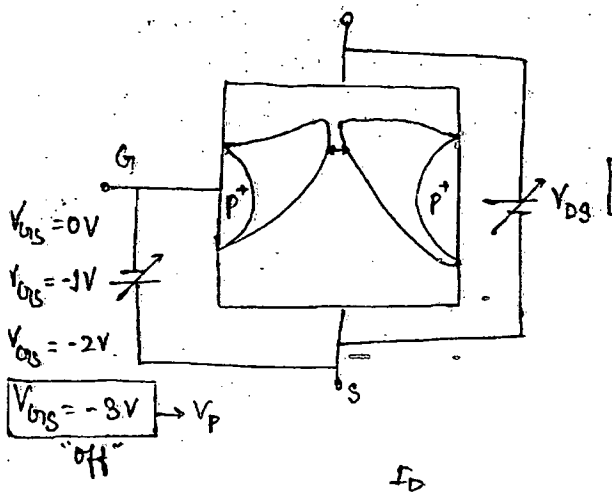


Pinch off
$V_{DS} = 1V$
$V_{DS} = 2V$
$V_{DS} = 3V$
Pinch off

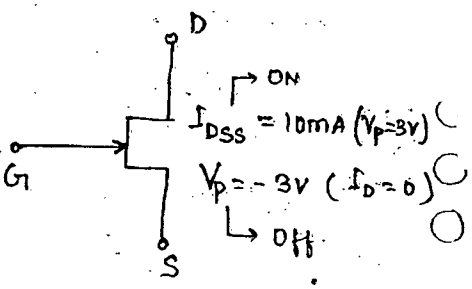
Shorted gate drain current

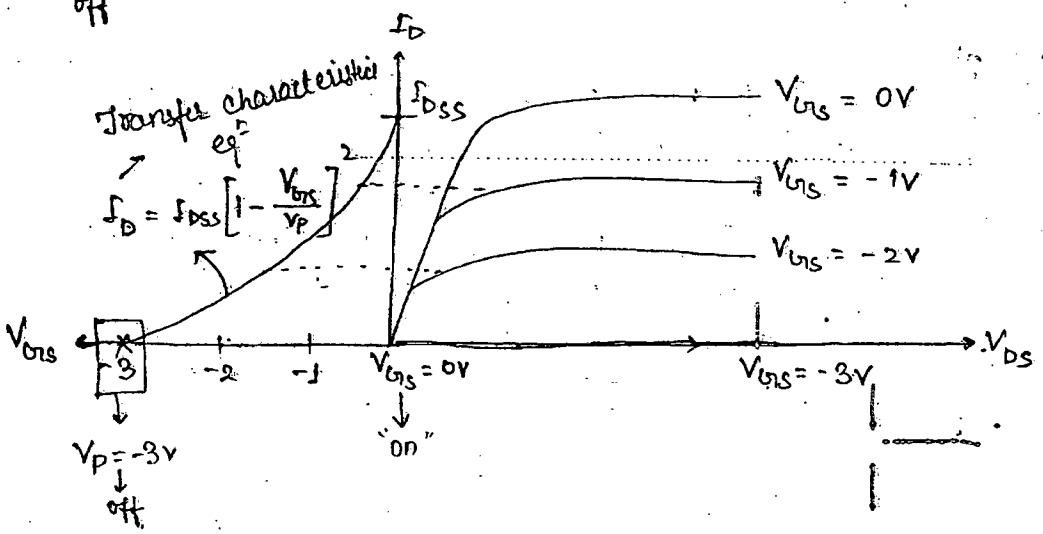


Case ii :- $V_{GS} \neq 0V$, $V_{DS} \neq 0V$.



"on"
$V_{DS} = 3V$ → V_P
$V_{DS} = 2V$
$V_{DS} = 1V$
$V_{DS} = 0V$





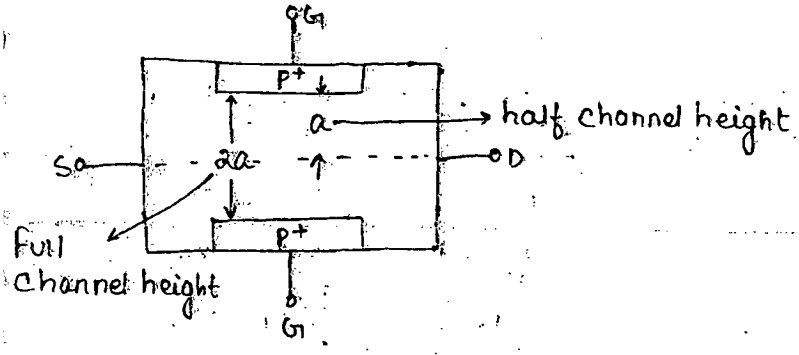
PINCH OFF VOLTAGE

$$V_P = \frac{a^2 q N_A}{2\epsilon} \quad (\text{or}) \quad V_P = \frac{a^2 q N_D}{2\epsilon}$$

P channel FET · N channel FET

Where N_A = Acceptor concentration
N_D = Donor concentration
$\epsilon = \epsilon_0 \epsilon_r$

$\epsilon_0 = 8.85 \times 10^{-12}$ F/m
$\epsilon_r = 12$ (Si)



TRANS CONDUCTANCE (g_m) :

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{\partial I_{DSS}}{\partial V_{GS}} \left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$g_m = \frac{-2 I_{DSS}}{V_P} \left[1 - \frac{(V_{GS})_Q}{V_P}\right]$$

$$\boxed{g_{mo} = \frac{-2 I_{DSS}}{V_P}} \rightarrow \text{max}^m \text{ transconductance}$$

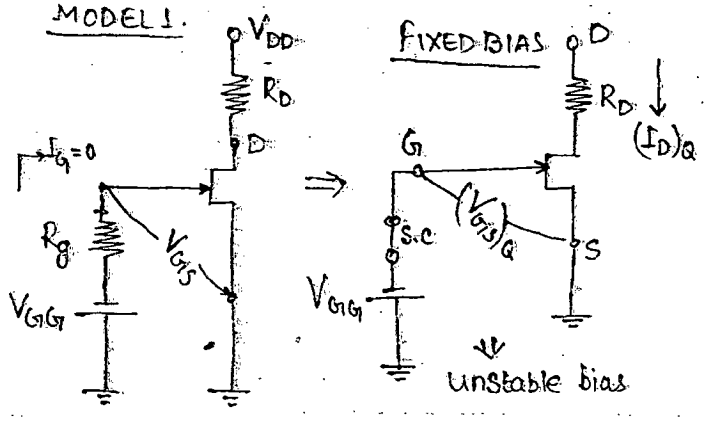
$V_{GS} = 0$.

FET BIASING.

(1) $I_G = 0$ (3) $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$

(2) $I_D = I_S$ (4) $Q\left((I_D)_Q, (V_{GS})_Q\right)$

MODEL 1.

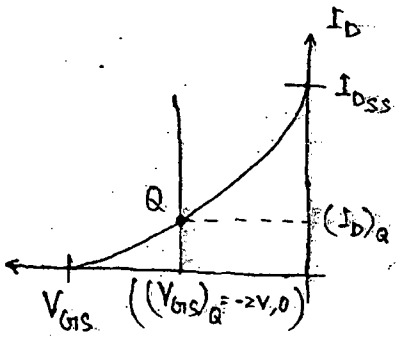


FIXED BIAS

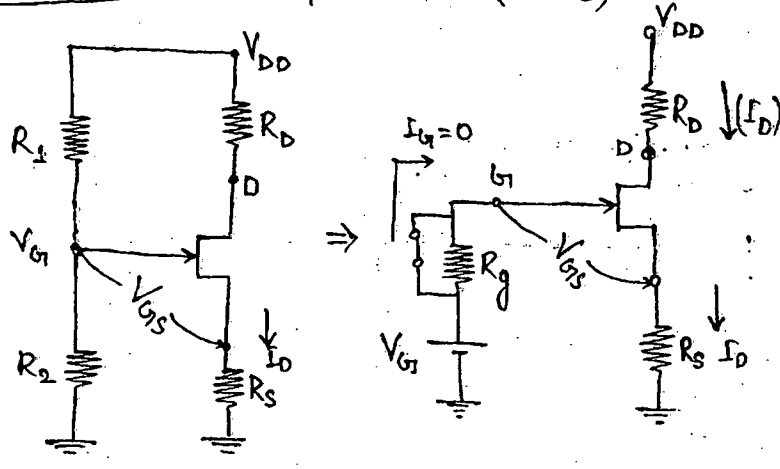
unstable bias

1. $(V_{GS})_Q = -V_{GG}$
2. $(I_D)_Q = I_{DSS}\left[1 - \frac{(V_{GS})_Q}{V_P}\right]^2$
3. $(V_{DS})_Q = V_{DD} - (I_D)_Q R_D$
4. $(V_D)_Q = (V_{DS})_Q$
5. $(V_S)_Q = 0$

6. $(V_{GS})_Q = (V_{GS})_Q$



MODEL-2. (VOLTAGE DIVIDER BIAS)



$$V_G = V_{DD} \times \frac{R_2}{R_1 + R_2}$$

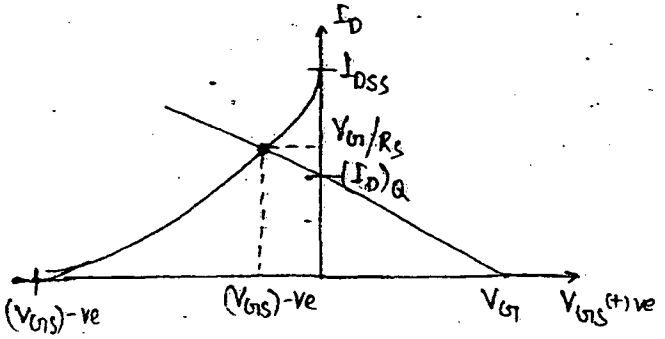
$$R_g = R_1 \| R_2$$

$$V_G = V_{GS} + I_D R_S$$

$$\boxed{V_{GS} = V_G - I_D R_S}$$

$$\boxed{I_D R_S > V_G}$$

V_{GS} = (-)ve (RB)

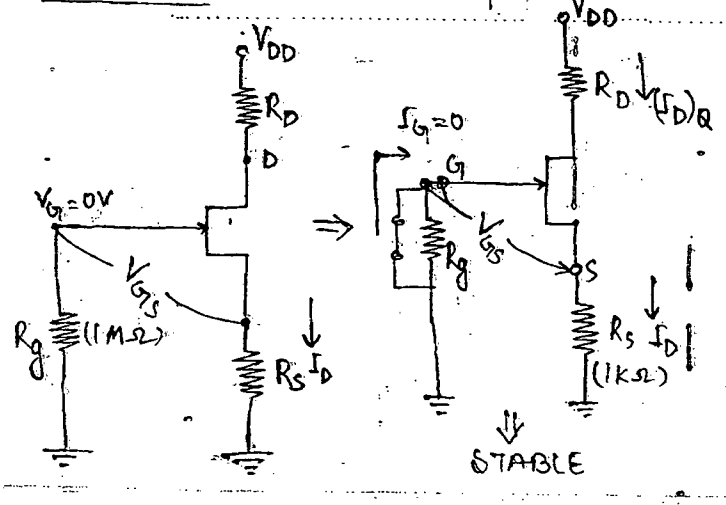


Suppose

$(I_D)_Q = 1mA$

$(V_{GS})_Q = V_G - (I_D)_Q R_S$

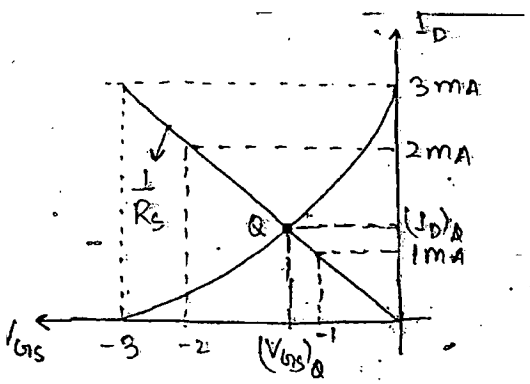
MODEL-3 SELF BIASING



$$V_G = V_{GS} + I_D R_S$$

$$0 = V_{GS} + I_D R_S$$

$$\boxed{V_{GS} = -I_D R_S}$$



$V_{GS} = 1V$, $R_S = 1K\Omega$ $\Rightarrow I_D = 1mA$

$V_{GS} = -2V$, $R_S = 1K\Omega$ $\Rightarrow I_D = 2mA$

$V_{GS} = -3V$, $R_S = 1K\Omega$ $\Rightarrow I_D = 3mA$

Suppose if

$(I_D)_Q = 1mA$

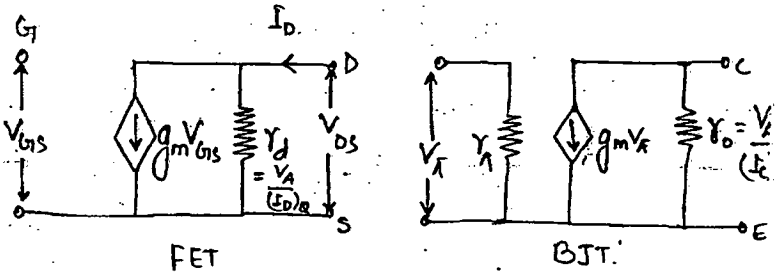
$(V_{GS})_Q = -(I_{DQ})R$

FET AMPLIFIER MODEL

$$I_D = f(V_{GS}, V_{DS})$$

$$I_D = \frac{\partial I_D}{\partial V_{GS}} + \frac{\partial I_D}{\partial V_{DS}} \cdot V_{DS}$$

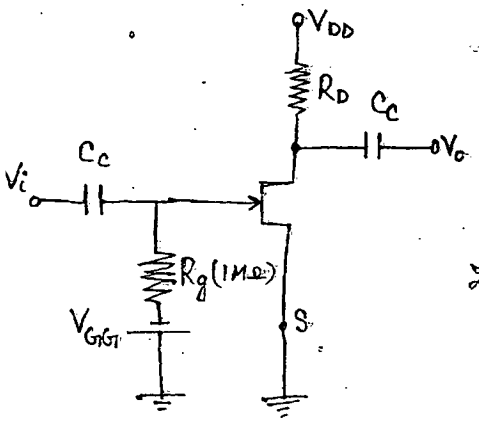
$$\boxed{I_D = g_m V_S + \frac{V_{DS}}{r_d}}$$



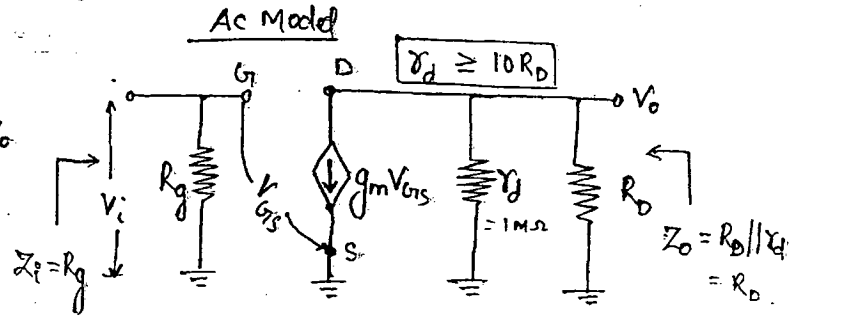
PRACTICAL FET AMPLIFIER MODELS.

1. Common Source bypass amplifier.
2. Common Source un bypass amplifier
3. Common Drain amplifier.
4. Common Gate amplifier

1. COMMON SOURCE BYPASS AMPLIFIER.

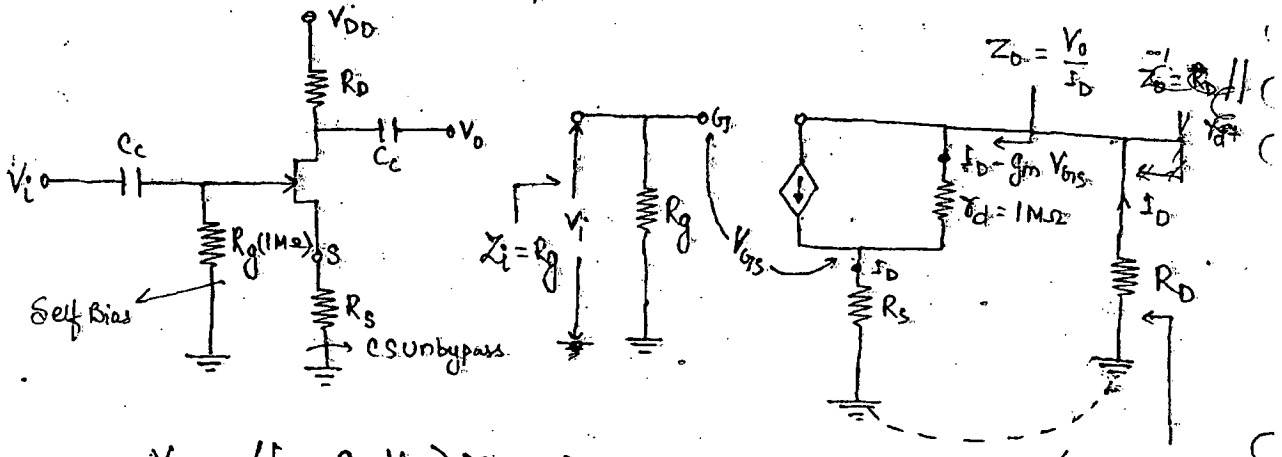


Ac Model



$V_o = -g_m V_{GS} R_D$ $\quad \boxed{V_{GS} = V_i}$ $\quad \boxed{A_V = \frac{V_o}{V_i} = -g_m R_D}$

2. COMMON SOURCE UNBYPASS AMPLIFIER.



$$V_o = (I_o - g_m V_{GS})\, r_d + I_D R_S$$

$$V_i = V_{GS} + I_D R_S$$

$$0 \quad V_{GS} = -I_D R_S$$

$$\boxed{Z_o = \frac{V_o}{I_D} = r_d + (1+\mu) R_S}$$

$$Z_o' = R_D \,||\, r_d + (1+\mu) R_S$$

$$A_V = \frac{V_o}{V_i} \qquad \boxed{V_o = -I_D R_D}$$

$$I_D R_D + (I_D - g_m V_{GS})\, r_d + I_D R_S = 0$$

$$V_{GS} = V_i - I_D R_S$$

$$\Rightarrow I_D R_D + \left\{ I_o - g_m (V_i - I_D R_S) \right\} r_d + I_D R_S = 0$$

$$\Rightarrow I_D \left(R_D + r_d + g_m R_S r_d + R_S \right) = g_m V_i r_d$$

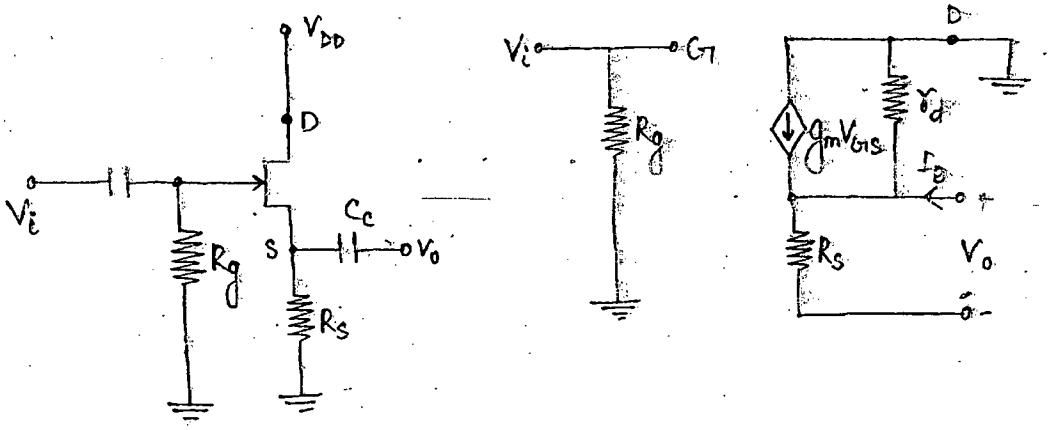
$$I_D = \frac{g_m V_i}{\frac{r_d}{r_d} + \frac{R_D}{r_d} + \frac{g_m R_S r_d}{r_d} + \frac{R_S}{r_d}} \qquad \Rightarrow \boxed{I_D = \frac{g_m V_i}{1 + g_m R_S}}$$

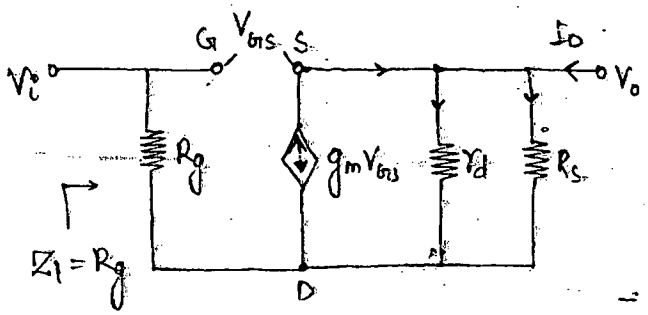
$$\boxed{\frac{V_o}{V_i} = \frac{-g_m R_D}{1 + g_m R_S}}$$

$g_m R_S \gg 1$ (FET)

$$\boxed{\frac{V_o}{V_i} = -\frac{R_D}{R_S}}$$

3. COMMON DRAIN AMPLIFIER





KVL at O/p

$$g_m V_{GS} + I_D = \frac{V_o}{r_d} + \frac{V_o}{R_S}$$

$$V_i = V_{GS} + V_o$$

$$V_{GS} = -V_o$$

$$-g_m V_o + I_D = V_o\left[\frac{1}{r_d} + \frac{1}{R_S}\right]$$

$$I_D = V_o\left[\frac{1}{r_d} + \frac{1}{r_S} + g_m\right]$$

$$Z_o = \frac{V_o}{I_o} = \frac{1}{\frac{1}{r_d} + \frac{1}{R_S} + g_m} = \frac{1}{\frac{1}{R_S} + g_m} = R_S \,||\, \frac{1}{g_m} \leq \frac{1}{g_m}\ (100\,\Omega)\ \text{FET}$$

$$\boxed{Z_o = R_S \,||\, \frac{1}{g_m}} \simeq \frac{1}{g_m}\ (100\,\Omega)\ \text{FET}$$

$$V_o = g_m V_{GS} R_S$$

$$V_i = V_{GS} + V_o$$

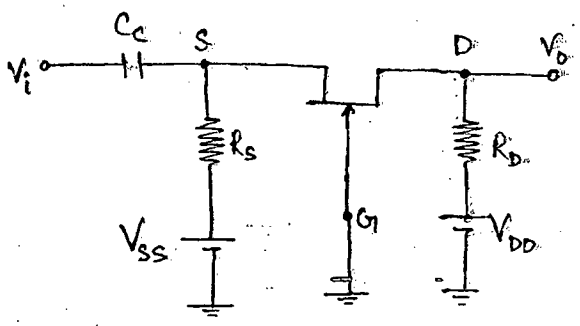
$$V_i = V_{GS}\left[1 + g_m R_S\right]$$

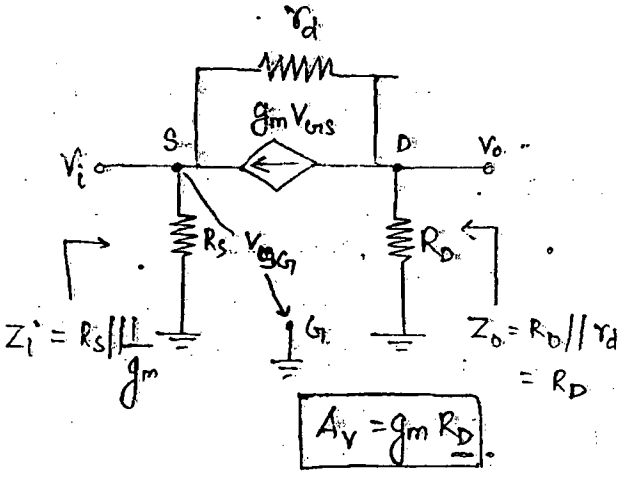
$$\boxed{\frac{V_o}{V_i} = \frac{g_m R_S}{1 + g_m R_S}}$$

$$g_m R_S >> 1$$

$$\boxed{\frac{V_o}{V_i} \approx 1}$$

4. COMMON GATE AMPLIFIER.





CONCLUSION :-

	Z_i	Z_o	A_V
CS By Pass	R_g	$R_D \| \| r_d$	$-g_m R_D$
CS un by Pass	R_g	$R_D \| \| r_d + (1+\mu) R_S$	$\frac{-g_m R_D}{1 + g_m R_S}$
Common Drain	R_g	$R_S \| \frac{1}{g_m}$	$\frac{g_m R_S}{1 + g_m R_S}$
Common gate	R_g	$R_o \| \| r_d$	$g_m R_D$