Short Answer Questions – I (PYQ)

Q. 1. Distinguish between a metal and an insulator on the basis of energy band diagrams. [CBSE (F) 2014]

Ans.

	Metal	Insulators
(i)	Conduction band and valence band overlap each other.	There is large energy gap between conduction band and valence band.
(ii)	Conduction band is partially filled and valence band is partially empty.	Conduction band is empty. This is because no electrons can be excited to it from valence band.

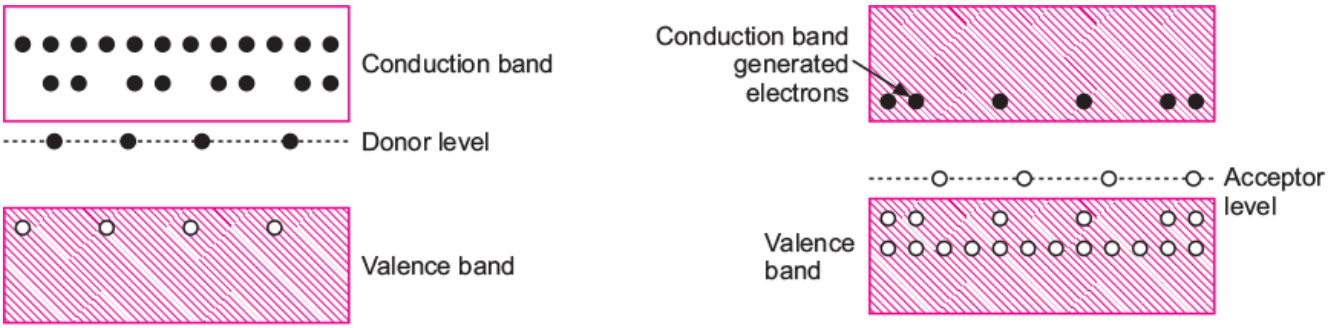
Q. 2. Write two characteristic features to distinguish between n-type and p-type semiconductors. [CBSE (F) 2012]

Ans.

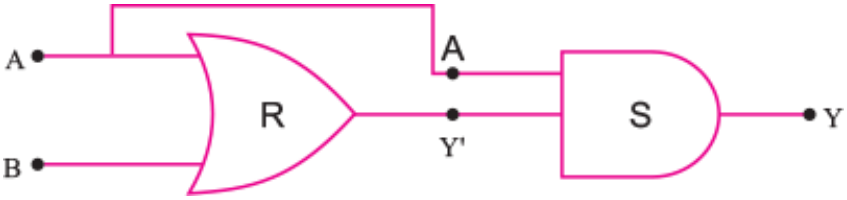
	n-type Semiconductor	p-type Semiconductor
(i)	It is formed by doping pentavalent impurities.	It is doped with trivalent impurities.
(ii)	The electrons are majority carriers and holes are minority carriers ($n_e >> n_h$).	The holes are majority carriers and electrons are minority carriers ($n_h >> n_e$).

Q. 3. Draw energy band diagrams of an n-type and p-type semiconductor at temperature T > 0 K. Mark the donor and acceptor energy levels with their energies.
[CBSE (F) 2014]

Ans.



Q. 4. Write the truth table for the combination of the gates shown. Name the gates used. [CBSE Delhi 2014]



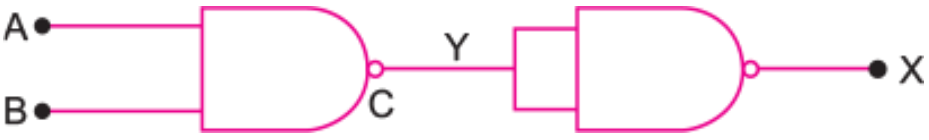
Ans.

Input		Y'	Y
A	B		
0	0	0	0
1	0	1	1
0	1	1	0
1	1	1	1

Gate R — OR gate

Gate S — AND gate

Q. 5. Draw the output waveform at X, using the given inputs A, B for the logic circuit shown alongside. Also identify the gate. [CBSE Delhi 2011]



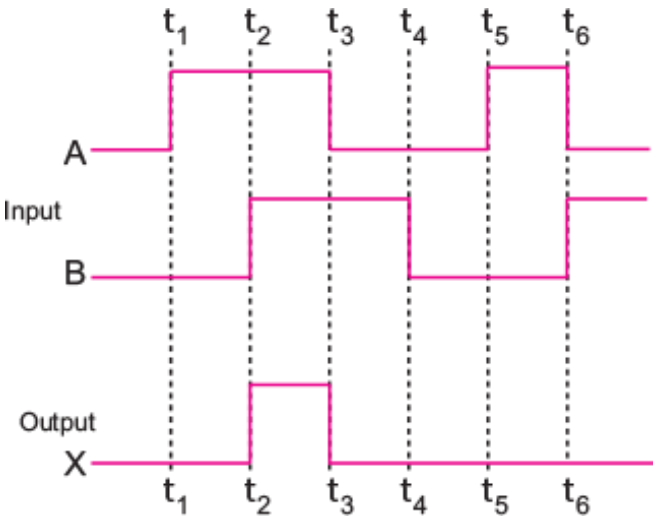
Ans.

$$Y = A \,.\, B$$

and $X = \bar{Y} = A \,.\, B$

This is AND operation. Therefore, the output is 1 when both inputs are 1.

Accordingly the waveform output is shown in figure.



Q. 6. Identify the logic gates marked P and Q in the given logic circuit. Write the truth table for the combination. [CBSE Delhi 2014]

Ans. P is 'NAND' gate and Q is 'OR' gate.

Truth Table

Input		Output
A	B	X
0	0	1
1	0	1
0	1	1
1	1	1

Q. 7. How is forward biasing different from reverse biasing in a p-n junction diode?
[CBSE Delhi 2011]

Ans. (1) Forward Bias:

(i) Within the junction diode the direction of applied voltage is opposite to that of built-in potential.

(ii) The current is due to diffusion of majority charge carriers through the junction and is of the order of mill amperes.

(iii) The diode offers very small resistance in the forward bias.

(2) Reverse Bias:

(i) The direction of applied voltage and barrier potential is same.

(ii) The current is due to leakage of minority charge carriers through the junction and is very small of the order of

(iii) The diode offers very large resistance in reverse bias.

Q. 8. The output of a 2-input AND gate is fed to a NOT gate. Give the name of the combination and its logic symbol. Write down its truth table.
[CBSE Delhi 2009]

Ans. Name of combination: NAND gate logic symbol.

Truth Table of NAND gate is

Input		Output
A	B	Y
0	0	1
1	0	1
0	1	1
1	1	0

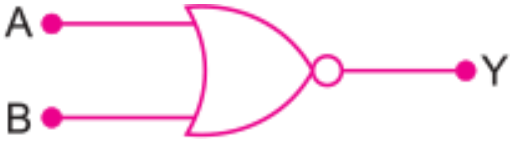
Q. 9. Draw the logic symbol of the gate whose truth table is given below:

Input		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

If this logic gate is connected to NOT gate, what will be output when (i) A = 0, B = 0 and

(ii) A = 1, B = 1? Draw the logic symbol of the combination. [CBSE (F) 2009]

Ans. The given truth table is of NOR gate. The logic symbol is shown in fig.

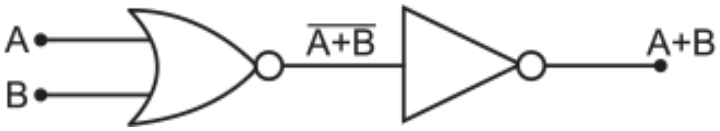


When it is connected to a NOT gate, the gate becomes OR gate.

(i) A = 0, B= 0 gives output 0.

(ii) A = 1, B = 1 gives output 1.

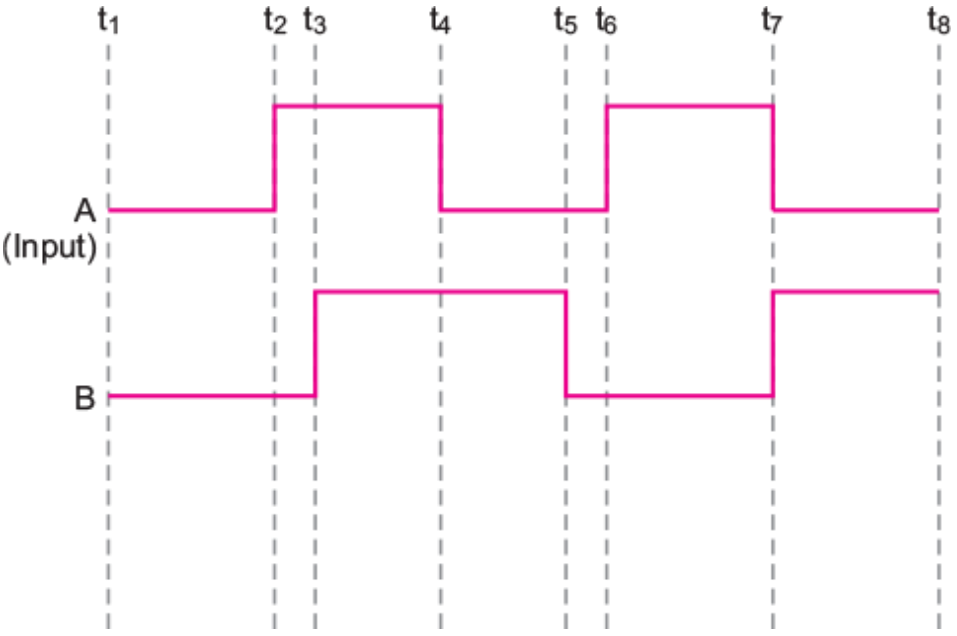
The combination is shown in fig.



Q. 10. Answer the following question :

(i) Identify the gate equivalent to the 'dotted box' shown here and give its symbol and truth table. [CBSE (AI) 2013, 2012, 2011, CBSE (F) 2014, 2010]

(ii) The input 'A' shown here is used with another unknown input 'B' in this set-up. If the output 'Y' has the form shown, give the intervals over which the input 'B' is in its 'high' state.



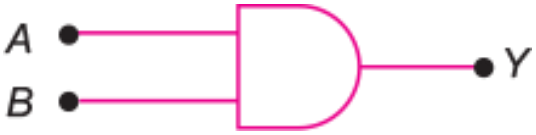
Ans. (i)

The output $Y = \bar{A} + \bar{B} = \bar{\bar{A}} \cdot \bar{\bar{B}} = AB$

That is equivalent gate is '**AND**' gate.

The symbol and truth table are shown in fig.

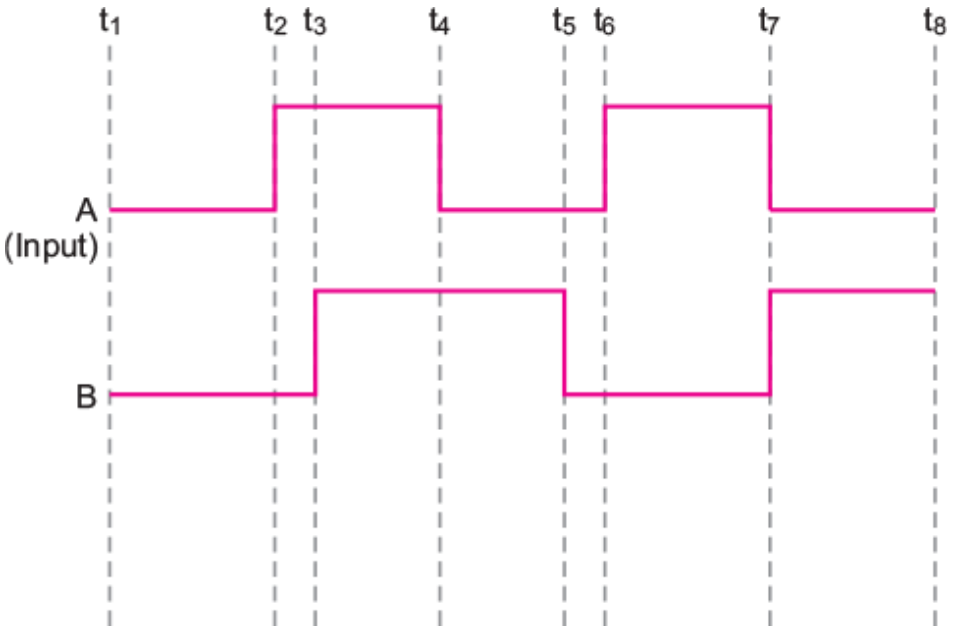
Truth Table



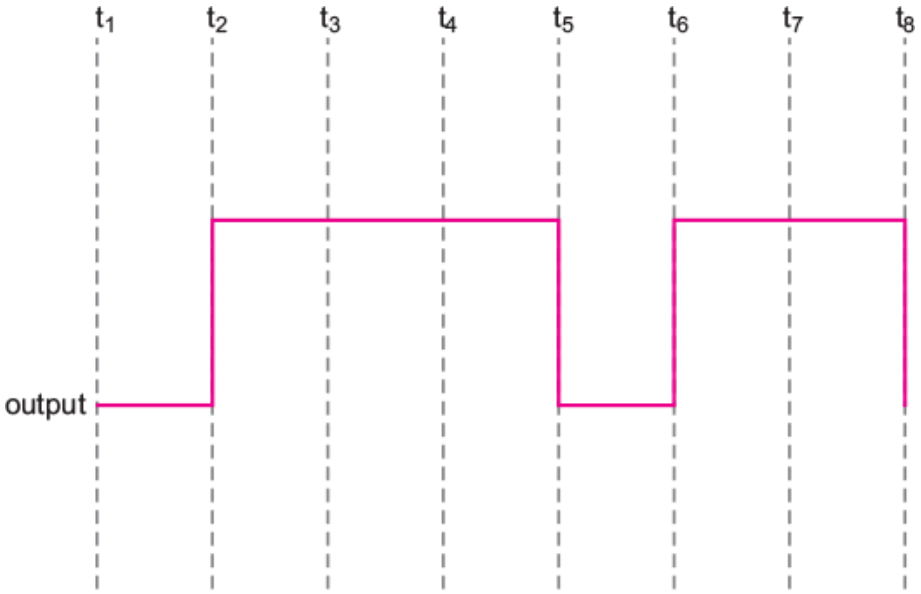
A	B	Y
0	0	0
1	0	0
0	1	0
1	1	1

(ii) Output will be high if both inputs A and B are high., so B is in higher state in higher state in intervals from 3 to 5 and from 7 to 8.

Q. 11. The figure shows input waveforms A and B to a logic gate. Draw the output waveform for an OR gate. Write the truth table for this logic gate and draw its logic symbol. [CBSE (AI) 2017]



Ans.

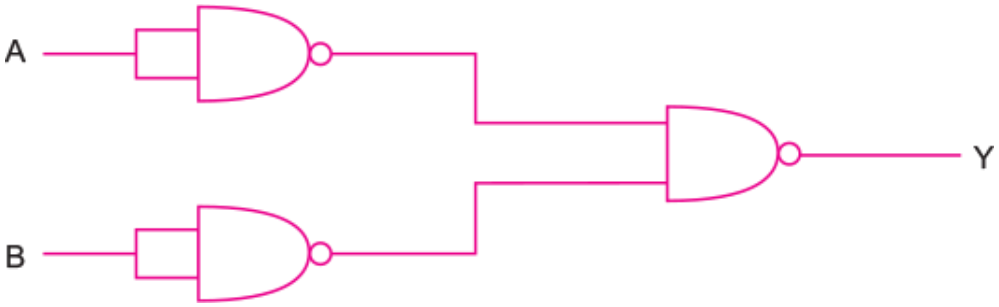


Truth Table

Input		Output
A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

OR Gate

Q. 12. Write the truth table for the logic circuit shown below and identify the logic operation performed by this circuit. [CBSE Delhi 2011, (AI) 2011, (F) 2014]



Ans.

The logic circuit performs OR-operation.

Truth table

A	B	Y
0	0	0
1	0	1
0	1	1
1	1	1

Q. 13. Using truth tables of AND gate and NOT gate, show that NAND gate is an AND gate followed by a NOT gate. Hence write the truth table of NAND gate.

Why are NAND gates called 'Universal Gates'? [CBSE Guwahati 2015]

Ans.

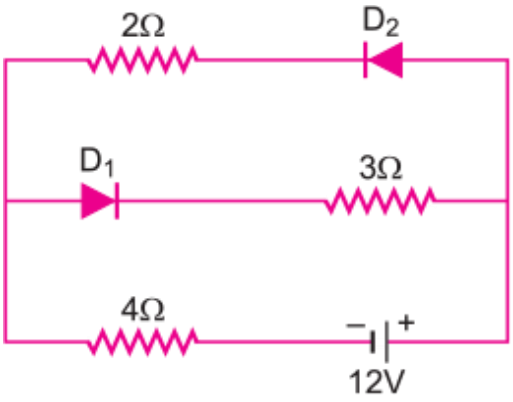
Input of AND Gate		Output of AND Gate and Input of NOT Gate	Output of NOT Gate
A	B		
0	0	0	1
1	0	0	1
0	1	0	1
1	1	1	0

Truth Table of NAND Gate

A	B	Output of NAND Gate
0	0	1
1	0	1
0	1	1
1	1	0

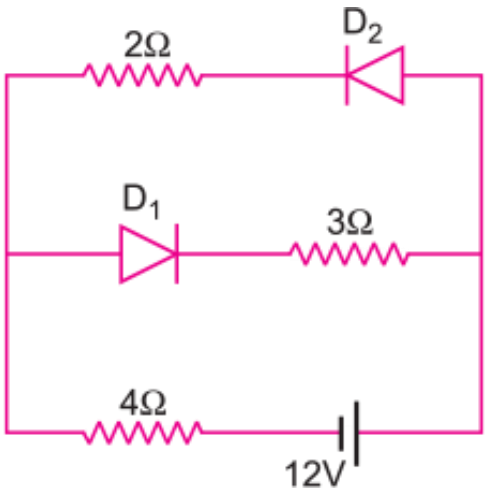
All primary gates like AND, NOT and OR gates can be realised by using NAND gate only. Hence, it is a universal gate.

Q. 14. The circuit shown in the figure has two oppositely connected ideal diodes connected in parallel. Find the current flowing through each diode in the circuit. [CBSE (F) 2013]



Ans. (i) Diode D_1 is reverse biased, so it offers an infinite resistance. So no current flows in the branch of diode D_1.

(ii) Diode D_2 is forward biased, and offers no resistance in the circuit. So current in the branch

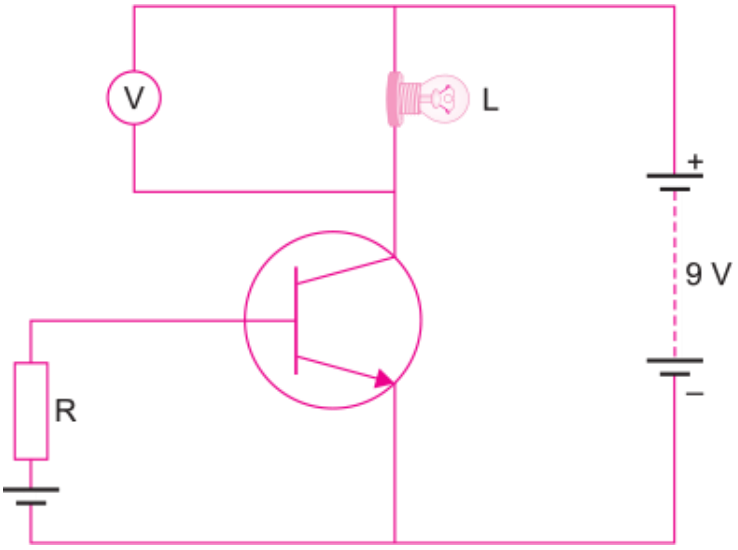


$$I = \frac{V}{R_{eq}} = \frac{12V}{2\Omega + 4\Omega} = 2A$$

Q 15. In the given circuit diagram, a voltmeter 'V' is connected across a lamp 'L'. How would (i) the brightness of the lamp and (ii) voltmeter reading 'V' be affected, if the value of resistance 'R' is decreased? Justify your answer.
[HOTS][CBSE Delhi 2013]

Ans. (i) If the value of the resistance *R* is reduced, the current in the forward biased input circuit increases. The emitter current IE and the collector current I_C (= I_E – I_B) both increase. Hence, the brightness of the lamp increases.

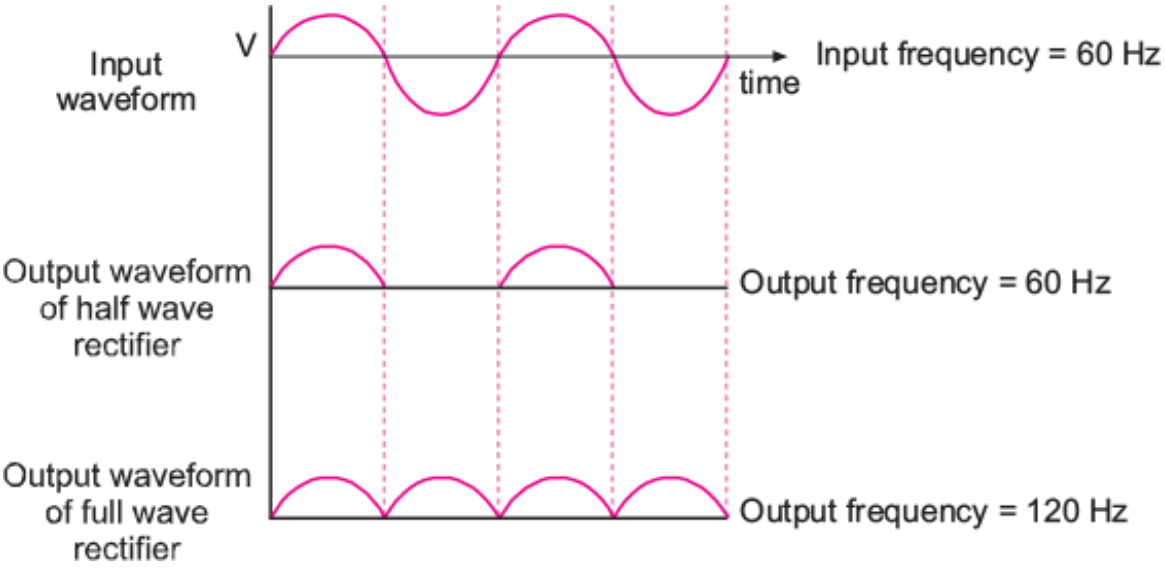
(ii) Due to increase in I_C, the potential drop across lamp *L* increases and hence the voltmeter reading *V* increases.



Short Answer Questions – I (OIQ)

Q. 1. An ac input signal of frequency 60 Hz is rectified by a (i) half wave (ii) full wave rectifier. Draw the output waveform and write the output frequency in each case.

Ans.



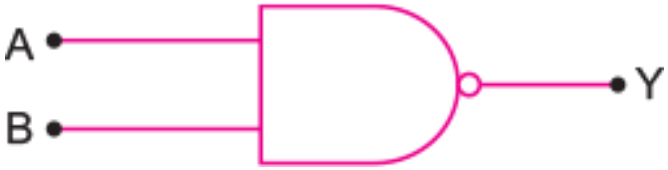
Q. 2. The following table gives the output of a two input logic gate.

(i) Identify the logic gate and draw its logic symbol.

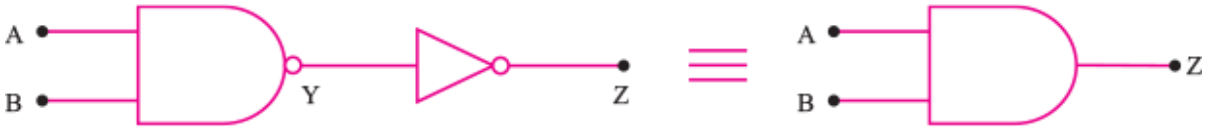
(ii) If the output of this gate is fed as input to a NOT gate, name the new logic gate so formed.

A	B	Y
0	0	1
1	0	1
0	1	1
1	1	0

Ans (i) The truth table given represents a NAND gate.



(ii) Clearly resulting gate will be an AND gate.

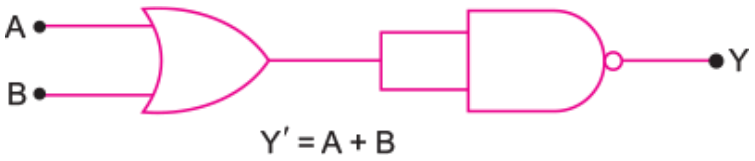


Truth table of new gate formed

Input		Output	
A	B	Y	$\bar{Y} = Z$
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

Q. 3. The output of an OR gate is connected to both the inputs of a NAND gate. Draw the logic circuit of this combination of gates and write its truth table.

Ans. The logic circuit is shown in fig.



The logic circuit represents NOR gate. Its truth table is

A	B	Y'	Y
0	0	0	1
1	0	1	0
0	1	1	0
1	1	1	0

Q. 4. In a common emitter mode of a transistor, the d.c. current gain is 20, the emitter current is 7 mA. Calculate (i) base current and (ii) collector current.

Ans.

Given $\beta = 20$, $i_E = 7$ mA

i. $\beta = \frac{i_C}{i_B} = \frac{i_E - i_B}{i_B}$ or $\beta_{i\beta} = i_E - i_B$

$\Rightarrow \quad i_B = \frac{i_E}{\beta+1} = \frac{7 \text{ mA}}{20+1} = \frac{7}{21} \text{ mA} = \frac{1}{3} \text{ mA}$

ii. $i_C = i_E - i_B = 7 - \frac{1}{3} = \frac{20}{3}$ mA

Q. 5. A semiconductor has equal electron and hole concentration of 6×10^8 / m^3. On doping with certain impurity, electron concentration increases to 9×10^{12} / m^3.

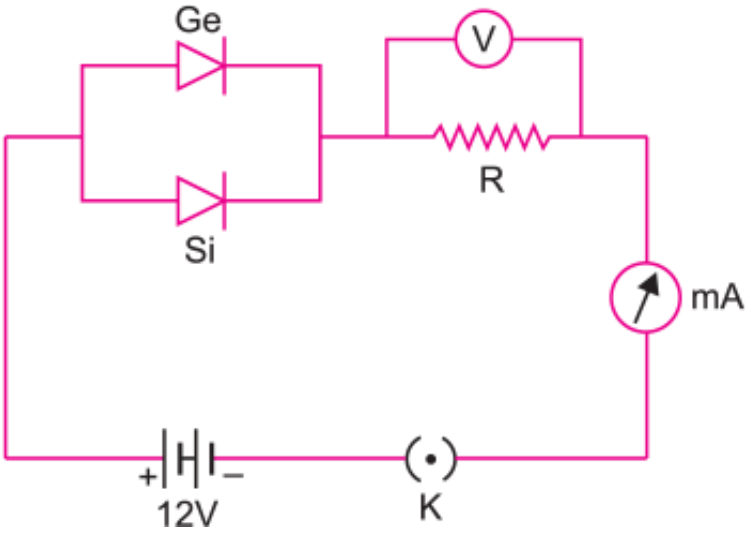
(i) Identify the new semiconductor obtained after doping.

(ii) Calculate the new hole concentration.

Ans. (i) The doped semiconductor is n-type.

ii. $n_e n_h = n_i^2 \quad \Rightarrow \quad n_h = \frac{n_i^2}{n_e} = \frac{(6\times10^8)^2}{9\times10^{12}} = 4 \times 10^4 \text{per m}^3$

Q. 6. Germanium and silicon junction diodes are connected in parallel. A resistance R, a 12 V battery, a milliammeter (mA) and key (K) are connected in series with them (figure). When key (K) is closed, a current begins to flow in the milliammeter. What will be the maximum reading of voltmeter connected across resistance R?
[HOTS]



Ans. The potential barrier of germanium junction diode is 0.3 V and of silicon is 0.7 V. Both germanium and silicon are forward biased. Therefore, for conduction the minimum potential difference across junction diode is 0.3 V.

Maximum reading of voltmeter connected across R = 12 – 0.3 = **11.7 V.**

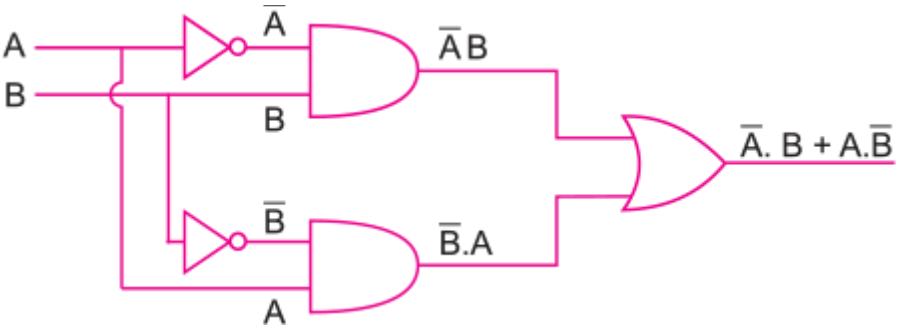
Q. 7. An X-OR gate has following truth table:

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

It is represented by following logic relation [HOTS][NCERT Exemplar]

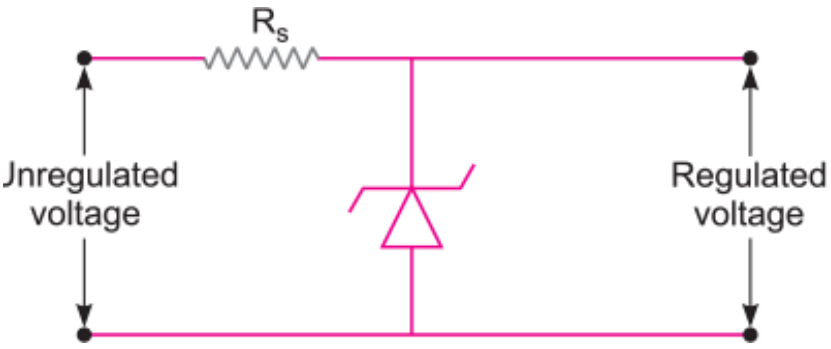
$Y = \bar{A}.\ B + A.\ \bar{B}$. Build this gate using AND, OR and NOT gates.

Ans.



Q. 8. A Zener of power rating 1 W is to be used as a voltage regulator. If zener has a breakdown of 5 V and it has to regulate voltage which fluctuated between 3 V

and 7 V, what should be the value of Rs for safe operation (see figure)? [HOTS][NCERT Exemplar]



Ans.

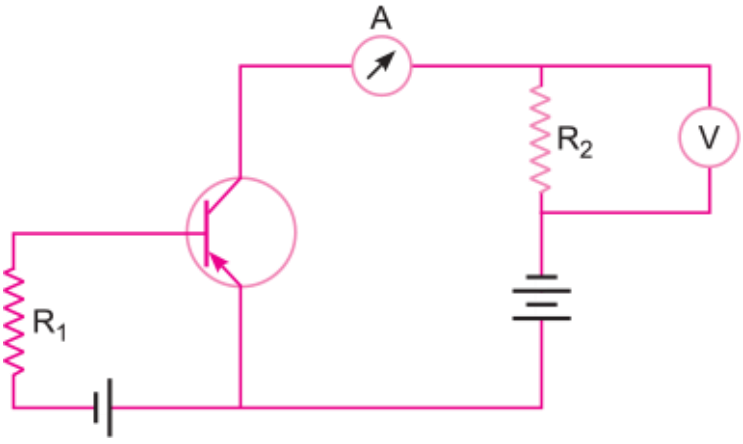
Here, P = 1W, V_z = 5V

V_s = 3V to 7V

$$I_{Z\ \max} = \frac{P}{V_Z} = \frac{1}{5} = 0.2A = 200\,\text{mA}$$

$$R_S = \frac{V_S - V_z}{I_{Z\ \max}} = \frac{7-5}{0.2} = \frac{2}{0.2} = 10\Omega$$

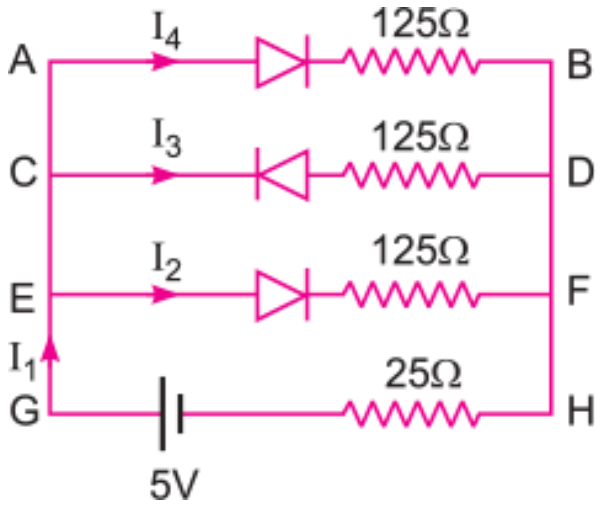
Q. 9. If the resistance R^1 is increased (Fig.), how will the readings of the ammeter and voltmeter change? [HOTS] [NCERT Exemplar]



Ans.

$I_B = \frac{V_{BB} - V_{BE}}{R_1}$. If R_1 is increased, I_B will decrease. Since $I_c = \beta I_b$, it will result in decrease in I_c, *i.e.*, decrease in ammeter and voltmeter readings.

Q. 10. If each diode in figure has a forward bias resistance of 25 Ω and infinite resistance in reverse bias, what will be the values of current I_1, I_2, I_3 and I_4? [HOTS] [NCERT Exemplar]



Ans. I_3 is zero as the diode in that branch is reverse biased. Resistance in the branch AB and EF are each (125 + 25)Ω = 150 Ω

As AB and EF are identical parallel branches, their effective resistance is $\frac{150}{2}$ = 75Ω

∴ Net resistance in the circuit = (75 + 25) Ω = 100 Ω

$$\therefore \text{Current } I_1 = \frac{5}{100} = 0.05A$$

As resistances of AB and EF are equal, and $I_1 = I_2 + I_3 + I_4$, $I_3 = 0$

$$\therefore I_2 = I_4 = \frac{0.05}{2} = 0.025\,A$$

Q. 11. Three photo diodes D_1, D_2 and D_3 are made of semiconductors having band gaps of 2.5 eV, 2 eV and 3 eV, respectively. Which ones will be able to detect light of wavelength 6000 Å? [HOTS][NCERT Exemplar]

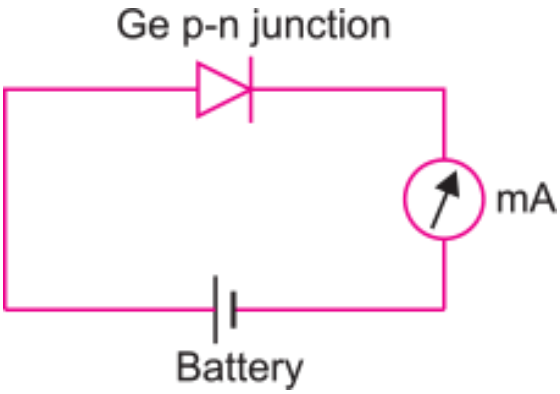
Ans. Energy of incident light photon,

$$E = h\nu = \frac{hc}{\lambda}$$

$$= \frac{6.6\times10^{-34}\times3\times10^{8}}{6\times10^{-7}\times1.6\times10^{-19}} = 2.06\ \text{eV}$$

For the incident radiation to be detected by the photodiode, energy of incident radiation photon should be greater than the band gap. This is true only for D_2. Therefore, only D_2 will detect this radiation.

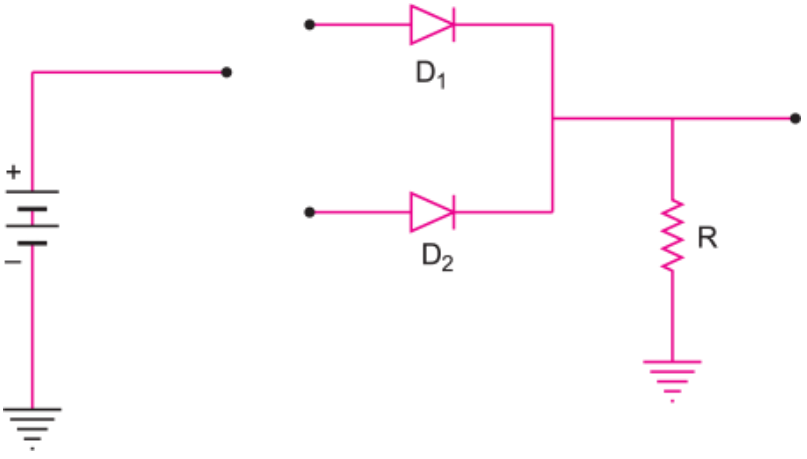
Q. 12. A germanium p-n junction is connected to a battery with milliammeter in series. What should be the minimum voltage of battery so that current may flow in the circuit?
[HOTS]



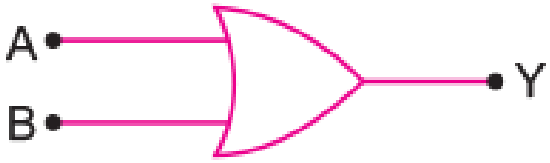
Ans. The internal potential barrier of germanium is 0.3 V, therefore to overcome this barrier the potential of battery should be equal to or more than 0.3 V.

Therefore, the minimum voltage of battery = 0.3 V.

Q. 13. Name the logic gate which can be realised by using a p-n junction diode in the given diagram. Give its logic symbol and write the truth table. Name the gate which will be obtained by combining with a NOT gate.



Ans. The logic gate shown in the circuit diagram is OR gate.



Symbol of OR gate:

Input		Output
A	**B**	**Y**
0	0	1
1	0	1
0	1	1
1	1	1

The gate obtained by combining OR gate with NOT gate will be NOR gate.