Chapter 4

Sequential Circuits

LEARNING OBJECTIVES

- *Sequential circuit*
- *Basic storage elements*
- *Latches (SR Latch, D Latch, JK Latch)*
- *Flip-flops (JK flip-flop, T flip-flop, D flip-flop)*
- *Counters*
- *Asynchronous counter design*
- *Synchronous counter design*
- *Registers*
- *Various types of registers*
- *Application of shift register*

Sequential Circuits

In sequential circuits the output depends on the input as well as on the previous history of output, i.e., they contain memory elements.

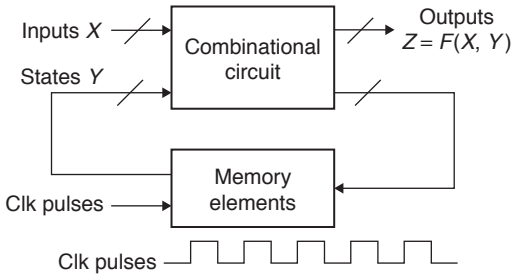


Figure 1 Block diagram of sequential circuit

Table 1 *Comparison between combinational and sequential circuits*

Combinational Circuits	Sequential Circuits
1. Output at any time depends on the combine set of input applied to it simultaneously at that instant of time	Output depends on the present input as well as on the previous history of output
2. Contains no memory element	Contains at least one memory element
3. Easy to design due to absence of memory	Difficult to design
4. Totally described by the set of output values	Its performance is totally described by the set of subsequent values as well as set of output values
5. Faster in speed because all inputs are primary inputs and applied simultaneously	Slower in speed because secondary inputs are also needed which are applied after delay
6. It need more hardware for realization	Less hardware required
7. Expensive in cost	Cheap in cost

Sequential circuits are of two types:

1. Clocked or synchronous
2. Unclocked or asynchronous

In synchronous sequential circuits the logic circuits action is allowed to occur in synchronization with the input clock pulse from a system clock.

In asynchronous sequential circuits the logic sequential action is allowed to occur at any time.

Basic Storage Elements

Latches and flip-flops

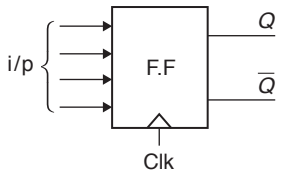
A storage element in digital circuit can maintain a binary state indefinitely until directed by an input signal to switch states. Storage elements that operate with signal levels (i.e., level triggering of signal inputs) are referred to as latches. Those controlled by a clock transition (i.e., edge triggering) are flip-flops.

Latches and filp-flops are related because latches are basic circuits from which all flip-flops are constructed. Latches are useful for storing binary information and for the design of asynchronous sequential circuits. But latches are not practical for use in synchronous sequential circuits, so we use flip-flops.

Flip-flops

They are also known as bistable multivibrators. This is a basic memory element to store 1-bit of information 0 or 1 and is used in storage circuits, counters, shift register, and many other computer applications. It has two stable states: 1 and 0. The high state is called set state and zero as reset.

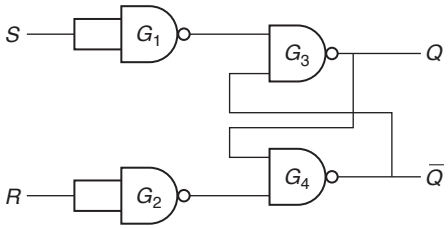
It has two outputs one being the complement of the other usually designated by Q and $\overline{Q}$.



There are different types of flip-flops S-R flip-flop, D-flip-flop, T-flip-flop, J-K flip–flops, etc.

Latches

(i) S-R Latch: The simplest latch is called S-R latch. S-R means Set-Reset. It has two outputs Q and $\overline{Q}$ and two inputs S and R, which represent set or reset signal.



Above figure shows two cross coupled gates G_3 and G_4 and inverters G_1 and G_2. Here output of G_3 is connected to the input of G_4 and output of G_4 is applied to the input of G_3. $S = 1$, $R = 0$ output of $G_1 = 0$ and $G_2 = 1$. Since one of the input of G_3 is 0, so its output will be certainly 1 and consequently both input of G_4 will be 1 and the output $\overline{Q} = 0$.

For $S = 1$, $R = 0$, $Q = 1$, $\overline{Q} = 0$. $S = 0$, $R = 1$ the output will be $Q = 0$ and $\overline{Q} = 1$. The first of the input condition $S = 1$ and $R = 0$ makes $Q = 1$ which referred as the set state and the second condition $S = 0$ and $R = 1$ makes $Q = 0$ which is referred as reset state.

For $S = 0$ and $R = 0$ output of both G_1 and G_2 will be one and hence there will be no change in Q and $\overline{Q}$.

For $S = R = 1$, both the outputs Q and $\overline{Q}$ will try to become one, which produces invalid results and should not be used for the above latch.

Input		Output		
S	R	Q	$\overline{Q}$	State
1	0	1	0	Set
0	1	0	1	Reset
0	0	0	0	No change
1	1	?	?	Invalid

(ii) SR latch by using NAND/NOR gates: The SR latch is a circuit with two cross-coupled NOR gates or two cross-coupled NAND gates. Two inputs labelled S for set and R for reset. Latch will have two outputs:

- Q: output state in normal form and
- Q': output state in complemented form.

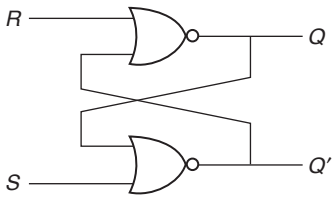


Figure 2 Logic diagram for SR latch

S	R	Q_{n+1}	Q'_{n+1}	
0	0	Q_n	Q'_n	(no change)
0	1	0	1	(Reset)
1	0	1	0	(set)
1	1	0	0	(invalid)

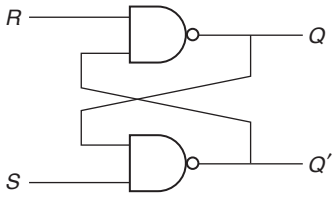
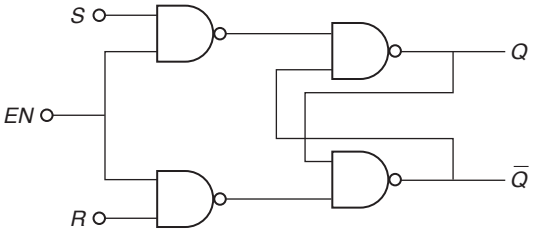


Figure 3 $\overline{S}\,\overline{R}$ Latch

S	R	Q_{n+1}	$\overline{Q}_{n+1}$	
0	0	1	1	(Invalid)
0	1	1	0	(Set)
1	0	0	1	(Reset)
1	1	Q_n	Q'_n	(No change)

$\overline{S}\,\overline{R}$ latch is active low SR latch

(iii) SR latch with control input: The working of gated SR latch is exactly the same as SR latch when the EN pulse is present. When the EN pulse is not present (EN pulse = 0) the gates G_1 and G_2 are inhibited and will not respond to the input.

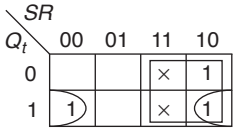


Characteristic table of SR latch shows the operation of latch in tabular form. Q_t stands as the binary state of the latch before the application of latch pulse and referred to as the present state. The S and R columns give the possible values of the inputs and Q_{t+1} is the state of the latch after the application of a single pulse, referred to as next stage. EN input is not included in the characteristic table.

Characteristic table for SR latch is given below:

Q_t	S	R	Q_{t+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	X
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	X

Characteristic equation of the latch is derived from the K-map.



$$\therefore Q_{t+1} = S + \bar{R}Q_t$$

This equation specifies the value of the state as a function of the present state and the inputs.

(iv) Preset and clear inputs: For the latch/flip-flop, when the power is switched ON, the state of the circuit is uncertain. It can be either $Q = 0$ (reset) or $Q = 1$ (set) state.

In many applications it is desired to set or reset the circuit, so that initial state of the circuit will be known. This is accomplished by using the asynchronous, inputs referred to as preset (Pr) and clear (Clr), inputs.

These inputs can be applied any time, and are not synchronized with EN input/Clr input.

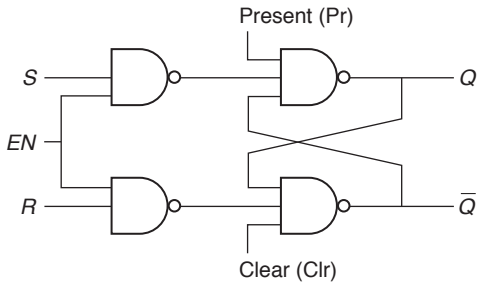


Figure 4 SR latch with Pr and Clr inputs

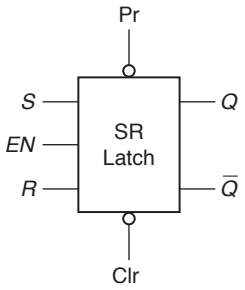
If Pr = Clr = 1, the circuits operates as of S–R latch explained previously.

If Pr = 0, Clr = 1, the output Q will become 1, which in turn changes $\bar{Q} = 0$.

If Pr = 1, Clr = 0 the output $\bar{Q}$ will become 1, which in turn changes $Q = 0$.

If Pr = Clr = 0, both Q and $\bar{Q}$ will become 1, which is invalid case, so Pr = Clr = 0 condition must not be used.

Pr	Clr	Q_{n+1}
1	1	Q – No change
0	1	1 – Set
1	0	0 – Reset
0	0	X – Invalid



(v) D latch (Transparent latch): One way to eliminate the invalid condition of SR latch (when $S = R = 1$) is to ensure that inputs S and R are never equal to 1 at the same time.

By connecting a NOT gate between S and R inputs. i.e, complement of S will be given to R, we can form D latch as shown in block diagram.

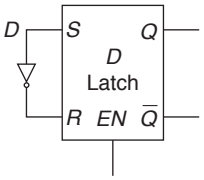


Figure 5 Block diagram for D latch

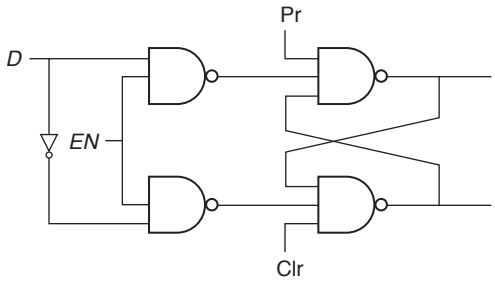


Figure 6 Logic diagram for D latch

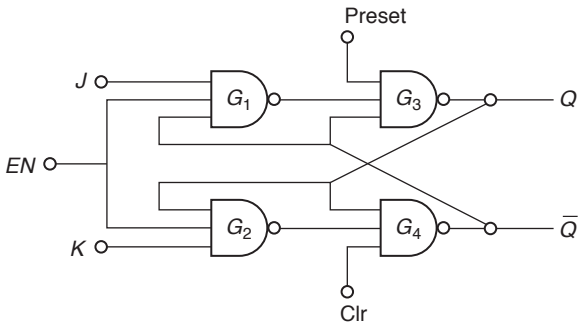
EN	D	Q_{n+1}
0	X	Q_n – No change (Disabled)
1	0	0 – Reset state
1	1	1 – Set state

When EN = 0, the circuit will be disabled and input D will not have only effect on output, and output will be same as previous state.

When EN = 1, $D = 0$, i.e., $S = 0$, $R = 1$ which makes output $Q = 0$ and $\bar{Q} = 1$ (Reset state).

When EN = 1, $D = 1$, i.e., $S = 1$, $R = 0$ which makes output $Q = 1$, and $\bar{Q} = 0$ (Set state).

(vi) JK latch: The function of JK latch is identical to that of SR latch except that it has no invalid state as that of SR latch where $S = R = 1$. In this case the state of the output is changed as complement of previous state.



EN	J	K	Q_{t+}	
1	0	0	Q_t	No change
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	$\bar{Q}_t$	Toggle
0	x	x	Q_t	No change

JK latch by using SR latch: The uncertainty of SR flip-flop (when $S = 1$, $R = 1$) can be eliminated by converting it into JK latch.

The data inputs J and K, which are ANDed with $\bar{Q}$ and Q respectively, to obtain S and R inputs.

$$S = J \cdot \bar{Q}, \quad R = K \cdot Q$$

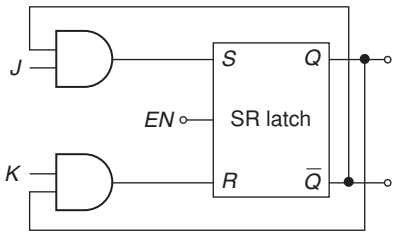
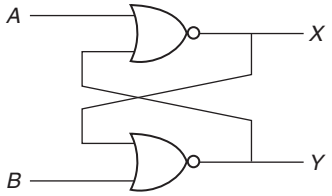


Figure 7 JK latch by using SR latch

J	K	S	R	Q_{n+1}	$\bar{Q}_{n+1}$
0	0	0	0	Q_n	$\bar{Q}_n$-No change
0	1	0	Q_n	0	1-Reset
1	0	$\bar{Q}_n$	0	1	0-Set
1	1	$\bar{Q}_n$	Q_n	$\bar{Q}_n$	Q_n-Toggle

Example 1: The following binary values were applied to A and B inputs of NOR gate latch shown in the figure, in the sequence indicated below. $A = 1$, $B = 0$; $A = 1$, $B = 1$; $A = 0$, $B = 0$. The corresponding stable X, Y outputs will be



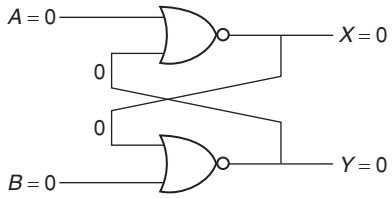
(A) 10, 01, 10 or 01
(B) 11, 00, 10
(C) 01, 00, 10 or 01
(D) 10, 11, 10 or 01

Solution: (C)
Given circuit is RS latch with NOR gates.
By comparing with RS latch $A = R$, $B = S$, and $X = Q$, $Y = \bar{Q}$, so from truth table of RS latch

S/B	R/A	Q/X	$\bar{Q}$/Y	
0	1	0	1	Reset (Invalid)
1	1	0	0	
0	0	1	0	(Same as previous state)
		0	1	

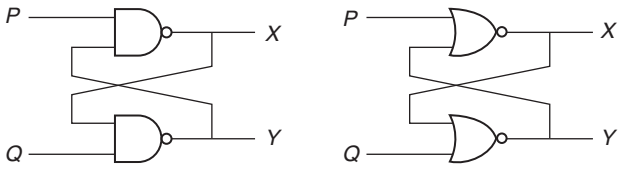
After invalid case $S = 1$, $R = 1$, i.e., $A = B = 1$,
The output $Q = 0$, $\bar{Q} = 0$, i.e., $X = Y = 0$
By applying $A = 0$, $B = 0$
The output X becomes $\overline{(0+0)} = 1$ and which in turn changes

$$Y = \overline{(B + X)} = \overline{(0+1)} = 0$$



(or) the output Y becomes $\overline{(0+0)} = 1$ and which in turn changes $X = \overline{(Y + A)} = \overline{(0+1)} = 0$. So, output (X, Y) cannot be predicted after the invalid condition. So, $X = 0$, $Y = 1$ or $X = 1$, $Y = 0$

Example 2: Refer to the NAND and NOR latches shown in the figure the inputs (P, Q) for both the latches are first made (1, 0) and then after a few seconds, made (0, 0). The corresponding stable outputs (X, Y) are



(A) NAND: first (0, 1) then (0, 1); NOR: first (1, 0) then (1, 0)
(B) NAND: first (0, 1) then (1, 1); NOR: First (0, 1) then (0, 1)
(C) NAND: first (1, 0) then (0, 0); NOR: first (1, 0) then (1, 0)
(D) NAND: first (1, 0), then (1, 0); NOR: first (1, 0) then (1, 1)

Solution: (B)
From the truth table of SR latch and $\bar{S}$ $\bar{R}$ latch SR latch with NOR gates:
For $(P, Q) = (1, 0) = (R, S)$ output $(X, Y) = (Q, \bar{Q}) = (0, 1)$

Then (P, Q) are made (0, 0), i.e., (R, S) = (0, 0), which results in no change at output. So, $(X, Y) = (Q, \bar{Q}) = (0,1)$

SR latch with NAND gates:

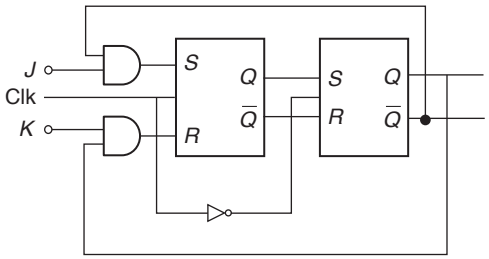
For $(P, Q) = (1, 0) = (S, R)$ output $(X, Y) = (Q, \bar{Q}) = (0,1)$. Then (P, Q) are made (0, 0), i.e., $(S, R) = (0, 0)$ which is invalid conditions for $\bar{S}\,\bar{R}$ latch. So, $(X, Y) = (Q, \bar{Q}) = (1,1)$

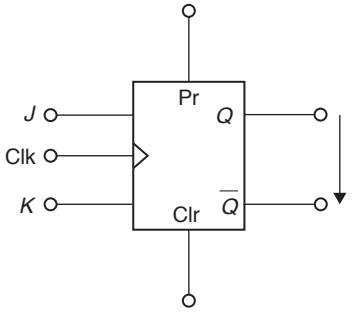
(vii) Race around condition: The difficulties of both the inputs ($S = R = 1$) being not allowed in an SR latch is eliminated in JK latch by using the feedback connection from the output to the input of the gate G_1 and G_2. In a normal JK latch if $J = K = 1$ and $Q = 0$ and enable signal is applied without RC differentiator, after a time interval Δt (the propagation delay through two NAND gate in series) the output will change to $Q = 1$. Now we have $J = K = 1$ and $Q = 1$ and after another time interval of Δt the output will change back to $Q = 0$. Hence for the duration of (t_p) of the enable signal the output will oscillates back and forth between 0 and 1. At the end of the enable signal the values of Q is uncertain. This situation is referred to as race around condition.

The race around condition can be avoided if enable time period $t_p < \Delta t$ but it may be difficult to satisfy this condition, because of very small propagation delays in ICs. To solve this problem the enable signals are converted to narrows spike using RC differentiator circuit having a short time constant. Its output will be high during the high transmission time of the enable. Another method to avoid this problem is master-slave JK flip-flop.

FLIP-FLOPS

(i) Master-slave JK flip-flop: This is a cascade of 2 SR latches with feedback from the output of the second SR latch to the inputs of the first as shown in the figure below.





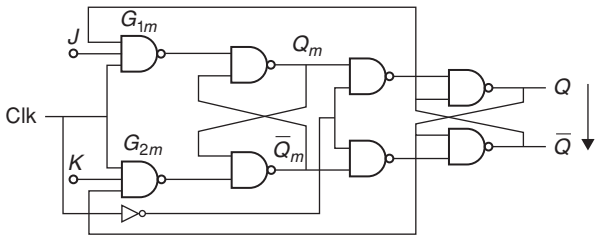


Figure 8 Logic diagram of JK flip-flop

Positive clock pulse is applied to the first latch and the clock pulse will be inverted before its arrival at the second latch. When Clk = 1, the first latch is enabled and the outputs Q_m and $\bar{Q}_m$ responds to the inputs J and K, according to the truth table of JK latch. At this time the 2nd latch is inhibited because its clock is low $(\overline{\text{Clk}} = 0)$. When the clock goes low (Clk = 0), the first latch is inhibited and the second is enabled. Therefore, the outputs Q and $\bar{Q}$ follow the outputs Q_m and $\bar{Q}_m$, respectively. Since the second latch simply follows the first one, it is referred to as slave and the first one as the master. Hence this configuration is known as master-slave JK flip-flop. In this circuit, the input to the gate G_{1m} and G_{2m} do not change, during the clock pulse levels.

The race around condition does not exist.

Table 2 *State/characteristic Table*

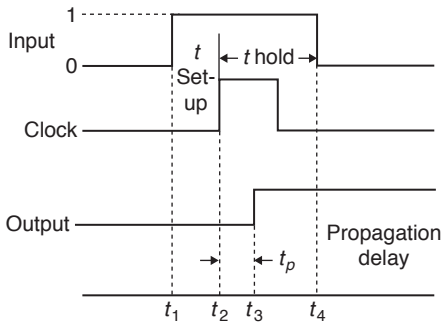
Clk	J	K	Q_t	Q_{t+1}	
↓	0	0	0	0	Q_1
↓	0	0	1	1	
↓	1	0	0	1	1
↓	1	0	1	1	
↓	0	1	0	0	0
↓	0	1	1	0	
↓	1	1	0	1	$\bar{Q}_t$
↓	1	1	1	0	

Q \ JK	00	01	11	10
0			1	1
1	1			1

$$Q_{t+1} = J\bar{Q}_t + Q_t\bar{K}$$

(ii) Flip-flop switching time: In designing circuits with flip-flop the following parameters are important:

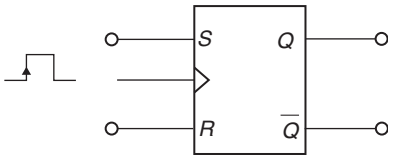
1. **Set-up time:** The minimum amount of time required for the data input to be present before the clock arrived.
2. **Hold time:** The minimum amount of time that the data input to be present after the clock trigger arrived.
3. **Propagation delay:** The amount of time it takes for the output to change states after an input trigger.



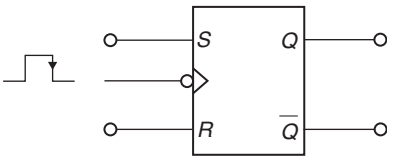
For example, t setup = 50 m sec and t hold = 5 m sec, the data bit has to be the input at least 50 m sec before the clock bit arrives and hold at least 5 m sec after the clock edge.

(iii) Triggering of flip-flop: The flip-flop can be triggered to set or reset either at one of the edges of the clock pulse. There are three types of triggering as described below:

1. **Positive edge triggering flip-flop:** These set or reset at the positive (rising or leading) edge of the clock pulse depending upon the state of i/p signal and o/p remain steady for 1 clock period. Positive edge triggering is indicated by an arrow head at the clock terminal of the flip-flop.



2. **Negative edge triggered flip-flop:** There are flip-flops those in which state transmissions take place only at the negative edge (falling or trailing) of the clock signal. Negative edge triggering is indicated by arrow head with bubble at the clock terminal.



3. **Level triggering:** Level triggering means the specified action occurs based on the steady state value of the input. That is, when a certain level is reached (0 or 1) the output will change states level triggering will be used in latches.

(iv) *D* flip-flop: It receives the designation from its ability to hold data into its internal storage. An SR/JK flip-flop has two inputs. It requires two inputs S/J and R/K to store 1 bit. This is a serious disadvantage in many application to overcome the difficulty D flip-flop has been developed which has only one input line. A D flip-flop can be realized using a SR/JK as show in the figure below.

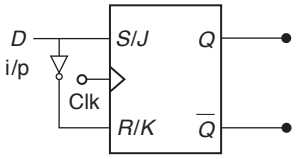


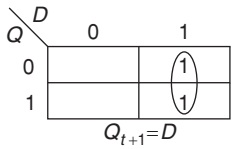
Table 3 *Truth Table*

clk	D	Q_{t+1}
↑	X	Q_t
↑	0	0
↑	1	1

There is no raising problem with D flip-flop. High or 1 state will set the flip-flop and a low or 0 state will reset the flip-flop. The presence of inverter at the input ensure that S/J and R/K inputs will always be in the opposite state.

Table 4 *Characteristic Table of D Flip-flop*

Q_t	D	Q_{t+1}
0	0	0
0	1	1
1	0	0
1	1	1



From the characteristic table of D.flip-flop, the next state of the flip-flop is independent of the present state since $Q_{t+1} = D$, whether $Q_t = 0$ or 1.

(v) *T* flip-flop: In a JK flip-flop $J = K = 1$ and the resulting flip-flop is referred to as a T flip-flop.

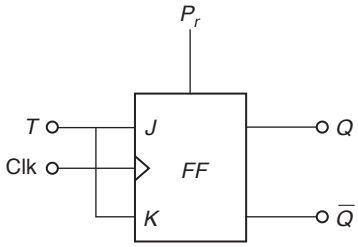


Table 5 *Truth Table*

Clk	T	Q_{n+1}
↑	0	Q_n
↑	1	$\overline{Q}_n$
↑	x	Q_n

If $T = 1$, it acts as a toggle switch for every Clk pulse with high input, the Q changes to its opposite state.

Table 6 *Characteristic Table*

Q_t	T	Q_{t+1}
0	0	0
0	1	1
1	0	1
1	1	0
1	0	1

Q \ T	0	1
0		1
1	1	

$$Q_{t+1} = T\overline{Q}_t + Q_t\overline{T}$$

(vi) Excitation table of flip-flops: The truth table of flip-flop is also referred to as the characteristic table, which specifies the operational characteristic of flip-flop.

Sometimes we come across situations in which present state and the next state of the circuit are known and we have to find the input conditions that must prevail to cause the desired transition of the state.

Consider initially JK flip-flop output $Q_n = 1, \overline{Q}_n = 0$, after clock pulse it changed to $Q_{n+1} = 0, \overline{Q}_{n+1} = 1$,

The input conditions, which made this transition, can be

Toggle – for $J = 1, K = 1, Q_{n+1} = \overline{Q}_n$

or

Reset – for $J = 0, K = 1, Q_{n+1} = 0, \overline{Q}_{n+1} = 1$

From the above conditions we can conclude that for transition $Q_n = 1$ to $Q_{n+1} = 0$ occurs when $J = 0$ (or) 1 (don't care) and $K = 1$.

Similarly, input conditions can be found out for all possible situations.

Table 7 *Excitation table of flip-flop.*

Present State	Next State	SR Flip-flop		JK Flip-flop		T Flip-flop	D Flip-flop
Q_n	Q_{n+1}	S	R	J	K	T	D
0	0	0	×	0	×	0	0
0	1	1	0	1	×	1	1
1	0	0	1	×	1	1	0
1	1	×	0	×	0	0	1

These excitation tables are useful in the design of synchronous circuits.

(vii) State diagrams of flip-flops: State diagram is a directed graph with nodes connected with directed arcs. State of the circuit is represented by the node, the directed arcs represent the state transitions, from present state (node) to next state (node) at the occurrence of clock pulse.

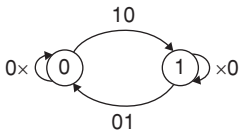


Figure 9 State diagram of SR flip-flop

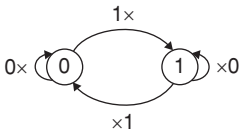


Figure 10 State diagram of JK flip-flop

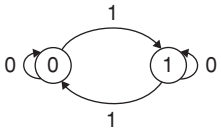


Figure 11 State diagram of *T* flip-flop

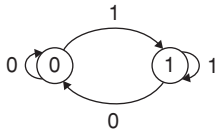


Figure 12 State diagram of *D* flip-flop

(viii) Conversion of one flip-flop to other flip-flop

Conversion of *T* flip-flop to JK flip-flop

1. Write the characteristic table of required flip-flop (here JK).
2. Write the excitation table of available or given Flip-flop (here *T*).
3. Solve for inputs of given flip-flop in terms of required flip-flop inputs and output.

Table 8 *JK flip-flop characteristic and T flip-flop excitation table*

JK Flip-flop Characteristic Table		T Flip-flop Excitation Table		
J	K	Q_n	Q_{n+1}	T
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	1
1	0	1	1	0
1	1	0	1	1
1	1	1	0	1

J \ KQ_n	00	01	11	10
0			1	
1	1		1	1

$$T = J\overline{Q}_n + KQ_n$$

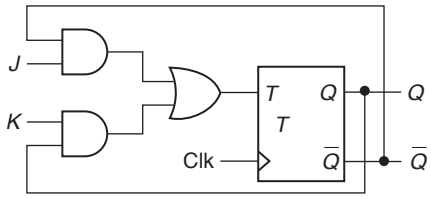


Figure 13 *D* Flip-flop by using other flip-flops

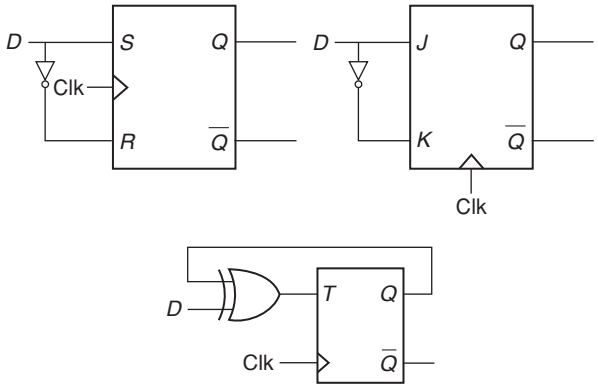
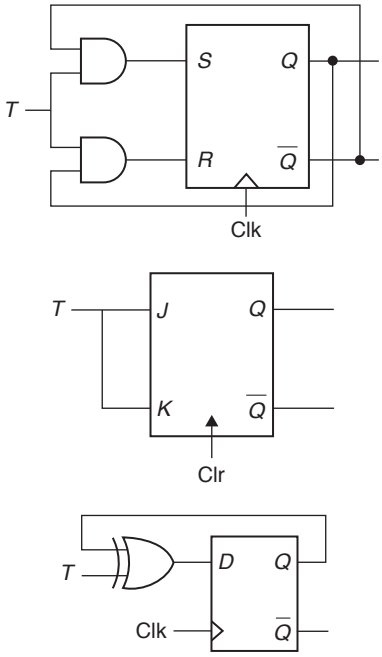
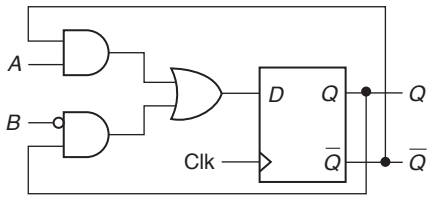


Figure 14 *T* flip-flop by using other flip-flops



Example 3: A sequential circuit using *D* flip-flop and logic gates is shown in the figure, where *A* and *B* are inputs and *Q* is output.



The circuit is

(A) SR flip-flop with inputs $A = S, B = R$

(B) SR flip-flop with inputs $A = \overline{R}, B = S$

(C) JK flip-flop with inputs $A = J, B = K$

(D) JK flip-flop with inputs $A = K, B = \overline{J}$

Solution: (C)

The characteristic equation of *D* flip-flop is

$$Q_{n+1} = D$$

Here input $D = A\overline{Q}_n + \overline{B}Q_n$

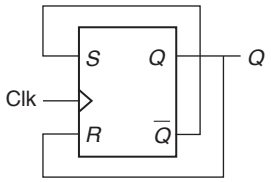
So, output $Q_{n+1} = A\overline{Q}_n + \overline{B}Q_n$

By comparing this equation with characteristic equation of JK

$$Q_{n+1} = J\overline{Q}_n + \overline{K}Q_n$$

If $A = J, B = K$, then this circuit works like JK flip-flop.

Example 4: The input Clk frequency for the flip-flop given is 10 kHz, then the frequency of *Q* will be



(A) 10 kHz (B) 5 kHz

(C) 20 kHz (D) 2.5 kHz

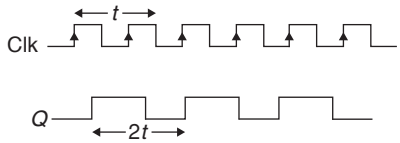
Solution: (B)

Form circuit we can say $S = \overline{Q}_n, R = Q_n$.

If initially $(Q_n, \overline{Q}_n) = (0, 1)$, then inputs $(S, R) = (1, 0)$, by applying clk pulse $(Q_{n+1}\overline{Q}_{n+1})$ becomes $(1, 0)\ldots$

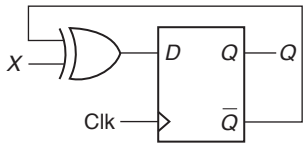
Clk	Q_n	$\overline{Q}_n$	S	R	Q_{n+1}	$\overline{Q}_{n+1}$
1	0	1	1	0	1	0
2	1	0	0	1	0	1
3	0	1	1	0	1	0
4	1	0	0	1	0	1

The output Q_{n+1} toggles for every clock pulse.



So frequency of $Q = \frac{1}{2t} = \frac{f}{2} = \frac{10}{2} = 5$ kHz

Examples 5: For the D flip-flop shown, if initially Q_n is set then what is the output state Q_{n+1} for $X = 0$, and for $X = 1$?



(A) 0, 0 (B) 0, 1
(C) 1, 0 (D) 1, 1

Solution: (B)
The characteristic equation of D is $Q_{n+1} = D$
Here $D = X \oplus \overline{Q_n}$
So $Q_{n+1} = X \oplus \overline{Q_n}$
We have $Q_n = 1$ (Q_n is set) for $X = 0$

$$Q_{n+1} = 0 \oplus 0 = 0$$

We have $Q_n = 1$ (Q_n is set), for $X = 1$

$$Q_{n+1} = 1 \oplus 0 = 1$$

Applications of flip-flops:

1. Data storage: A group of flip-flops connected in series/parallel is called a register, to store a data of N-bits, N-flip-flops are required. Data can be stored in parallel or serial order. Similarly, serial to parallel conversion and parallel to serial conversion can be done by using registers.
2. Counting: A number of flip-flops can be connected in a particular fashion to count the pulses applied (Clk) electronically. One flip-flop can count 2 Clk pulses, two flip-flops can count up to $2^2 = 4$ pulses, similarly n flip-flops can count up to 2^n pulses. Flip-flops may be used to count up/down.
3. Frequency division: Flip-flops may be used to divide input signal frequency by any number. A single flip-flop may be used to divide the input frequency by 2. Similarly n flip-flops may be used to divide the input frequency by 2^n. Output of a MOD-n counter (i.e., which counts n states) will divide input frequency by n.

Counters

Digital counters consist of a number of flip-flops. Their function is to count the number of clock pulses arriving at its clock input.

(i) Counter classification: Counters are classified according to their operational characteristic. Some of these characteristics include:

1. Counter triggering techniques
2. Frequency division characteristic
3. Counter modulus
4. Asynchronous or synchronous

In a synchronous counter all flip-flops are clocked simultaneously. In asynchronous counter the flip-flops are not clocked simultaneously. Each flip-flop is triggered by the previous flip-flop.

(ii) Asynchronous counters (ripple counters): Asynchronous counters do not have a common clock that controls all the flip-flop stages. The control clock is input to the first stage. The clock for each stage subsequent is obtained from the flip-flop of the prior stages. Let us analyze the 3-bit counter and its corresponding wave form diagram shown below.

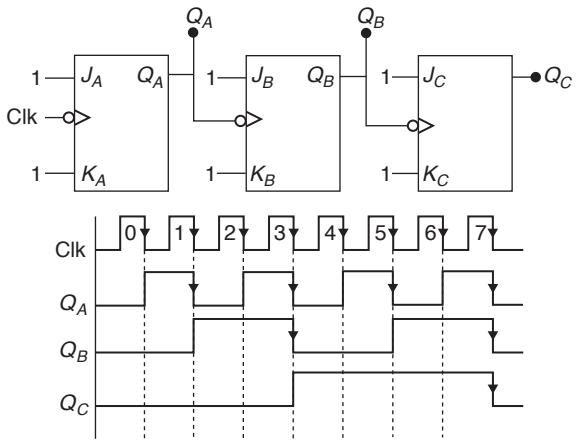


Figure 15 Timing diagrams

- The counter has three flip-flops and three output bits, therefore it is a three stage counter.
- The input clock does not trigger the three flip-flops, therefore it is an asynchronous counter.
- The J and K inputs are tied together as kept high. So they are considered to be toggle flip-flops.
- The flip-flops are negative edge triggered.
- The wave form analysis reveals that Q_A is the LSB and that its frequency is $\frac{1}{2}$ the input clock frequency. Further more, Q_c is the MSB and its frequency is $\frac{1}{8}$ the input clock frequency.
- The count sequence is 000, 001, 010, 011, 100, 101, 110, 111 where the LSB is Q_A. Thus it is MOD-8 binary up counter.
- Asynchronous counters are also known as ripple counters because the effect of the input clock ripples through the counter until it reaches the final stage.

Asynchronous Counter Design

Step I: Write the counting sequence.
Step II: Tabulate the values of reset signals. R for various state of counter.
Step III: Obtain the minimal expression for R and $\overline{R}$ using K-map or any other method.
Step IV: Provide a feedback such that R or $\overline{R}$ resets all the flip-flops after the desired count.

Table 9 *Identification of up/down Counters*

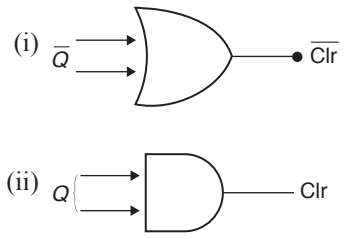
Clock Triggering	Q	Type
+ve edge	$\overline{Q}$	Up
+ve edge	Q	Down
–ve edge	$\overline{Q}$	Down
–ve edge	Q	Up

Clock is negative triggering pulse and Q is connected to next level clock, it is acting like a up counter.

Table 10 *Identification of GATE to Clear the Flip-flops*

Input to the Gate	Output of the Gate	Type of Gate
$\overline{Q}$	$\overline{Clr}$	OR
$\overline{Q}$	Clr	NOR
Q	$\overline{Clr}$	NAND
Q	Clr	AND

Example:

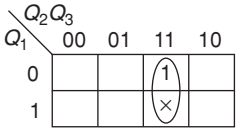


Example 6: Design and Implement a MOD-6 asynchronous counter using T flip-flops.

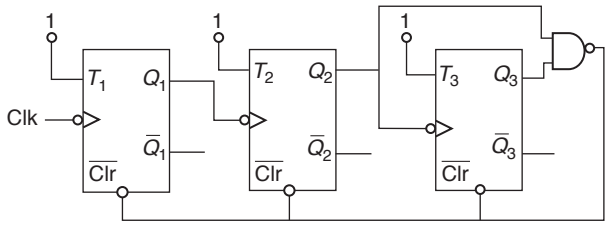
Solution: Counting sequence is 00, 001, 010, 011, 100, 101

After Pulses	States Q_3, Q_2, Q_1	Reset R
0	000	0
1	001	0
2	010	0
3	011	0
4	100	0
5	101	0
6	110	1
7	↓↓↓	
	000	0
	111	X

From the Truth table $R = Q_3 Q_2$
For active Low $\overline{R}$ is used.
$\therefore$ $R = 0$ for 000 to 101
$R = 1$ for 110
$R = X$ for 111
$\therefore$ K-map is



$\therefore$ $R = Q_2 Q_3$
Logic diagram is



Asynchronous Decode Counter

A ripple counter is an asynchronous sequential circuit, clock is applying only for LSB side. Decade ripple counter it counts from 0 to 9 for up counter.

MOD-10 counter it counts starting from 0000 to 1001. If the NAND gate output is logic '0' at that instant the counter reset to initial state.

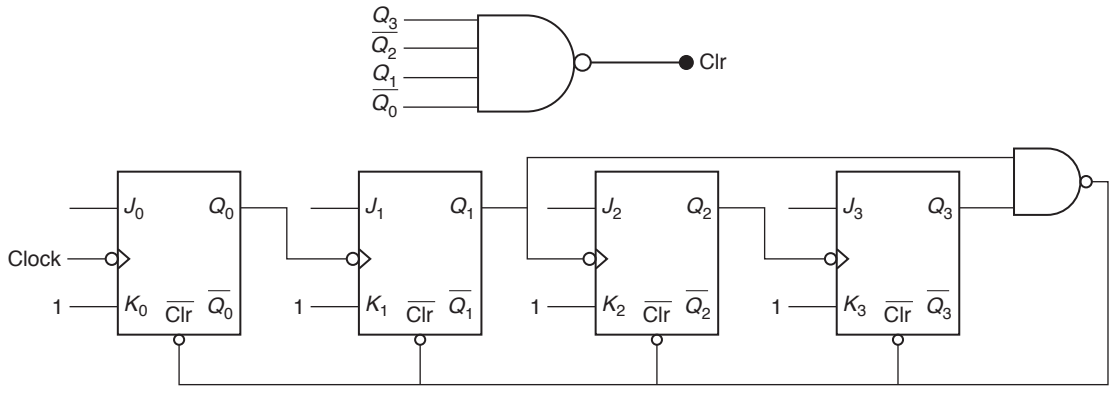


Figure 16 MOD-10 or decade counter

To design a MOD-N counter minimum number of flip-flops required is

$N \le 2^n$

where $N \rightarrow$ MOD

$n \rightarrow$ No. of flip-flops

Example:

MOD-5 counter

$5 \le 2^n$

$\therefore n = 3$

Operating Clock Frequency

(i) Synchronous counter:

$$f_{Clk} \le \frac{1}{t_{pd}}$$

(ii) Asynchronous counter:

$$f_{Clk} \le \frac{1}{n t_{pd}}$$

Output frequency of the MOD-N counter is

$$\Rightarrow f_o = \frac{f_{Clk}}{N}.$$

(iii) Synchronous counter: When counter is clocked such that each flip-flop in the counter is triggered at the same time, the counter is called as synchronous counter.

- Synchronous counters have the advantage of high speed and less severe decoding problems.
- Disadvantage is having more circuiting than that of asynchronous counter.

Synchronous Series Carry Counters

For normal ring counters to count N sequence total N flip-flops are required.

Unused states in ring counter = $2^N - N$.

Unused states in Johnson ring counter = $2^N - 2N$.

Asynchronous counters are slower than the synchronous counters. By using synchronous series carry adders we can design MOD-N counter with n Flip-flops-only.

For non-binary counters $N \le 2^n$

3-bit series carry up counter

It counts from initial state 000 to 111.

$\therefore$ MOD = 2^n = 8 states

$\therefore$ MOD-8

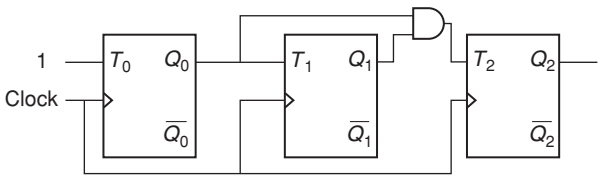


Figure 17 3-bit series carry counter

$$f_{Clk} \le \frac{1}{t_{pd} + (n-2)t_{pd\ AND}}$$

where

$t_{pd} \rightarrow$ Propagation delay of each flip-flop.

$t_{pd\ AND} \rightarrow$ Propagation delay of AND gate.

$n \rightarrow$ Number of flip-flops.

In this, Q_o toggles for every clock pulse.

Q_1 toggles when Q_o is 1.

Q_2 toggles when o/p of AND gate is logic 1.

Note: To design a synchronous series carry down counter. Connect $\overline{Q_o}$ to the next flip-flop input.

Design of Synchronous Counter

Step I: Determine the required number of flip-flop.

Step II: Draw the state diagram showing all possible states.

Step III: Select the type of flip-flop to be used and write the excitation table.

Step IV: Obtain the minimal expressions for the excitations of the FFs using the K-maps.

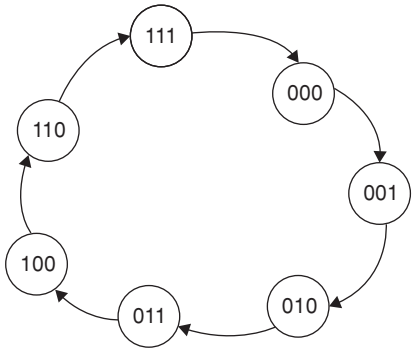
Step V: Draw a logic diagram based on the minimal expression. Let us employ these techniques to design a MOD-8 counter to count in the following.

Example 7: Sequence: 0, 1, 2, 3, 4, 5, 6, and 7. Design a synchronous counter by using JK flip-flops.

Solution:

Step I: Determine the required number of flip-flops. The sequence shows a 3-bit up counter that requires 3 flip-flops.

Step II: Draw the state diagram.

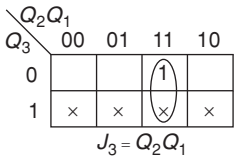


Step III: Select the type of flip-flop to be used and write the excitation table.

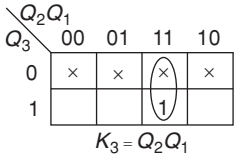
JK flip-flop is selected and excitation table of a 3-bit up counter is

PS	*NS*	Required Excitation
$Q_3\ Q_2\ Q_1$	$Q_3\ Q_2\ Q_1$	$J_3\ K_3\ J_2\ K_2\ J_1\ K_1$
0 0 0	0 0 1	0 x 0 x 1 x
0 0 1	0 1 0	0 x 1 x x 1
0 1 0	0 1 1	0 x x 0 1 x
0 1 1	1 0 0	1 x x 1 x 1
1 0 0	1 0 1	x 0 0 x 1 x
1 0 1	1 1 0	x 0 1 x x 1
1 1 0	1 1 1	x 0 x 0 1 x
1 1 1	0 0 0	x 1 x 1 x 1

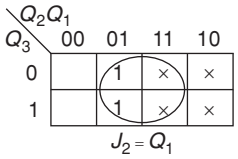
Step IV: Obtain the minimal expression using K-map.



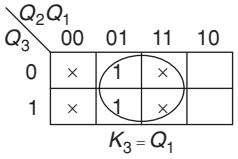
$J_3 = Q_2Q_1$



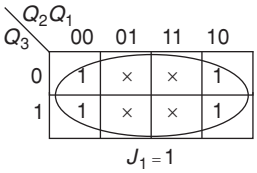
$K_3 = Q_2Q_1$



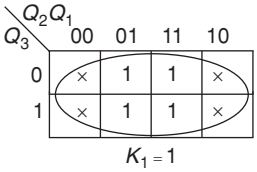
$J_2 = Q_1$



$K_3 = Q_1$



$J_1 = 1$



$K_1 = 1$

Step V: Draw the logic diagram based on the minimal expression.

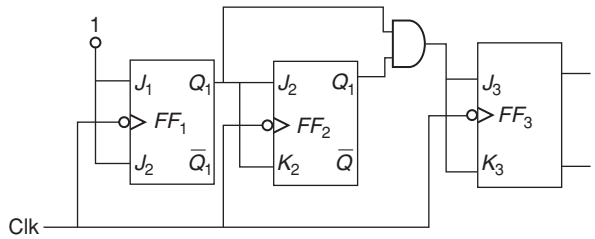


Table 11 *Comparison between asynchronous counter and synchronous counter*

Asynchronous Counter	Synchronous Counter
1. In this type of counter, flip-flops are connected in such a way that output of first flip-flop drives the clock for the next flip-flop	In this type there is no connection between output of first flip-flop and clock input of the next flip-flop
2. All the flip-flops are not clocked simultaneously	All the flip-flops are clocked simultaneously
3. Logic circuit is very simple even for more number of states	Design involves complex logic circuits as number of state increases
4. Main draw back of these counters is their low speed as the clock is propagated through number of flip-flops before it reaches last flip-flop	As clock is simultaneously given to all flip-flops, there is no problem of propagation delay. Hence they are preferred when number of flip-flops increases in the given design.

The main drawback of ripple counters is their high delays, if propagation delay of each flip-flop is assumed as x, then to get output of the first flip-flop it takes x, i.e., after x seconds the second flip-flop will get its clock pulse from previous stage, and output of second flip-flop will be out after another x seconds, similarly the final output of last flip-flop will be after nx seconds, where n is the number of flip-flops. So the propagation delay of ripple counter is nx, which is directly proportionate to the number of flip-flops.

The maximum frequency of operation of ripple counter is inverse of delay, $f_{max} = \frac{1}{nx}$

Maximum operating frequency is the highest frequency at which a sequential circuit can be reliably triggered. If the clock frequency is above this maximum frequency the flip-flops in the circuit cannot respond quickly and the operation will be unreliable.

In case of synchronous counters (synchronous circuits) as clock is applied simultaneously to all the flip-flops, the output of all the flip-flops change by x seconds (delay of one flip-flop) and this delay is independent of number of flip-flops used in circuit.

The maximum frequency of operation of synchronous counter is inverse of delay $f_{max} = \frac{1}{x}$

Example 8: The maximum operation frequency of a MOD-64 ripple counter is 33.33 kHz, the same flip-flops are used to design a MOD-32 synchronous counter, and then the maximum operating frequency of the new counter is

(A) 400 kHz (B) 200 kHz
(C) 40 kHz (D) 500 kHz

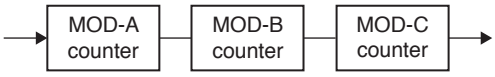
Solution: For ripple counter $f_{max} = \frac{1}{nx}$, given is a MOD-64 ripple counter, i.e., 2^6 states, so $n = 6$ flip-flops are required.

$$x = \frac{1}{33.33K \times 6} = 5\mu S$$

For synchronous counter

$$f_{max} = \frac{1}{x} = \frac{1}{5\ \mu S} = 0.2\ \text{MHz} = 200\ \text{kHz}$$

When multiple counters are connected in cascade, then the total number of states of the new counter is $A \times B \times C$, i.e., it will work as MOD-$A \times B \times C$ counter.



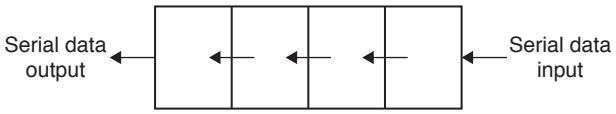
For example, decade counter counts from 0 to 9, 10 states – If two such decade counters are connected in cascade, then the total counting states will be 10 × 10 = 100, it will work as MOD-100 counter, which counts from 00 to 99.

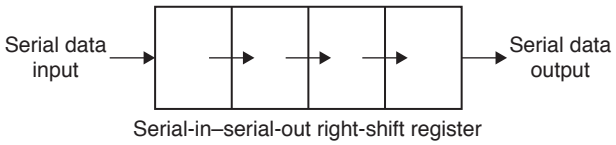
Registers

A number of flip-flops connected together such that data may be shifted into and shifted out of them is called a shift register. There are four basic types of shift register:

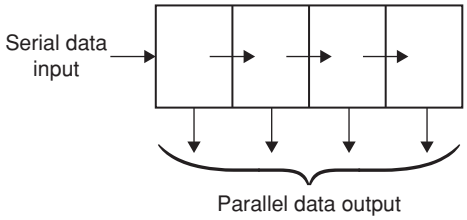
1. Serial-in–serial-out
2. Serial-in–parallel-out
3. Parallel-in–serial-out
4. Parallel-in–serial-out

(i) Serial-in–serial-out:

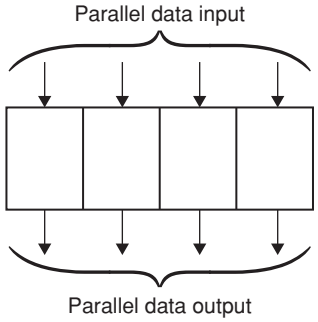




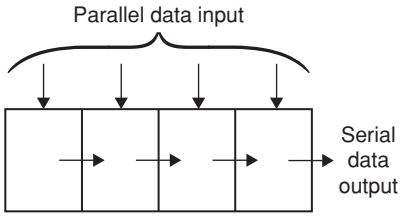
(ii) Serial-in–parallel-out:



(iii) Parallel-in–parallel-out:



(iv) Parallel-in–serial-out:



Serial input and serial output register: This type of shift register accepts data serially, i.e., one bit at a time and also outputs data serially. The logic diagram of 4-bit serial input, serial output, shift-right, shift register is shown in the following figure. With four D flip-flops the register can store up to four bits of data.

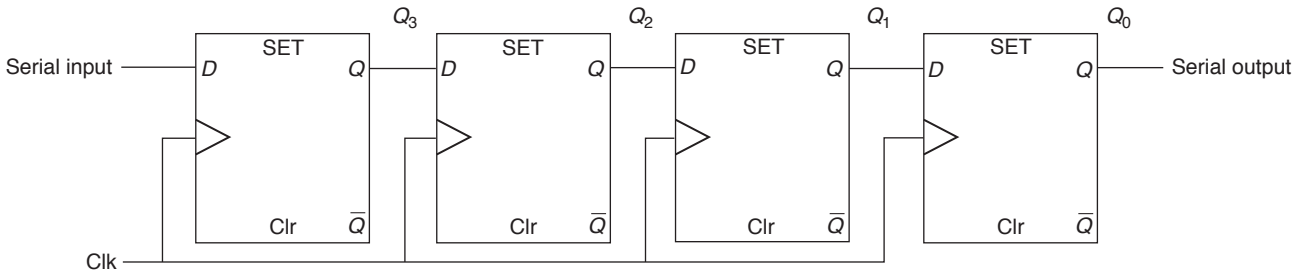


Figure 18 Serial input and serial output register

If initially, all flip-flops are reset, then by applying serial input 1101, the flip-flop states will change as shown in below table.

Clk	S.I	Q_3	Q_2	Q_1	Q_0
0	1	0	0	0	0
1	0	1	0	0	0
2	1	0	1	0	0
3	1	1	0	1	0
4		1	1	0	1

The first data bit 1 will appear at serial output after 4 clock pulses.

Application of Shift Registers

1. Delay line: Serial input and serial output shift register can be used to introduce delay in digital signals.

   $$\text{Delay} = \text{no.of flip-flops} \times \frac{1}{\text{Clk frequency}} = \text{No. of flip-flops} \times \text{time period of clock pulse}$$

2. Serial to parallel, parallel to serial converter: SIPO, PISO registers used for data conversion.
3. Sequence generator: A circuit, which generates a prescribed sequence of bits, with clock pulses is called as sequence generator
   The minimum number of flip-flops 'n' required to generate a sequence of length 'S' bits is given by $S \le 2^n - 1$

Shift register counters

One of the applications of the shift register is that they can be arranged to work as ring counters. Ring counters are constructed by modifying the serial-in, serial-out, shift registers. There are two types of ring counters—basic ring counter and twisted ring counter (Johnson counter). The basic ring counter is obtained from SISO shift register by connecting serial output to serial input.

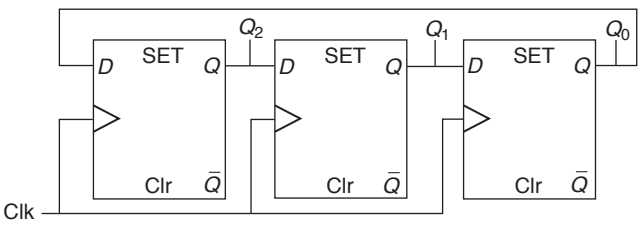
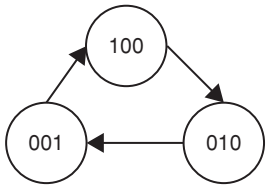


Figure 19 Ring counter

In most instances, only a single 1 or single 0 is in the register and is made to circulate around the register as long as the clock pulses are applied. Consider initially first flip-flop is set, and others are reset. After 3 clock pulses, again we will get initial state of 100. So this is a MOD-3 counter.

Clk	Q_2	Q_1	Q_0
0	1	0	0
1	0	1	0
2	0	0	1
3	1	0	0
4	0	1	0



A ring counter with N flip-flops can count up to N states, i.e., MOD-N counter, whereas, N-bit asynchronous counter can count up to 2^N states. So, ring counter is uneconomical compared to a ripple counter, but has the advantage of requiring no decoder. Since it is entirely synchronous operation and requires no gates for flip-flop inputs, it has further advantage of being very fast.

Twisted ring counter (Johnson counter): This counter is obtained from a SISO shift register by connecting the complement of serial output to serial input as shown in below figure.

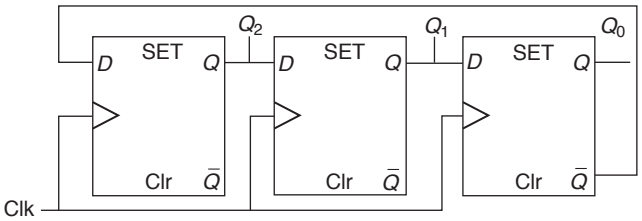
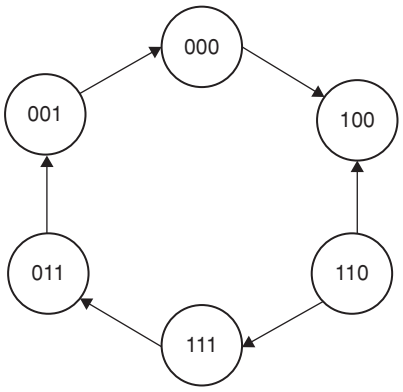


Figure 20 Twisted Ring Counter

Let initially all the FFs be reset, after each clock pulse the complement of last bit will appear as at MSB, and other bits shift right side by 1-bit. After 6 clock pulses the register will come to initial state 000. Similarly, the 3-bit Johnson counter will oscillate between the states 101, 010.

Clk	Q_2	Q_1	Q_0
0	0	0	0
1	1	0	0
2	1	1	0
3	1	1	1
4	0	1	1
5	0	0	1
6	0	0	0



An n-bit Johnson counter can have $2n$ unique states and can count up to $2n$ pulses, so it is a MOD-$2n$ counter. It is more economical than basic ring counter but less economical than ripple counter.

Solved Examples

Example 1: Assume that 4-bit counter is holding the count 0101. What will be the count after 27 clock pulses?

Solution: Total clock pulses: 27 = 16 + 11
0101 + 1011 = 0000

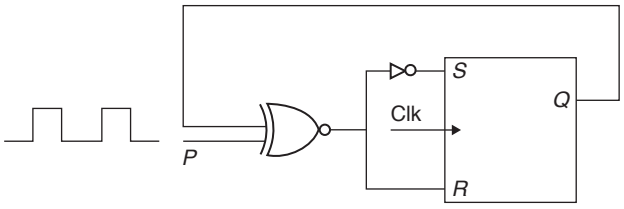
Example 2: A MOD-2 counter followed by MOD-5 counter is

Solution: A decade counter, counts 10 states (5 × 2).

Example 3: A 4-bit binary ripple counter uses flip-flops with propagation delay time of 25 msec each. The maximum possible time required for change of state will be

Solution: The maximum time = 4 × 25 ms = 100 ms

Example 4: Consider the circuit, the next state Q^+ is



Solution

P	Q	S	R	Q^+
0	0	0	1	0
0	1	1	0	1
1	0	1	0	1
1	1	0	1	0

So, $Q^+ = P \oplus Q$

Example 5: A certain JK FF has t_{pd} = 12 n sec what is the largest MOD counter, that can be constructed from these FF and still operate up to 10 MHz?

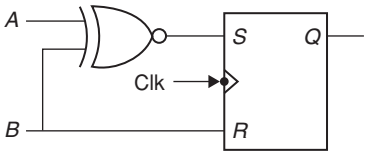
Solution: $N \le \dfrac{1}{f_{\max} \cdot t_{pd}}$

$f_{\max}$ = 10 MHz $N \le 8$
t_{pd} = 12 ns

$$N \le \frac{1}{10 \times 10^6 \times 12 \times 10^{-9}}$$

MOD counter is = $2^N = 2^8 = 256$

Example 6: An AB flip-flop is constructed from an SR flip-flop as shown below. The expression for next state Q^+ is

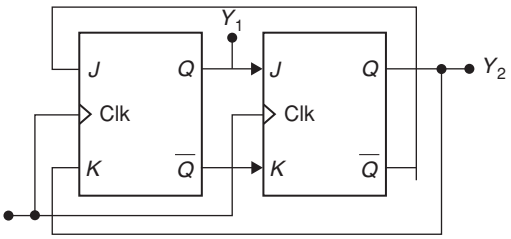


Solution:

A	B	Q	S	R	Q^+
0	0	0	1	0	1
0	0	1	1	0	1
0	1	0	0	1	0
0	1	1	0	1	0
1	0	0	0	0	0
1	0	1	0	0	1
1	1	0	1	1	×
1	1	1	1	1	×

$\therefore Q^+ = \overline{A}\overline{B} + AQ = \overline{A}\overline{B} + \overline{B}Q$

Example 7: In the circuit shown below, the output y_1 and y_2 for the given initial condition $y_1 = y_2 = 1$ and after four input pulses will be



Solution:
After 1st pulse $y_1 = 0, y_2 = 1$
After 2nd pulse $y_1 = 0, y_2 = 0$
After 3rd pulse $y_1 = 1, y_2 = 0$
After 4th pulse $y_1 = 1, y_2 = 1$

Example 8: A ripple counter is to operate at a frequency of 10 MHz. If the propagation delay time of each flip-flop in the counter is 10 ns and the storbing time is 50 ns, how many maximum stages can the counter have?

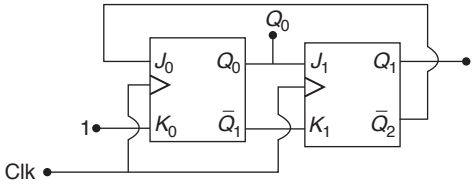
Solution: $nt_{pd} + t_s \le \frac{1}{f}$

where, n = number of stages
t_{pd} = propagation delay time
t_s = strobing time
f = frequency of operation = $10 \times 10^{-9} n + 50 \times 10^{-9}$

$$\le \frac{1}{10 \times 10^6}$$

(or) $10n + 50 \le 100$
(or) $10n \le 50$
For max stages $n = \frac{50}{10} = 5$

Example 9: In the circuit assuming initially $Q_0 = Q_1 = 0$. Then the states of Q_0 and Q_1 immediately after the 33rd pulse are

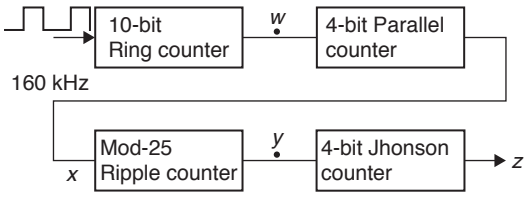


Solution:

J_0	K_0	J_1	K_1	Q_0	Q_1	Count
1	1	0	1	0	0	Initial
1	1	1	0	1	0	1st pulse
0	1	0	1	0	1	2nd
1	1	0	1	0	0	3rd
1	1	1	0	1	0	4th
0	1	0	1	0	1	5th pulse

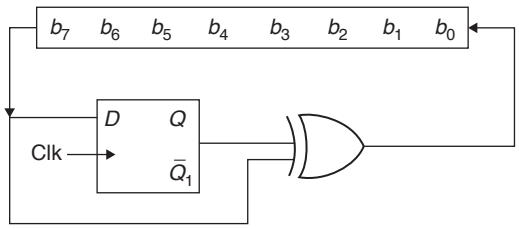
After 4th pulse, output is same as after 1st one, so, sequence gets repeated. So output after 33rd pulse would be same as after 3rd pulse. i.e., (00).

Example 10: The frequency of the pulse at z in the network shown in figure is



Solution: 10-bit ring counter is a MOD-10. So, it divides the 160 kHz input by 10. Therefore, w = 16 kHz. The 4-bit parallel counter is a MOD-16. Thus, the frequency at x = 1 kHz. The MOD-25 ripple counter produces a frequency at y = 40 Hz (1 kHz/25 = 40 Hz). The 4-bit Johnson counter is a MOD-8. The frequency at Z = 5Hz.

Example 11: The 8-bit shift left shift register, and D flip-flop shown in the figure is synchronized with the same clock. The D flip-flop is initially cleared. The circuit acts as

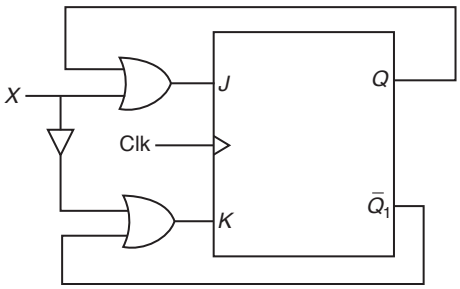


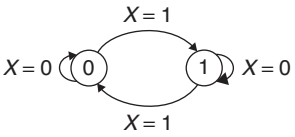
Solution: The output of XOR gate is $Z = b_{i+1} \oplus b_i$ and this output shift the register to left. Initially, $Z = 0$
After 2nd clock $Z = b_7 \oplus 0 = b_7$
After 2nd clock $Z = b_7 \oplus b_6$
3rd clock $Z = b_6 \oplus b_5$
4th clock $Z = b_5 \oplus b_4$
It is a binary to gray code converter.

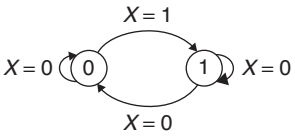
Example 12: A 4-bit MOD-16 ripple counter uses JK flip-flops. If the propagation delay of each flip-flop is 50 ns sec, the maximum clock frequency that can be used is equal to

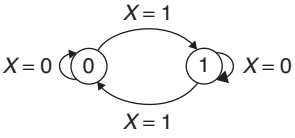
Solution: Max = clock frequency $= \frac{1}{4 \times 50 \times 10^{-9}} = 5$ MHz

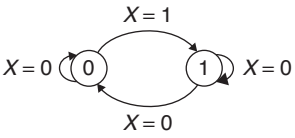
Example 13: What is the state diagram for the sequential circuit shown?



(A)


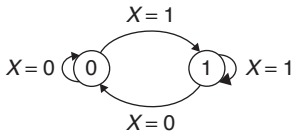
(B)


(C)


(D)


Solution: (D)
State diagram of a sequential circuit will have states (output) of all the flip-flops.

Present state	Next state	Q_{n+1}
Q_n	For $x = 0$	For $x = 1$
0	0	1
1	0	1



EXERCISES

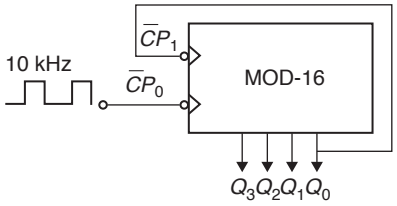
Practice Problems I

Directions for questions 1 to 22: Select the correct alternative from the given choices.

1. How many flip-flops are needed for MOD-16 ring counter and MOD-16 Johnson counter?
(A) 16, 16 (B) 16, 8
(C) 4, 3 (D) 4, 4

2. A 2-bit synchronous counter uses flip-flops with propagation delay time of 25 n sec, each. The maximum possible time required for change of state will be
(A) 25 n sec (B) 50 n sec
(C) 75 n sec D) 100 n sec

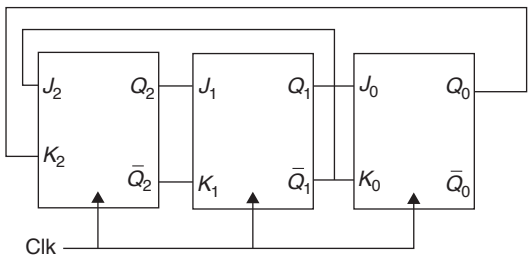
3. For given MOD-16 counter with a 10 kHz clock input determine the frequency at Q_3



(A) 625 Hz (B) 10 kHz
(C) 2.5 kHz (D) 0 Hz

4. A 4-bit ripple counter and a 4-bit synchronous counter are made using flip-flops having a propagation delay of 10 n sec each. If the worst case delay in the ripple counter and the synchronous counter be R and S, respectively, then
(A) $R = 10$ ns, $S = 40$ ns (B) $R = 40$ ns, $S = 10$ ns
(C) $R = 10$ ns, $S = 30$ ns (D) $R = 30$ ns, $S = 10$ ns

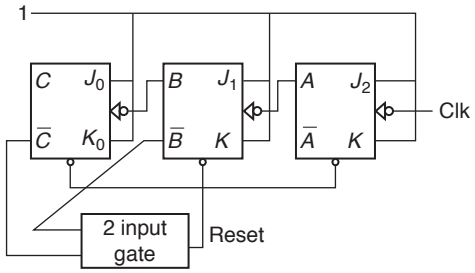
5. The counter shown in the figure has initially $Q_2Q_1Q_0 = 000$. The status of $Q_2Q_1Q_0$ after the first pulse is



(A) 001 (B) 010
(C) 100 (D) 101

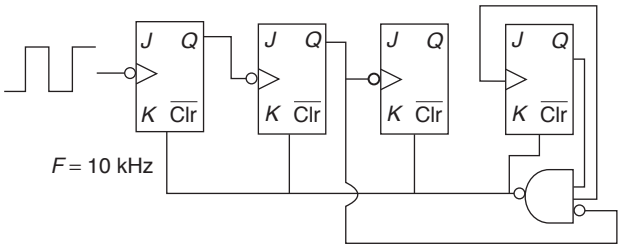
6. 12 MHz clock frequency is applied to a cascaded counter of MOD-3 counter, MOD-4 counter and MOD-5 counter. The lowest output frequency is
(A) 200 kHz (B) 1 MHz
(C) 3 MHz (D) 4 MHz

7. In the modulo-6 ripple counter shown in the figure below, the output of the 2-input gate is used to clear the JK flip-flops. The 2-input gate is



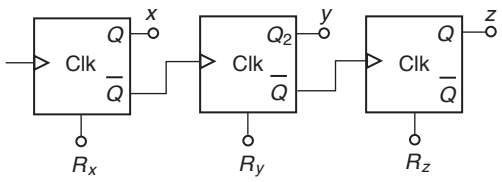
(A) a NAND gate (B) a NOR gate
(C) an OR gate (D) an AND gate

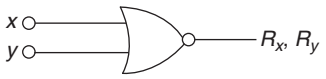
8. In figure, J and K inputs of all the 4 flip-flops are made high, the frequency of the signal at output y is

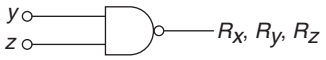


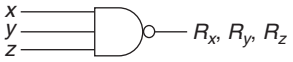
(A) 0.833 kHz (B) 1.0 kHz
(C) 0.91 kHz (D) 0.77 kHz

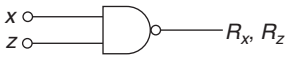
9. In a number system a counter has to recycle to 0 at the sixth count. Which of the connections indicated below will realize this resetting? (a logic '0' at the R inputs resets the counters)



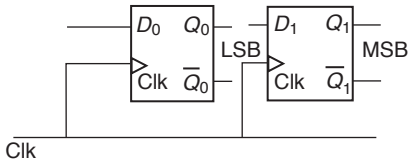
(A) 

(B) 

(C) 

(D) 

10. Two D flip-flops, as shown below, are to be connected as a synchronous counter that goes through the following Q_1Q_0 sequence $00 \rightarrow 01 \rightarrow 11 \rightarrow 10 \rightarrow 00$. The inputs D_0 and D_1 respectively should be connected as



(A) $\overline{Q}_0$ and Q_1 (B) $\overline{Q}_0$ and Q_1

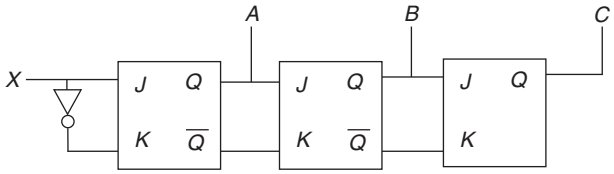
(C) $\overline{Q}_1\overline{Q}_0$ and $\overline{Q}_1Q_0$ (D) $\bar{Q}_1\bar{Q}_0$ and $\bar{Q}_1Q_0$

11. N flip-flops can be used to divide the input clock frequency by

(A) N (B) $2N$

(C) 2^N (D) 2^{N-1}

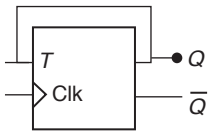
12. For a shift register as shown, $x = 1011$, with initially FF cleared, ABC will have value of after 3 clock pulses



(A) 101 (B) 011

(C) 001 (D) 111

13. If a FF is connected as shown what will be the output? (initially $Q = 0$)



(A) 11111 (B) 0000

(C) 1010 (D) 0101

14. The excitation table for a FF whose output conditions are if $AB = 00$, no change of state occurs
$AB = 01$, FF becomes 1 with next clock pulse
$AB = 10$, FF becomes 0 with next clock pulse
$AB = 11$, FF changes its state

(A)

Q_n	Q_{n+1}	A	B
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

(B)

Q_n	Q_{n+1}	A	B
0	0	1	x
0	1	0	x
1	0	x	0
1	1	x	1

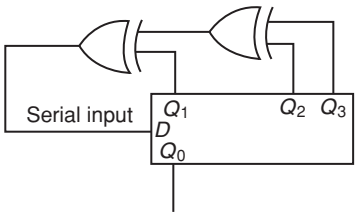
(C)

Q_n	Q_{n+1}	A	B
0	0	x	0
0	1	x	1
1	0	x	x
1	1	0	x

(D)

Q_n	Q_{n+1}	A	B
0	0	x	0
0	1	1	x
1	0	x	1
1	1	0	x

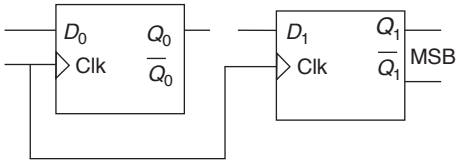
15. A shift register that shift the bits 1 position to the right at each clock pulse is initialized to 1100 (Q_0, Q_1, Q_2, Q_3). The outputs are combined using an XOR gate circuit and fed to the D input. After which clock pulse, will the initial pattern reappear at the output?



(A) 6th (B) 5th

(C) 4th (D) 7th

16. If we need to design a synchronous counter that goes through the states $00 \rightarrow 01 \rightarrow 11 \rightarrow 10 \rightarrow 00$ using D FF, what should be the input to the FF?



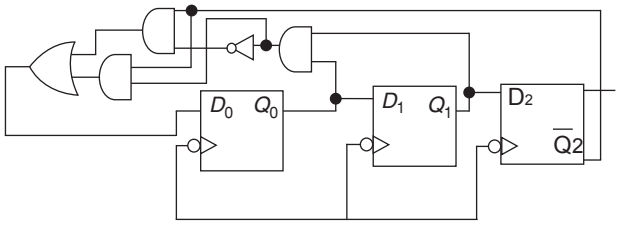
(A) $D_0 = Q_0, D_1 = \bar{Q}_1$

(B) $D_0 = \bar{Q}_1, D_1 = Q_0$

(C) $D_0 = \bar{Q}_1 \cdot Q_0, D_1 = \bar{Q}_1\bar{Q}_0$

(D) $D_0 = \bar{Q}_0, D_1 = Q_1$

17. Find the counter state sequence (Assume Q_0 as MSB).

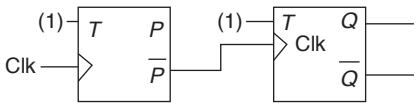


(A) 4, 6, 7, 3, 1, 0, 4 (B) 4, 6, 5, 3, 1, 0, 4

(C) 4, 5, 6, 7, 0, 4, 5 (D) 4, 6, 7, 1, 0, 4

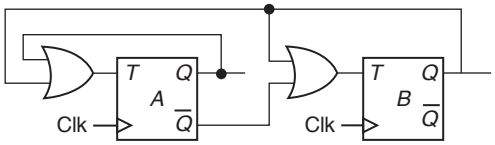
18. If the propagation delay of each FF is 50 ns, and for the AND gate to be 20 ns. What will be the f_{max} for MOD-32 ripple and synchronous counters?
(A) 14.3 MHz, 4 MHz (B) 14.3 MHz, 5 MHz
(C) 5 MHz, 14.3 MHz (D) 3.7 MHz, 14.3 MHz

19. For a given counter identify its behavior



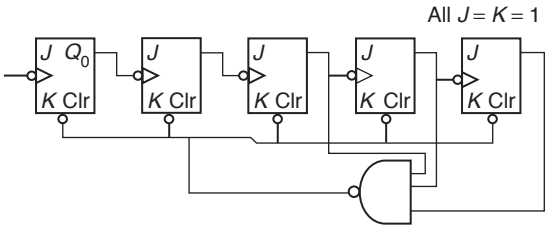
The output is taken from PQ.
(A) MOD-4 up counter
(B) MOD-2 down counter
(C) MOD-4 down counter
(D) MOD-2 up counter

20. A circuit using T FF is given. Identify the circuit.



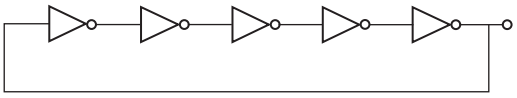
(A) MOD-2 counter
(B) MOD-4 counter
(C) MOD-3 counter
(D) MOD-2 generate 00, 10, 00

21. The MOD number of asynchronous counter shown



(A) 24 (B) 48
(C) 29 (D) 28

22. For the oscillator, find the fundamental frequency if propagation delay of each inverter is 1000 psec.



(A) 100 MHz (B) 10 MHz
(C) 1 GHz (D) 10 GHz

Practice Problems 2

Directions for questions 1 to 30: Select the correct alternative from the given choices.

1. Match List 1 (operation) with List 2 (associated device) and select the correct answer using the codes given below:

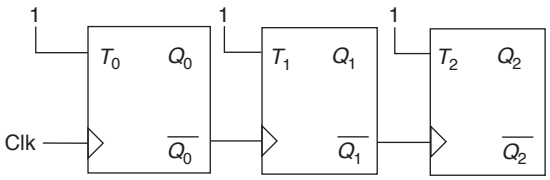
List 1	List 2
(a) Frequency Ddivision	(1) ROM
(b) Decoding	(2) Multiplexer
(c) Data selection	(3) Demultiplexer
(d) Code conversion	(4) Counter

(A) a–3, b–4, c–2, d–1
(B) a–3, b–4, c–1, d–2
(C) a–4, b–3, c–1, d–2
(D) a–4, b–3, c–2, d–1

2. A MOD-5 synchronous counter is designed by using JK flip-flop, the number of counts skipped by it will be
(A) 2 (B) 3
(C) 5 (D) 0

3. A counter starts off in the 0000 state, then clock pulses are applied. Some time later the clock pulses are removed and the counter flip-flops read 0011. How many clock pulses have occurred?
(A) 3 (B) 35
(C) 51 (D) Any of these

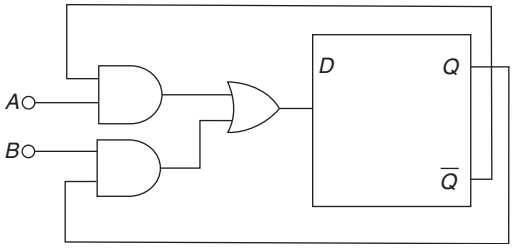
4. Figure below shown as ripple counter using positive edge triggered flip-flops. If the present state of the counters is $Q_2\,Q_1\,Q_0 = 011$, then its next state ($Q_2Q_1Q_0$) will be



(A) 010 (B) 100
(C) 111 (D) 101

5. A synchronous sequential circuit is designed to detect a bit sequence 0101 (overlapping sequence include). Every time, this sequence is detected, the circuit produces output of 1. What is the minimum number of states the circuit must have?
(A) 4 (B) 5
(C) 6 (D) 7

6. What is represented by digital circuit given below?



(A) An SR flip-flop with $A = S$ and $B = R$
(B) A JK flip-flop with $A = K$ and $B = J$
(C) A JK flip-flop with $A = J$ and $B = \overline{K}$
(D) An SR flip-flop with $A = R$ and $B = S$

7. In a ripple counter, the state whose output has a frequency equal to $\frac{1}{8}$th that of clock signal applied to the first stage, also has an output periodically equal to $\frac{1}{8}$th that of the output signal obtained form the last stage. The counter is
(A) MOD-8 (B) MOD-6
(C) MOD-64 (D) MOD-16

8. A flip-flop is popularly known as
(A) Astable multivibrator
(B) Bistable multivibrator
(C) Monostable multivibrator
(D) None of these

9. Which of the following represents the truth table for JK flip-flop?

(A)

J	K	Output
0	0	Q_0
0	1	0
1	0	1
1	1	$\overline{Q}_0$

(B)

J	K	Output
0	0	$\overline{Q}_0$
0	1	0
1	0	1
1	1	Q_0

(C)

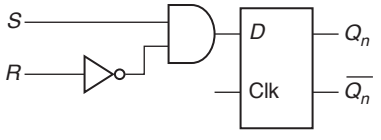
J	K	Output
0	0	Q_0
0	1	0
1	0	1
1	1	Invalid

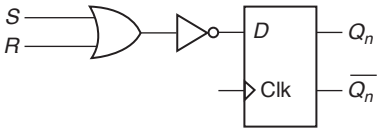
(D)

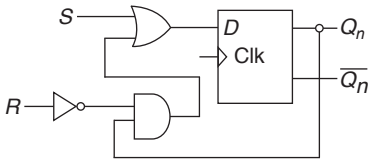
J	K	Output
0	0	1
0	1	0
1	0	1
1	1	0

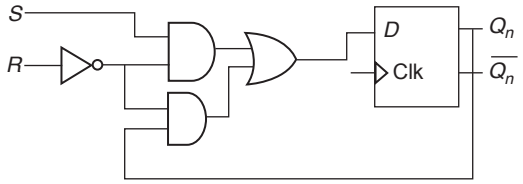
10. One disadvantage of master-slave FF is
(A) setup time becomes longer.
(B) it requires input to be held constant before clock transition.
(C) unpredictable output even if input held constant.
(D) hold time becomes longer.

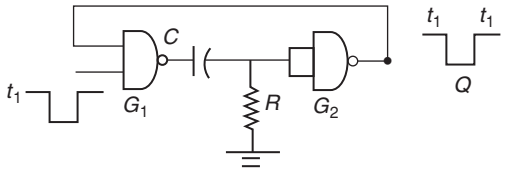
11. Which of the following converts D FF to SR FF?

(A)


(B)


(C)


(D)


12. Which of the circuit is being represented by the figure?


(A) NAND gate
(B) Monostable multivibrator
(C) Astable multivibrator
(D) Schmitt trigger

13. Hold time is
(A) time for which output is held constant.
(B) time for which clock is to be held constant on applying input.
(C) time for which input should be maintained constant after the triggering edge of clock pulse.
(D) time for which input should be maintained constant prior to the arrival of triggering edge of clock pulse.

14. Shift registers are made up of
(A) MOS inverters (B) FF
(C) Latches (D) None of these

15. Data from a satellite is received in serial form. If the data is coming at 8 MHz rate, how long will it take to serially load a word in 40-bit shift register?
(A) 1.6 μs (B) 5 μs
(C) 6.4 μs (D) 12.8 μs

16. A JK FF can be converted into T FF by connecting
(A) $\overline{Q}$ to 0
(B) 0 to $\overline{Q}$
(C) 0 to Q
(D) by connecting both J and K inputs to T

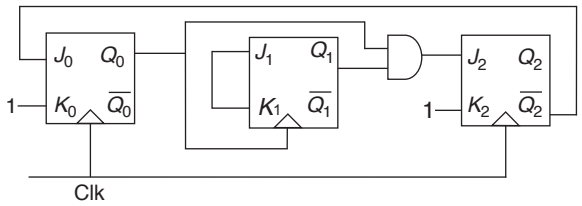
17. The flip-flop that is not affected by race around condition
(A) T FF (B) JK FF
(C) SR FF (D) None of these

18. The characteristic equation of JK FF is
(A) $J'Q(t) + KQ'(t)$ (B) $J'Q(t) + KQ(t)$
(C) $JQ'(t) + K'Q(t)$ (D) None of these

19. For a D.FF input, the s $\overline{Q}$ is connected. What would be the output sequence?
(A) 0000 (B) 1111
(C) 010101 (D) 101010

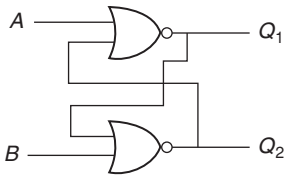
20. In order to implement a MOD-6 synchronous counter we have 3 FF and a combination of 2 input gate(s). Identify the combination circuit.
(A) One AND gate
(B) One OR gate
(C) One AND and one OR gate
(D) Two AND gates

21. Given a MOD-5 counter. The valid states for the counter are (0, 1, 2, 3, 4). The propagation delay of each FF is T_F and that of AND gate is t_A. The maximum rate at which counter will operate satisfactorily



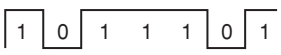
(A) $\frac{1}{t_F + t_A}$ (B) $\frac{1}{3t_F}$
(C) $\frac{1}{2t_F + t_A}$ (D) $\frac{1}{3t_F - t_A}$

22. For a NOR latch as shown up A and B are made first (0, 1) and after a few seconds it is made (1, 1). The corresponding output (Q_1, Q_2) are



(A) first (1, 0) then (0, 0)
(B) first (1, 0) then (1, 0)
(C) first (1, 0) then (1, 1)
(D) first (1, 0) then (0, 1)

23. In order to design a pulse generator to generate the wave form using a shift register, what is the number of FF required?

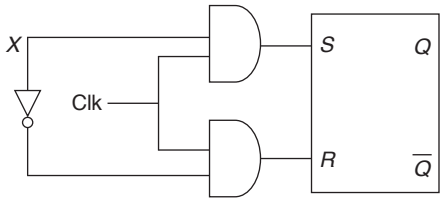


(A) 3 (B) 4
(C) 5 (D) 6

24. For what minimum value of propagation delay in each FF will a 10-bit ripple counter skip a count when it is clocked at 5 MHz?
(A) 10 ns (B) 20 ns
(C) 25 ns (D) 15 ns

25. A divide by 50 counter can be realized by using
(A) 5 no. of MOD-10 counter
(B) 10 no. of MOD-5 counter
(C) One MOD-5 counter followed by one MOD-10 counter
(D) 10 no. of MOD-10 counter

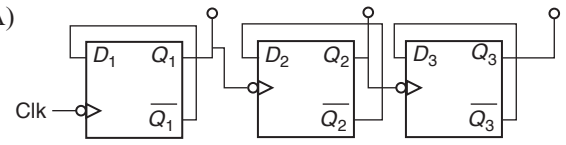
26. The following latch is



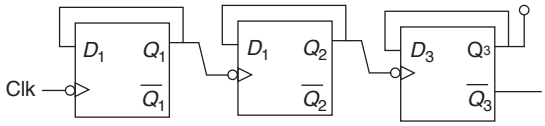
(A) D latch (B) T latch
(C) JK latch (D) RS latch

27. Which of the following represent a 3-bit ripple counter using D FF?

(A)

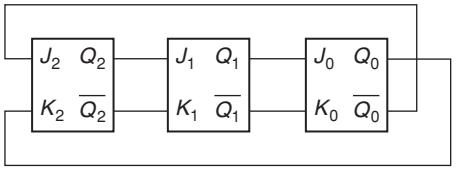


(B)



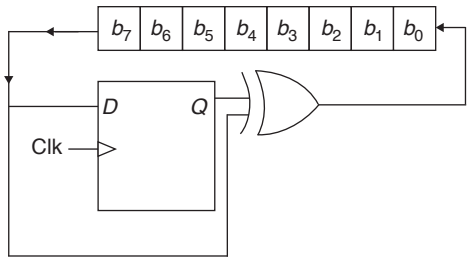
(C) Both (A) and (B)
(D) None of these

28. For the Johnson counter with initial Q_2, Q_1, Q_0 as 101, the frequency of the output is (Q_2, Q_1, Q_0)



(A) $\frac{f_c}{8}$ (B) $\frac{f_c}{6}$
(C) $\frac{f_c}{2}$ (D) $\frac{f_c}{4}$

29. For the given circuit the contents of register ($b_7 - b_0$) are 10010101, what will be the register contents after 8 clock pulses?



(A) 10010101 (B) 01101010
(C) 11011111 (D) 01101011

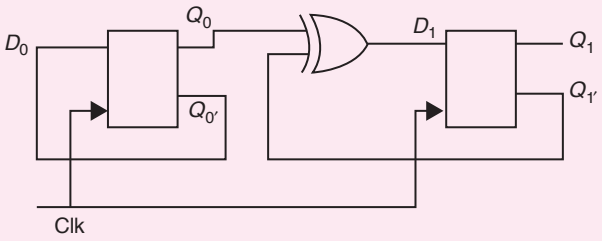
30. A latch is to be build with A and B as input. From the table find the expression for the next state Q^+

A	B	Q	Q^+
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

(A) A
(B) B
(C) $A+\overline{B}$
(D) $A\overline{B}+AB$

Previous Years' Questions

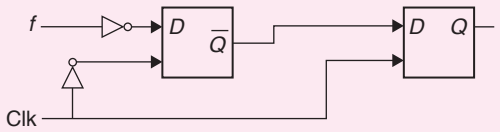
1. Consider the following circuit.

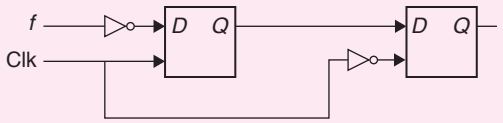


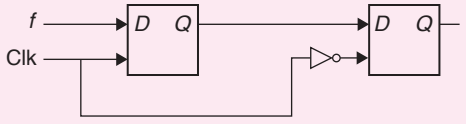
The flip-flops are positive edge triggered D FFs. Each state is designated as a 2-bit string Q_0Q_1. Let the initial state be 00. The state transition sequence is **[2005]**

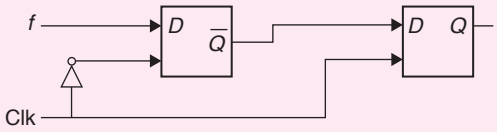
(A) 00 → 11 → 01
(B) 00 → 11
(C) 00 → 11 → 01 → 11
(D) 00 → 11 → 01 → 10

2. You are given a free running clock with a duty cycle of 50% and a digital waveform f which changes only at the negative edge of the clock. Which one of the following circuits (using clocked D flip-flops) will delay the phase of f by 180°? **[2006]**

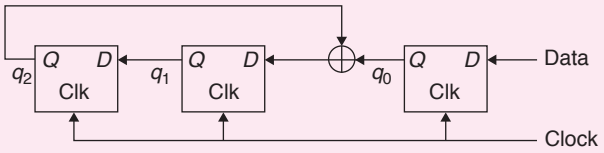
(A)


(B)


(C)


(D)


3. Consider the circuit in the diagram. The ⊕ operator represents Ex-OR. The D flip-flops are initialized to zeros (cleared). **[2006]**



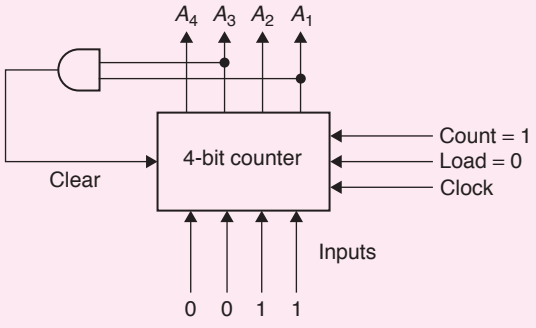
The following data: 100110000 is supplied to the data terminal in 9 clock cycles. After that the values of $q_2q_1q_0$ are

(A) 000 (B) 001
(C) 010 (D) 101

4. The control signal functions of a 4-bit binary counter are given below (where X is 'don't care'):

Clear	Clock	Load	Count	Function
1	X	X	X	Clear to 0
0	X	0	0	No change
0	↑	1	X	Load input
0	↑	0	1	Count next

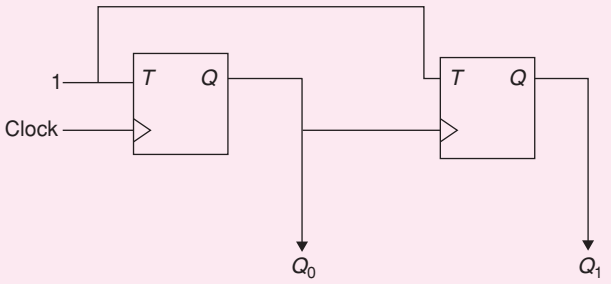
The counter is connected as follows:



Assume that the counter and gate delays are negligible. If the counter starts at 0, then it cycles through the following sequence: **[2007]**

(A) 0, 3, 4 (B) 0, 3, 4, 5
(C) 0, 1, 2, 3, 4 (D) 0, 1, 2, 3, 4, 5

5. In the sequential circuit shown below, if the initial value of the output Q_1Q_0 is 00, what are the next four values of Q_1Q_0? **[2010]**

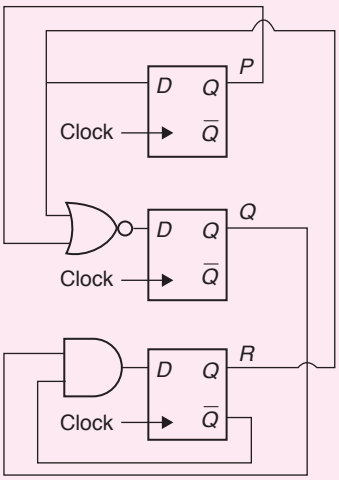


(A) 11, 10, 01, 00 (B) 10, 11, 01, 00
(C) 10, 00, 01, 11 (D) 11, 10, 00, 01

6. The minimum number of D flip-flops needed to design a MOD-258 counter is **[2011]**

(A) 9 (B) 8
(C) 512 (D) 258

Common Data for Questions 7 and 8: Consider the following circuit involving three D-type flip-flops used in a certain type of counter configuration.



7. If all the flip-flops were reset to 0 at power on, what is the total number of distinct outputs (states) represented by PQR generated by the counter? **[2011]**

(A) 3 (B) 4
(C) 5 (D) 6

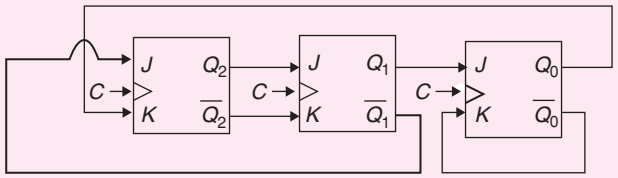
8. If at some instance prior to the occurrence of the clock edge, P, Q, and R have a value 0, 1, and 0, respectively, what shall be the value of PQR after the clock edge? **[2011]**

(A) 000 (B) 001
(C) 010 (D) 011

9. Let $K = 2^n$. A circuit is built by giving the output of an n-bit binary counter as input to an n-to-2^n-bit decoder. This circuit is equivalent to a **[2014)**

(A) K-bit binary up counter
(B) K-bit binary down counter
(C) K-bit ring counter
(D) K-bit Johnson counter

10.



The above synchronous sequential circuit built using JK flip-flops is initialized with $Q_2Q_1Q_0$ = 000. The state sequence for this circuit for the next 3 clock cycles is **[2014]**

(A) 001, 010, 011 (B) 111, 110, 101
(C) 100, 110,111 (D) 100, 011, 001

11. Consider a 4-bit Johnson counter with an initial value of 0000. The counting sequence of this counter is **[2015]**

(A) 0, 1, 3, 7, 15, 14, 12, 8, 0
(B) 0, 1, 3, 5, 7, 9, 11, 13, 15, 0
(C) 0, 2, 4, 6, 8, 10, 12, 14, 0
(D) 0, 8, 12, 14, 15, 7, 3, 1, 0

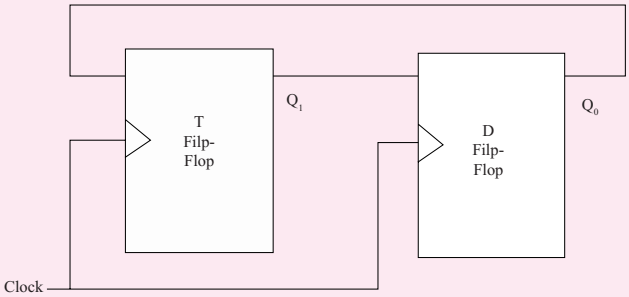
12. A positive edge-triggered D–flip-flop is connected to a positive edge-triggered JK flip-flop as follows. The Q output of the D flip-flop is connected to both the J and K inputs of the JK flip-flop, while the Q output of the JK flip-flop is connected to the input of the D flip-flop. Initially, the output of the D flip-flop is set to logic one and the output of the JK flip-flop is cleared. Which one of the following is the bit sequence (including the initial state) generated at the Q output of the JK flip-flop when the flip-flops are connected to a free-running common clock? Assume that $J = K = 1$ is the toggle mode and $J = K = 0$ is the state-holding mode of the JK flip-flop. Both the flip-flops have non-zero propagation delays. **[2015]**

(A) 0110110… (B) 0100100…
(C) 011101110… (D) 011001100…

13. The minimum number of JK flip-flops required to construct a synchronous counter with the count sequence (0, 0, 1, 1, 2, 2, 3, 3, 0, 0, …) is _____ **[2015]**

14. We want to design a synchronous counter that counts the sequence 0-1-0-2-0-3 and then repeats. The minimum number of *J-K* flip-flops required to implement this counteris _____ . **[2016]**

15. Consider a combination of T and D flip-flops connected as shown below. The output of the D flip-flop is connected to the input of the T flip-flop and the output of the T flip-flop is connected to the input of the D flip-flop.



Initially, both Q_0 and Q_1 are set to 1 (before the 1st clock cycle). The outputs **[2017]**

(A) $Q_1 Q_0$ after the 3rd cycle are 11 and after the 4th cycle are 00 respectively

(B) $Q_1 Q_0$ after the 3rd cycle are 11 and after the 4th cycle are 01 respectively

(C) $Q_1 Q_0$ after the 3rd cycle are 00 and after the 4th cycle are 11 respectively

(D) $Q_1 Q_0$ after the 3rd cycle are 01 and after the 4th cycle are 01 respectively

16. The next state table of a 2-bit saturating up-counter is given below.

Q_1	Q_0	Q_1^+	Q_0^+
0	0	0	1
0	1	1	0
1	0	1	1
1	1	1	1

The counter is built as a synchronous sequential circuit using T flip-flops. The expressions for T_1 and $T_0$are **[2017]**

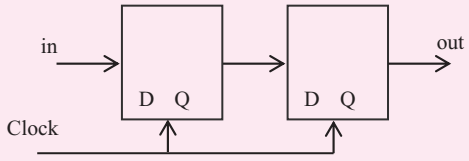
(A) $T_1 = Q_1 Q_{0,} \qquad T_0 = \overline{Q}_1 \overline{Q}_0$

(B) $T_1 = \overline{Q}_1 Q_{0,} \qquad T_0 = \overline{Q}_1 + \overline{Q}_0$

(C) $T_1 = Q_1 + Q_{0,} \qquad T_0 = \overline{Q}_1 + \overline{Q}_0$

(D) $T_1 = \overline{Q}_1 Q_{0,} \qquad T_0 = Q_1 + Q_0$

17. Consider the sequential circuit shown in the figure, where both flip-flops used are positive edge-triggered D flip-flops.



The number of states in the state transition diagram of this circuit that have a transition back to the same state on some value of "in" is _____. **[2018]**

Answer Keys

Exercises

Practice Problems 1

1. B	**2.** A	**3.** A	**4.** B	**5.** C	**6.** A	**7.** C	**8.** A	**9.** B	**10.** A
11. C	**12.** B	**13.** B	**14.** C	**15.** D	**16.** B	**17.** A	**18.** D	**19.** A	**20.** C
21. D	**22.** A								

Practice Problems 2

1. D	**2.** B	**3.** D	**4.** B	**5.** A	**6.** C	**7.** C	**8.** B	**9.** A	**10.** B
11. C	**12.** B	**13.** C	**14.** B	**15.** B	**16.** D	**17.** C	**18.** C	**19.** C	**20.** D
21. C	**22.** A	**23.** D	**24.** B	**25.** C	**26.** A	**27.** A	**28.** C	**29.** C	**30.** A

Previous Years' Questions

1. D	**2.** C	**3.** C	**4.** C	**5.** A	**6.** A	**7.** B	**8.** D	**9.** C	**10.** C
11. D	**12.** A	**13.** $3(8 = 2^3)$		**14.** 3	**15.** B	**16.** B	**17.** 2		