6 Integrated-Circuit Logic Families

Multiple Choice Questions

Q.1 Consider the following statements describing the property of a complementary MOS (CMOS) inverter:

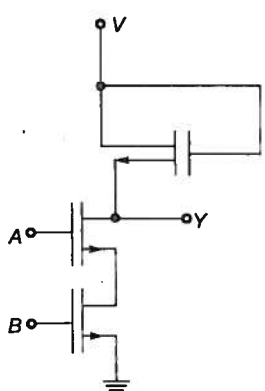
1. It is a combination of an n-channel FET and a p-channel FET.
2. There is power dissipation when the input carries the logical 1 signal.
3. There is no power dissipation when the input carries the logical 1 signal.
4. There is power dissipation during transition from 0 to 1 or from 1 to 0.

Which of the statements given above are correct?

(a) 1, 2 and 3 (b) 2, 3 and 4
(c) 1, 3 and 4 (d) 1, 2 and 4

[ESE-2006]

Q.2 The NMOS circuit shown below is a gate of the type



(a) NAND (b) NOR
(c) AND (d) EXCLUSIVE - OR

[ESE-2003(EE)]

Q.3 A inverter gate has guaranteed output levels as: logic '1' = 3.8 V and logic '0' = 0.7 V. The maximum low level input voltage at which the output remains high = 2 V. The minimum high-level input voltage at which the output remains low = 3.1 V. What are the noise margins of this gate?

(a) $NM_H = 2.4$ V, $NM_L = 1.8$ V
(b) $NM_H = 1.8$ V, $NM_L = 1.3$ V
(c) $NM_H = 0.7$ V, $NM_L = 1.8$ V
(d) $NM_H = 0.7$ V, $NM_L = 1.3$ V

[ESE-2004(EE)]

Q.4 For a logic family

V_{OH} is the minimum output high level voltage
V_{OL} is the maximum output low level voltage
V_{IH} is the minimum acceptable input high level voltage
V_{IL} is the maximum acceptable input low level voltage

The correct relationship among these is:

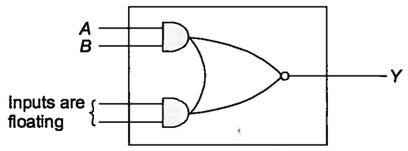
(a) $V_{IH} > V_{OH} > V_{IL} > V_{OL}$
(b) $V_{OH} > V_{IH} > V_{IL} > V_{OL}$
(c) $V_{IH} > V_{OH} > V_{OL} > V_{IL}$
(d) $V_{OH} > V_{IH} > V_{OL} > V_{IL}$ **[ESE-1999]**

Q.5 The open collector output of two 2-input NAND gates are connected to a common pull-up resistor. If the inputs of the gates are A, B and C, D respectively, the output is equal to

(a) $\overline{AB}\,\overline{CD}$ (b) $\overline{AB} + \overline{CD}$
(c) $AB + CD$ (d) $AB \times CD$

[ESE-2002]

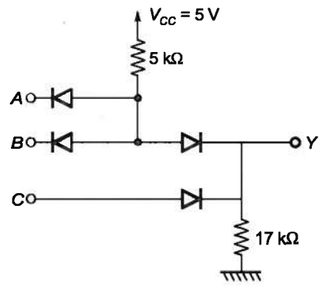
Q.6 The figure shows the internal schematic of a TTL AND-OR-Invert (AOI) gate. For the inputs shown in the figure, the output Y is



(a) 0 (b) 1
(c) AB (d) $\overline{AB}$

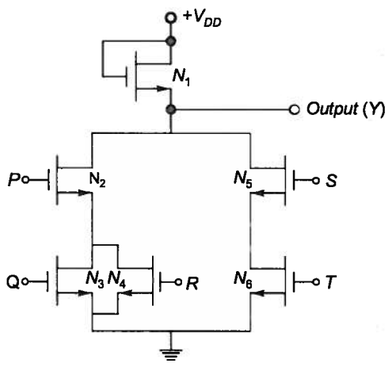
[GATE-2004]

Q.7 The logical expression for the output 'Y' of the diode circuit below is



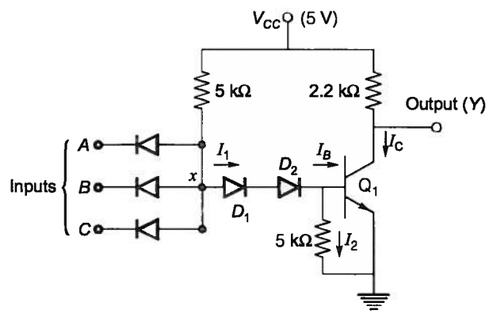
(a) $(A+B)C$ (b) $\overline{A+B}+C$
(c) $(\overline{A+B})C$ (d) $AB+C$

Q.8 An NMOS circuit is shown in the figure below:



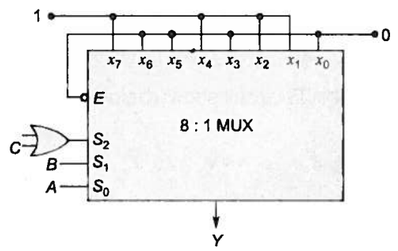
The logical expression for the output (Y) equals to
(a) $\overline{P(Q+R)+ST}$ (b) $P(\overline{Q+R})\cdot ST$
(c) $P+(\overline{QR})(S+T)$ (d) $(\overline{P+Q})R+\overline{S}\,\overline{T}$

Q.9 Consider a DTL circuit as given below:



If all the inputs (A, B, C) are high then,
(a) Input diodes D_1 is ON and D_2 is OFF, Q_1 is in cut-off mode and $Y=\overline{ABC}$.
(b) Input diodes D_1 and D_2 is ON, Q_1 is in active mode and $Y=\overline{A+B+C}$.
(c) Input diodes D_1 and D_2 is ON, Q_1 is in saturation mode and $Y=\overline{ABC}$.
(d) Input diodes D_2 is ON and D_1 is OFF, Q_1 is in saturation and $Y=ABC$.

Q.10 In the TTL circuit in the figure, S_2, S_1 and S_0 are select lines and x_7 and x_0 are input lines. S_0 and x_0 are LSBs. The output Y is



(a) indeterminate (b) $A\oplus B$
(c) $\overline{A\oplus B}$ (d) $\overline{C}(\overline{A\oplus B})+C(A\oplus B)$

[GATE-EC:2001]

Q.11 Which of the following is not a type of output configuration in TTL gates?
(a) Totem-pole output
(b) Open-collector output
(c) Transmission-Gate output
(d) Tri-state output

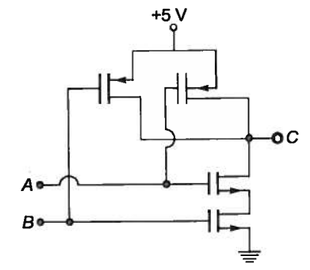
Q.12 The DTL, TTL, ECL and CMOS family of digital ICs are compared in the following 4 columns

	(P)	(Q)	(R)	(S)
Fanout is minimum	DTL	DTL	TTL	CMOS
Power Consumption is minimum	TTL	CMOS	ECL	DTL
Propagation delay is minimum	CMOS	ECL	TTL	TTL

The correct column is
(a) P (b) Q
(c) R (d) S

[GATE-EC:2003]

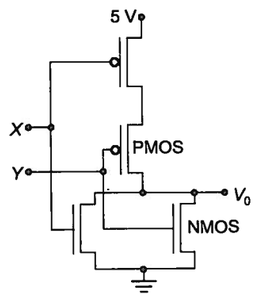
Q.13 Identify the logic gate given in the figure.



(a) NOR (b) NAND
(c) AND (d) OR

[GATE-IN:2005]

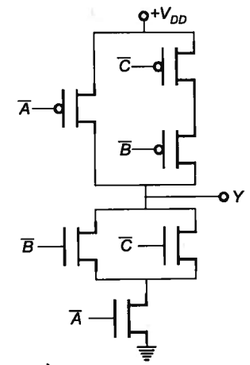
Q.14 A CMOS implementation of a logic gate is shown in the following figure:



The boolean logic function realized by the circuit is
(a) AND (b) NAND
(c) NOR (d) OR

[GATE-IN:2007]

Q.15 The expression for output "Y" for the circuit given below is



(a) $\overline{A}\cdot(\overline{B}+\overline{C})$ (b) $A+BC$
(c) $\overline{A}+\overline{BC}$ (d) $A(B+C)$

Q.16 The switching speed of ECL is very high, because the transistors
(a) are switched between cut-off and saturation region
(b) are switched between active and saturation region
(c) are switched between active and cut-off region
(d) may operate in any of the three regions

Q.17 The figure of merit of a logic family is given by
(a) Gain bandwidth product
(b) (Propagation delay time) × (power dissipation)
(c) (Fan out) × (Propagation delay time)
(d) (Noise-margin) × (Power dissipation)

Q.18 Match **List-I** with **List-II** and select the correct answer using the code given below the Lists:

List-I		List-II
A. HTL	1.	High fan-out
B. CMOS	2.	Highest speed of operation
C. I^2L	3.	High noise immunity
D. ECL	4.	Lowest product of power & delay

Codes:

	A	B	C	D
(a)	3	4	1	2
(b)	2	4	1	3
(c)	3	1	4	2
(d)	2	1	4	3

Numerical Data Type Questions

Q.19 The inverter 74 AL S01 has the following specifications:
$I_{OH\,max}$ = –0.4 mA, $I_{OL\,max}$ = 8 mA,
$I_{IH\,max}$ = 20 μA, I_{ILmax} = –0.1 mA.
The fan out based on the above will be_____.

Q.20 An IC family has an average propagation delay of 10 ns and an average power dissipation of 5 mW. Figure of merit of IC family is_____ pJ.

Try Yourself

T1. The fan-out of the TTL gate having
I_{OH} = – 8 μA, I_{IH} = 40 μA, I_{OL} = 16 mA,
I_{IL} = –1.6 mA is equal to _____.

T2. The transistors used in a portion of the TTL gate shown in the figure have a β = 100. The base-emitter voltage of is 0.7 V for a transistor in active region and 0.75 V for a transistor in saturation. If the sink current I = 1 mA and the output is at logic 0, then the current I_R will be equal to ____mA.