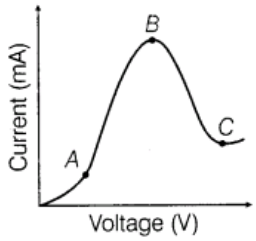
Chapter 14. Semiconductor Electronics

Semiconductor, Diode and its Application

1 Mark Questions

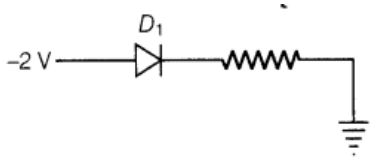
1.The graph shown in the figure represents a plot of current versus voltage for a given semiconductor. Identify the region, if any over which the semiconductor has a negative resistance. [All India 2013]



Ans. Resistance of a material can be found out by the slope of the curve V versus I. Part BC of the curve shows the negative resistance as with the increase in current and decrease in voltage.

2.What happens to the width of depletion layer of a p-n junction when it is
(i)forward biased?
(ii)reverse biased? [All India 2011]
Ans.(i) Width of depletion layer's decreases in forward bias
(ii) Width depletion layer increases in reverse bias.

3.Why cannot we take one slab of p-type semiconductor and physically join it to another slab of n-type semiconductor to get p-n junction?

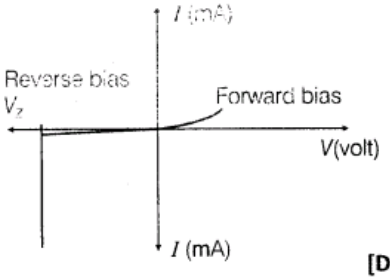


Ans.In this way, continuous contact cannot be produced at atomic level and junction will behave as a discontinuity for the flowing charge carrier.

4.What is the most common use of photo diode? [All India 2009]
Ans. The photodiode can be used as a photodetector to detect optical signals

5.State the relation between the frequency v of radiation emitted by LED and the band gap energy E, of the semiconductor used to fabricate it.[All India 2009 C]
Ans.Zener diode, which is used as a DC voltage regulator.

6.Figure show the I-V characteristics of a given device. Name the device and write where it is used.



[Delhi 2009]

Ans.

In LED, energy of the photon should be equal to or less than the band gap energy i.e.

$$h\nu \leq E_g$$

where, E_g = band gap energy,

ν = frequency of emitted photon.

7.State the reason, why GaAs is most commonly used in making of a solar cell. [All India 2008]

Ans.solar radiation is nearly 1.5 eV. In order to have photo excitation, the energy of radiation (hv) must be greater than energy band gap (E_g). Therefore, the semiconductor with energy band gap about 1.5 eV or lower than it and with higher absorption coefficient is likely to give better solar conversion efficiency. The energy band gap for Si is about 1.1 eV, while for GaAs, it is about 1.53 eV. The GaAs is better inspite of its higher band gap than Si because it absorbs relatively more energy from the incident solar radiations being of relatively higher absorption coefficient.

8.At what temperature would an intrinsic semiconductor behave like a perfect insulator? [Delhi 2008 C]

Ans. At O° K temperature, an intrinsic semiconductor behaves like a perfect insulator

9.Why should a photo diode be operated at reverse bias?[All India 2008]

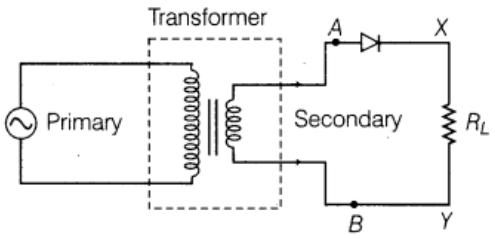
Ans.The photodiodes are used to detect the optical signals. The fraction change in minority

carrier in case of reverse biased diode is easily measurable than that of forward biased. That is why photodiode is operated at reverse bias.

2 Marks Questions

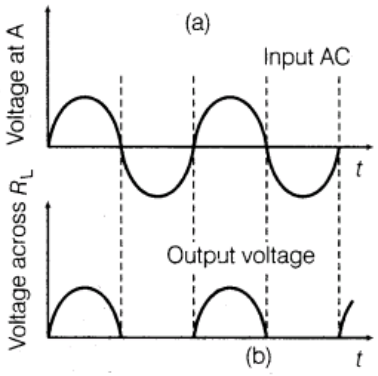
10.Explain, with the help of a circuit diagram, the working of a p-n junction diode as a half-wave rectifier. [ah India 2014]

Ans.p-n Junction Diode as a Half-Wave Rectifier AC voltage to be rectified is connected to the primary coil of a step-down transformer. Secondary coil is connected to the diode through resistors Rj,, across which output is obtained.



Working During positive half cycle of the input AC, the p-n junction is forward biased. Thus, the resistance in p-n junction becomes low and current flows. Hence, we get output in the load.

During negative half cycle of the input AC, the p-n junction is reverse biased. Thus, the resistance of p-n junction is high and current does not flow. Hence, no output in the load. So, for complete cycle of AC, current flows through the load resistance in the same direction.

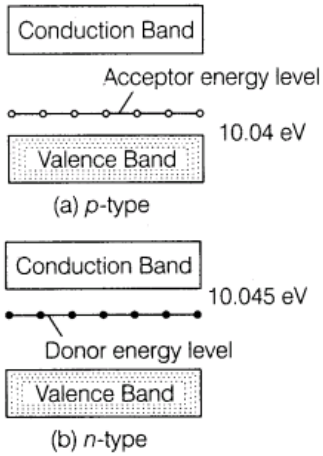


Input and output waveforms

11.Draw energy band diagram of n-type and p-type semiconductor at temperature T > OK. Mark the donar and acceptor energy level with their energies. [Foreign 2014]

Ans.

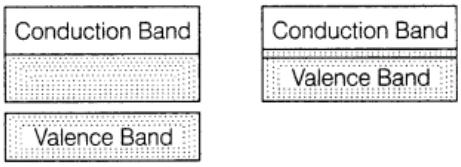
The required energy band diagram is shown below:



12.Distinguish between a metal and an insulator on the basis of energy band diagram.

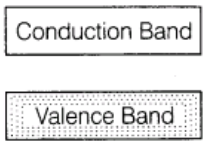
[Foreign 2014]

Ans.(i) **Metal** For metals, the valence band is completely filled and the conduction band can have two possibilities either it is partially filled with an extremely small energy gap between the valence and conduction bands or it is empty, with two bands overlapping each other as shown below:



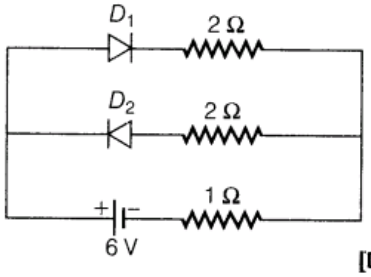
(ii) On applying an small even electric field, metals can conduct electricity.

(i) **Insulators :** for insulator, the energy gap between the conduction and valence bands are very large, also the conduction band is practically empty, as shown below:



(ii) When an electric field is applied across such a solid, the electrons find it difficult to acquire. So, a large amount of energy is required to reach the conduction band.Thus, the conduction band continues to be empty. That is why no current flows through insulators.

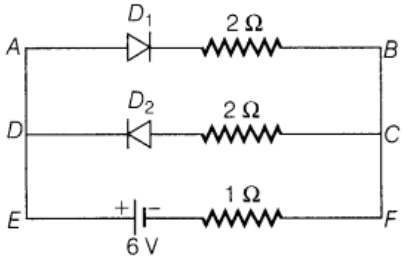
13. Assuming that the two diodes D_1 and D_2 used in the electric circuit shown in the figure are ideal, find out the value of the current flowing through 1 Ω resistor.



[Delhi 2013C]

Ans.

According to the question



$$R_{AB} = 2 + 1 = 3\ \Omega$$

$$\frac{1}{R'} = \frac{1}{2} + \frac{1}{3} = \frac{3+2}{6} = \frac{5}{6}\Omega^{-1};\ R' = \frac{6}{5}\Omega$$

$$I_{EF} = \frac{V}{R'} = \frac{6}{6/5} = 5\text{A}$$

(2)

14.Explain the term 'drift velocity' of electrons in conductor. Hence, obtain an expression for the current through a conductor in terms of 'drift velocity'.[All India 2013]

Ans.'Drift velocity' of electrons in a conductor

Metals contain a large number of free electrons. These electrons are in continuous random

motion. Due to the random motion, the free electrons collide with positive metal ions with high frequency and undergo change in direction at each collision. So, the average velocity for the electrons in a conductor is zero.Now, when this conductor is connected to a source of emf, an electric field is established in the conductor, such that E = V/L
where, V = potential difference across the conductor and L = length of the conductor. The electric field exerts an electrostatic force -Ee on each free electron in the conductor. The acceleration of each electron is given by

$$\mathbf{a} = -\frac{e\mathbf{E}}{m}$$

where, e = electric charge on electron and m = mass of electron.
The average velocity of all the free electrons in the conductor is called the drift velocity of free electrons of the conductor.

$$v_d = -\frac{e\mathbf{E}}{m}\tau \qquad \ldots(\text{i})$$

where, τ = relaxation time between two successive collisions.

Thus, the expression for the drift velocity is electric field.

$$E = -\frac{V}{L} \qquad \ldots(\text{ii})$$

Let n = number density of electrons in the conductor.

Number of free electrons in the conductor = nAL

Total charge on the conductor, $q = nALe$

Time taken by this charge to cover the length L of the conductor, $t = L / v_d$

Current, $I = \frac{q}{t} = \frac{nALe}{L} \times v_d$

Using Eqs. (i) and (ii), we get that

$$I = nAe \times \left(-\frac{e\mathbf{E}}{m}\tau\right) = nAe \times \left(-\frac{e(-V)}{mL}\tau\right)$$

$$I = \left(\frac{ne^2A}{mL}\tau\right)V \qquad \textbf{(1)}$$

15.Mention the important considerations required while fabricating a p-n junction diode to be used as a Light Emitting Diode (LED). What should be the order of band gap of an LED, if it is required to emit light in the visible range? [Delhi 2013]
Ans.

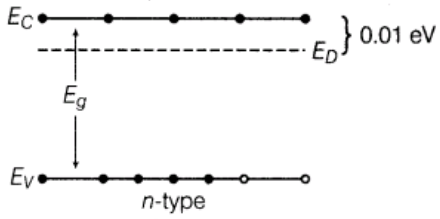
For LEDs, the threshold voltages are much higher and slightly different for different colours. The reverse breakdown voltages of LEDs are low generally around 5V. It is due to this reason, the care is taken that high reverse voltages do not appear across LEDs. There is very little resistance to limit the current in LED. Therefore, a resistor must be used in series with the LED to avoid any damage to it. **(1)**

The semiconductor used for fabrication of visible LEDs must at least have a band gap of 1.8eV (spectral range of visible light is from about 0.4 μm to 0.7 μm i.e. from about 3 eV to 1.8 eV). **(1)**

16.Write two characteristics features to distinguish between n-type and p-type semiconductors. [All India 2012]

Ans.

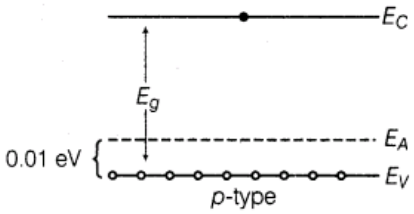
(i) In *n*-type semiconductor, the semiconductor is doped with pentavalent impurity. In it the electrons are majority carriers and holes are minority carriers or $n_e >> n_h$ (n_e= number density of electrons, n_h= number density of holes). In energy band diagram of *n*-type semiconductor, the donor energy level E_D is slightly below the bottom of E_C conduction band and thus, the electron can move to conduction band, even with small supply of energy.



(1)

(*ii*) In *p*-type semiconductor, the semiconductor is doped with trivalent impurity. In this semiconductor, the holes are the majority carriers and electrons are the minority carriers i.e. $n_h >> n_e$.

In energy-band diagram of *p*-type, the acceptor energy level is slightly above the top of valence band E_V. Thus, even with small supply of energy electron from valence band can jump to level, E_A and ionize the acceptor, negatively.



17.Give two advantages of LED's over the conventional incandescent lamps.[Foreign 2012]

Ans. When we apply sufficient voltage to LED, electron move across the junction into p-region and get attracted to the holes there. Thus, electrons and holes recombine. During each recombination, the electric potential energy is converted into the electromagnetic energy and a photon of light with a characteristic frequency is emitted, this is how, LED works.
Advantages of LEDs over incandescent lamps
(i) Since, LEDs do not have a filament that can burn out, hence, they last longer.
They do not get hot during use.

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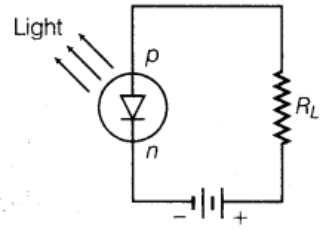


(1)

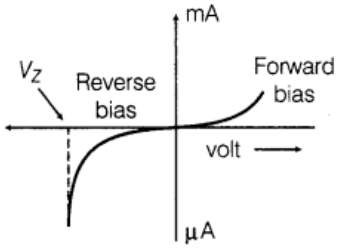
18. The current in the forward bias is known to be more (~ mA) than the current in the reverse bias (~μA). What is the reason, to operate the photodiode in reverse bias? **[Delhi 2012]**

Ans.When photo diode is illuminated with light due to breaking of covalent bonds, equal number of additional electrons and holes comes into existence whereas fractional change in minority charge carrier is much higher than fractional change in majority charge carrier. Since, the fractional change of minority carrier current is measurable significantly in reverse bias than that of forward bias. Therefore, photo diode are connected in reverse bias.

19.Name the semiconductor device that can be used to regulate an unregulated DC power supply. With the help of 7-V characteristics of this device, explain its working principle. [Delhi 2011]

Ans. Zener diode is used as voltage regulator.

Principle Zener diode is operated in the reverse breakdown region. The voltage across it remains constant, equal to the breakdown voltage for large charge in reverse current



Characteristic of a Zener diode

20.How is forward biasing different from reverse biasing in a p-n junction diode? [Delhi 2011]

Ans.Differences between forward and reverse biases are given below:

Forward bias	Reverse bias
Positive terminal of battery is connected to *p*-type and negative terminal to *n*-type semiconductor.	Positive terminal of battery connected to *n*-type and negative terminal to *p*-type semiconductor.
Depletion layer is very thin.	Depletion layer is thick.
p-n junction offers very low resistance.	*p-n* junction offers very high resistance.
An ideal diode have zero resistance.	An ideal diode have infinite resistance.

21.Explain, how a depletion region is formed in a junction diode?[Delhi 2011]

Ans. With the formation of p-n junction, the holes from p-region diffuse into the n-region and electrons from n-region diffuse into p-region and electron-hole pair combine and get annihilated.

This input produces potential barrier, V_B across in junction which opposes the further diffusion through the junction. Thus, small region forms in the vicinity of the junction which is depleted of free charge carrier and has only immotile ions is called the depletion region.

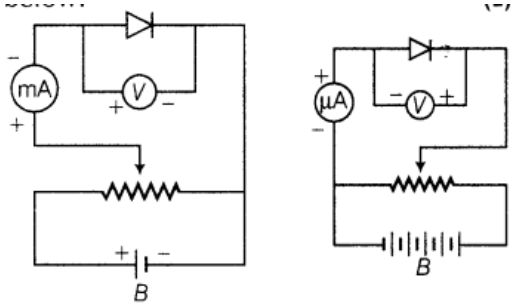
22.Draw the circuit diagram showing how a p-n junction diode is

(i)forward biased

(ii)reverse biased.

How is the width of depletion layer affected in the two cases?[All India 2011 C]

Ans.Circuit diagram of forward biased and reverse biased p-n junction diode is shown



The width of depletion layer (i) decreases in forward bias.

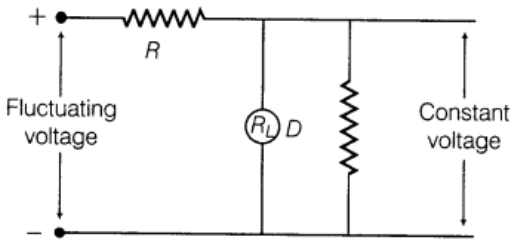
(ii) increases in reverse bias.

23.Carbon and silicon both have four valence electrons each, then how are they distinguished? [Delhi 2011 c]

Ans.The four valence electrons of carbon are present in second orbit while that of silicon in third orbit. So, energy required to extricate an electron from silicon is much smaller than carbon.

Therefore, the number of free electrons for conduction in silicon is significant on contrary of carbon. This makes silicon conductivity much higher than carbon. This is the main distinguishable property.

24. Name the device, D which is used as a voltage regulator in the given circuit and give its symbol.



[Delhi 2011C]

Ans.

Device, D is a Zener diode.

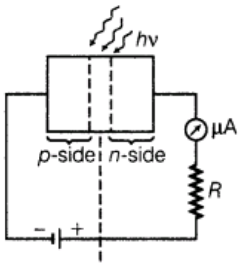
Symbol of Zener diode

25.Draw the circuit diagram of an illuminated photo diode in reverse bias. How is photo diode used to measure light intensity? [Delhi 2010]26.Write the main use of the

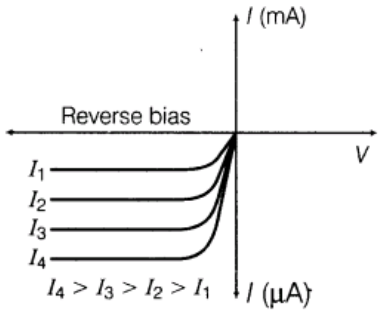
(i)photo diode

(ii)Zener diode. [All India 2010 c]

Ans. Circuit diagram of illuminated photo diode in reverse bias is shown below:



A reverse biased photodiode



Reverse bias currents through a photodiode

Hence, frequency of light ν such that $h\nu > E_g$, where E_g is band gap of increasing intensity I_1, I_2, I_3, etc. The value of reverse saturation current increases with the increase of intensity of light.

Thus, the measurement of charge in the reverse saturation current can give the intensity of incident light. **(1)**

26.Write the main use of the (i) photo diode (ii) Zener diode [All India 2010 c]

Ans.**Main use of photo diode** In demodulation of optical signal and detection of optical signal.

Main use of Zener diode As DC voltage regulator.

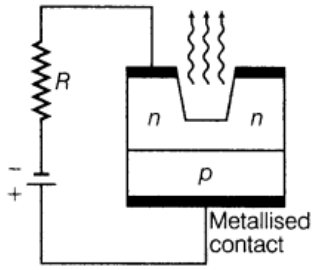
27. Distinguish between an intrinsic semiconductor and *p*-type semiconductor. Give reason, why a *p*-type semiconductor crystal is electrically neutral, although $n_h >> n_e$? **[Delhi 2008C]**

Ans.Differences between intrinsic and p-type semiconductors are given below:

Intrinsic semiconductor	*p*-type semiconductor
Pure semiconductor of tetravalent crystal.	Impure semiconductor of tetravalent crystal doped with trivalent impurity.
$n_e = n_h$	$n_e < n_h$
Conductivity depends on temperature.	Conductivity depends on temperature as well as dopant concentration.

In p-type semiconductor, trivalent impurity is doped with tetravalent pure semiconductor. Both type of atom (impurity and host semiconductor) are electrically neutral and hence, so produced p-type semiconductor is electrically neutral

28.Draw a circuit diagram showing the biasing of an LED. State the factor which controls (i)wavelength of light.
(ii) intensity of light emitted by the diode. [Foreign 2008]
Ans. Circuit diagram of a forward biased LED is shown below:



A forward biased LED **(1)**

(*i*) Wavelength of light is controlled by band gap (E_g) of semiconductor material.

(*ii*) Intensity of light emitted by the diode depends on concentration of impurity in junction diode. **(1)**

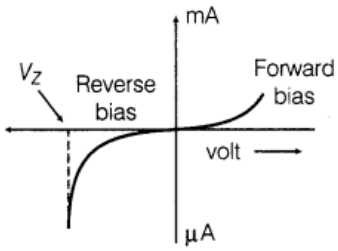
29.How is that the reverse current in a Zener diode starts increasing suddenly at a relatively low breakdowns voltage of 5 V or so?[All India 2008 C]
Ans.

In Zener diode, the depletion layer width is very small ($< 10^{-7}$ m) and hence even a very small breakdown voltage of 5 V, set up a high electric field 5×10^7 V/m which facilitating of breaking of covalent band and liberation of electrons drifted towards *n*-type semiconductor. It produces large reverse current. **(2)**

30.Draw the (i) symbol and (ii) the reverse I-V characteristics of a Zener diode. Explain briefly, which property of the characteristics enables us to use Zener diode as voltage regulator. [All India 2008 C]

Ans. Zener diode is used as voltage regulator.

Principle Zener diode is operated in the reverse breakdown region. The voltage across it remains constant, equal to the breakdown voltage for large charge in reverse current



Characteristic of a Zener diode

Device, *D* is a Zener diode.

Symbol of Zener diode

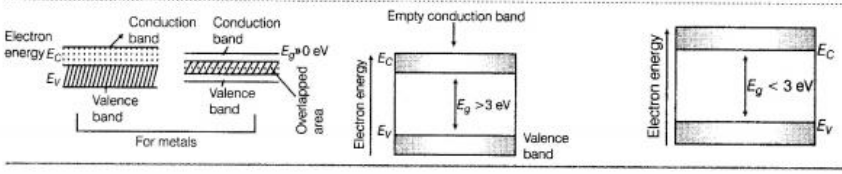
3 Marks Questions

31.Write any two distinguishing features between conductors, semiconductors and insulators on the basis of energy band diagrams. [All India 2014]32.Draw the circuit diagram of a full-wave rectifier using p-n junction diode. Explain its working and show the output input waveforms. [Delhi 2012]

Ans.

Differences between conductor, insulator and semiconductor on the basis of energy bands are given below:

Conductor (Metal)	**Insulator**	**Semiconductor**
In conductor, either there is no energy gap between the conduction band which is partially filled with electrons and valence band or the conduction band and valence band overlap each other.	In insulator, the valence band is completely filled, the conduction band is completely empty and energy gap is quite large that small energy from any other source cannot overcome it.	In semiconductor also, like insulators the valence band is totally filled and the conduction band is empty but the energy gap between conduction band and valence band, unlike insulators is very small.
Thus, many electrons from below the fermi level can shift to higher energy levels above the fermi level in the conduction band and behave as free electrons by acquiring a little more energy from any other sources.	Thus, electrons are bound to valence band and are not free to move and hence, electric conduction is not possible in this type of material.	Thus, at room temperature, some electrons in the valence band acquire thermal energy greater than energy band gap and jump over to the conduction band where they are free to move under the influence of even a small electric field and acquire small conductivity.

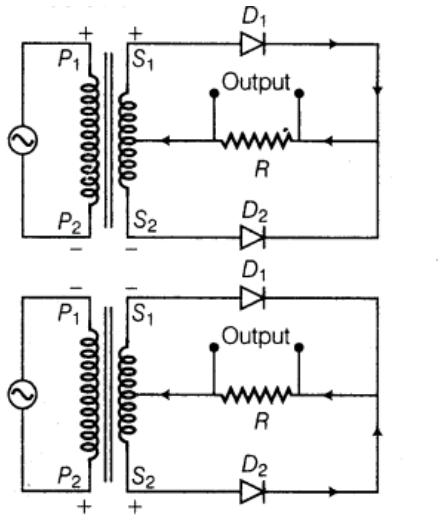


32.Draw the circuit diagram of a full-wave rectifier using p-n junction diode. Explain its working and show the output input wave forms. [Delhi 2012]

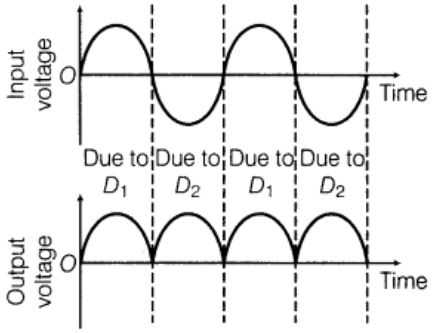
Ans.

In these type of questions, we have to mind that in full-wave rectifier, full cycle of the input will be used.

The circuit diagram of full-wave rectifier is shown below:



The input and output waveforms have been given below:



(2)

Its working based on the principle that junction diode offer very low resistance in forward bias and very high resistance in reverse bias. **(1)**

33.Draw V-I characteristics of a p-n junction diode. Answer the following questions, giving reasons.

(i)Why is the current under reverse bias almost independent of the applied potential up to a critical voltage?

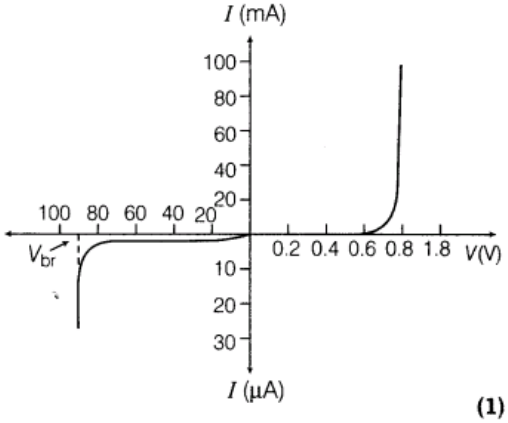
(ii)Why does the reverse current show a sudden increase at the critical voltage?

Name any semiconductor device which operates under the reverse bias in the breakdown region.

[All India 2012]

Ans.

V-I characteristic of *p-n* junction diode



(1)

(i)Under the reverse bias condition, the holes of p-side are attracted towards the negative terminal of the battery and the electrons of the n-side are attracted towards the positive

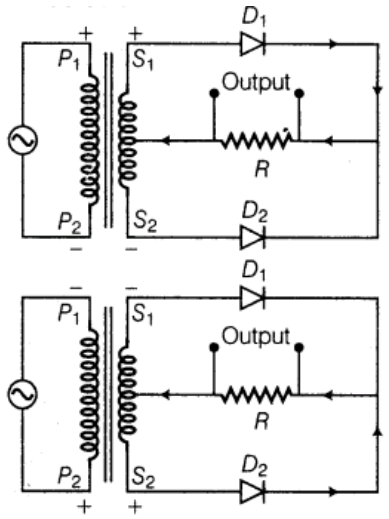
terminal of the battery. This increases the depletion layer and the potential barrier. However, the minority charge carriers are drifted across the junction producing a small current.
At any temperature, the number of minority carriers is constant, so there is the small current at any applied potential. This is the reason for the current under reverse bias to be almost'independent of applied potential. At the critical voltage, avalanche breakdown takes place which results in a sudden flow of large current.
(ii) At the critical voltage, the holes in the n-side and conduction electrons in the p-side are accelerated due to the reverse bias voltage. These minority carriers acquire sufficient kinetic energy from the electric field and collide with a valence electron.
Thus, the bond is finally broken and the valence electrons move into the conduction band resulting in enormous flow of electrons and thus, formation of hole-electron pairs. Thus, there is a sudden increase in the current at the critical voltage.
Zener diode is a semiconductor device which operates under the reverse bias in the breakdown region.

34.Draw a labelled diagram of a full -wave rectifier circuit. State its working principle. Show the input-output wave forms.[All India 2011]

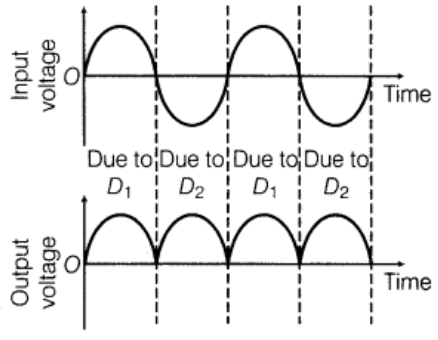
Ans.

In these type of questions, we have to mind that in full-wave rectifier, full cycle of the input will be used.

The circuit diagram of full-wave rectifier is shown below:



The input and output waveforms have been given below:

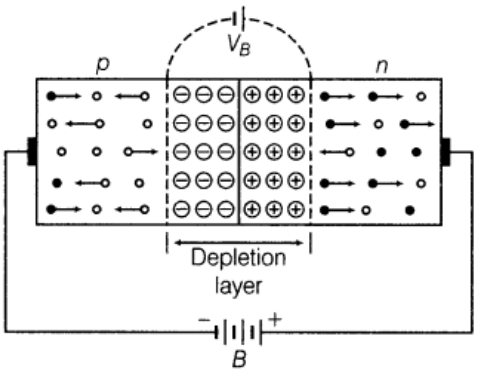


(2)

Its working based on the principle that junction diode offer very low resistance in forward bias and very high resistance in reverse bias. **(1)**

35.Name the important processes that occurs during the formation of a p-n junction.Explain briefly, with the help of asuitable diagram, how a p-n junction is formed.Define the term 'barrier potential'?[Foreign 2011]

Ans.



During formation of p-n junction, diffusion of charge takes place. As, soon as p-type semiconductor is joined with n-type semiconductor, diffusion of free charges across the junction starts.

For explanation of formation p-n junction

With the formation of p-n junction, the holes from p-region diffuse into the n-region and electrons from n-region diffuse into p-region and electron-hole pair combine and get annihilated.

This input produces potential barrier, V_B across in junction which opposes the further diffusion through the junction. Thus, small region forms in the vicinity of the junction which is depleted of free charge carrier and has only immotile ions is called the depletion region.

Potential barrier The potential distribution near the p-n junction is known as potential barrier

36.(i) Why is a photo diode operated in reverse bias mode?

(ii)For what purpose is a photo diode used?

(iii)Draw its I-V characteristics for different intensities of illumination. [HOTS; All India 2011 C]

Ans.

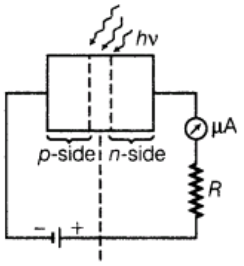
In these type of questions, we should mind that the diode is connecte reverse biased or forward biased.

(i) Photo diode is connected in reverse bias and feeble reverse current flows due to thermally generated electron-hole pair, known as dark current. When light of

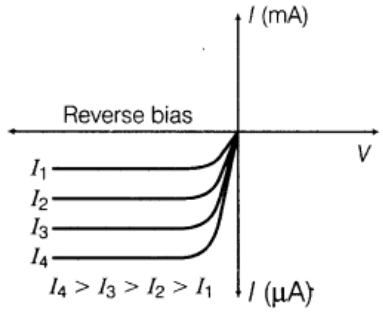
suitable frequency (v) such that $h\nu > E_g$, where E_g is band gap is incident on diode, additional electron-hole pair generated and current grows in the circuit.(1)

(ii)**Main use of photo diode** In demodulation of optical signal and detection of optical signal.

(iii)Circuit diagram of illuminated photo diode in reverse bias is shown below:



A reverse biased photodiode



Reverse bias currents through a photodiode

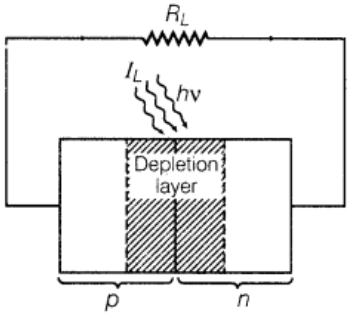
Hence, frequency of light ν such that $h\nu > E_g$, where E_g is band gap of increasing intensity I_1, I_2, I_3, etc. The value of reverse saturation current increases with the increase of intensity of light.

Thus, the measurement of charge in the reverse saturation current can give the intensity of incident light. **(1)**

37.(i)Why are Si and GaAs preferred materials for solar cells?
(ii)Describe briefly with the help of a necessary circuit diagram, the working principle of a solar cell.[All India 2011 C]

Ans. (i) solar radiation is nearly 1.5 eV. In order to have photo excitation, the energy of radiation (hv) must be greater than energy band gap (E_g). Therefore, the semiconductor with energy band gap about 1.5 eV or lower than it and with higher absorption coefficient is likely to give better solar conversion efficiency. The energy band gap for Si is about 1.1 eV, while for GaAs, it is about 1.53 eV. The GaAs is better inspite of its higher band gap than Si because it absorbs relatively more energy from the incident solar radiations being of relatively higher absorption coefficient.

(*ii*) When light of frequency, ν such that $h\nu > E_g$ (band gap) is incident on junction, then electron-hole pair liberated in the depletion region drifts under the influence of potential barrier. The gathering of these charge carriers make *p*-type as positive electrode and *n*-type as negative electrode and hence, generating photo-voltage across solar cell.



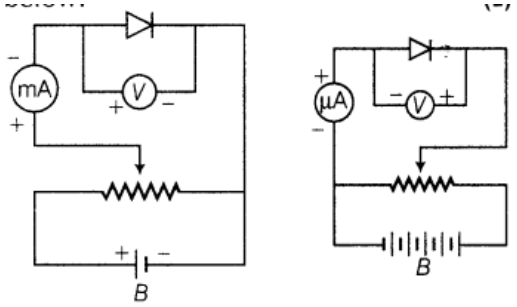
38.(i) Describe the working of Light Emitting Diodes (LEDs).
(ii)Which semiconductors are preferred to make LEDs and why?
(iii)Give two advantages of using LEDs over conventional incandescent low power lamps.
[All India 2011]

Ans.(i) Working of LED LED is a forward biased p-n junction which converts electrical energy into optical energy of infrared and visible light region.

Being in forward bias, thin depletion layer and low potential barrier facilitate diffusion of

electron and hole through the junction when high energy electron of conduction band combines with the low energy holes in valence band, then energy is released in the form of photon, may be seen in the form of light.
(ii) Semiconductors with appropriate band gap (E_g) close to 1.5 eV are preferred to make LED size GaAs, CdTe, etc.the other reasons to select these materials e high optical absorption, availability of raw material and low cost
(iii) Uses of LEDs (a) LED can operate at very low voltage and consumes less power in comparison to incandescent lamps
(b) Unlike the lamps, they take very less operational time and have long life.

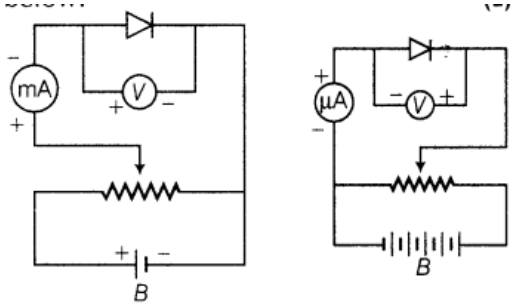
39.With the help of a suitable diagram, explain the formation of depletion region in a p-n junction. How does its width change when the junction is
(i)forward biased and
(ii)reverse biased? [All India 2009]
Ans. With the formation of p-n junction, the holes from p-region diffuse into the n-region and electrons from n-region diffuse into p-region and electron-hole pair combine and get annihilated.
This input produces potential barrier, V_B across in junction which opposes the further diffusion through the junction. Thus, small region forms in the vicinity of the junction which is depleted of free charge carrier and has only immotile ions is called the depletion region.
Circuit diagram of forward biased and reverse biased p-n junction diode is shown



The width of depletion layer (i) decreases in forward bias.
(ii) increases in reverse bias.

40.(i) With the help of circuit diagrams, distinguish between forward biasing and reverse biasing of p-n junction diode.
(ii)Draw V-I characteristics of a p-n junction diode in
(a)forward bias.
(b)reverse bias. [AH India 2009]

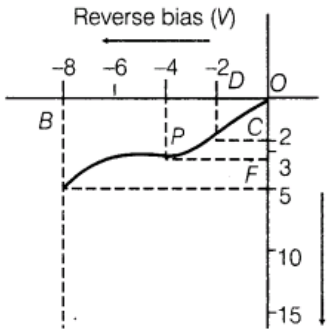
Ans.(i)Circuit diagram of forward biased and reverse biased p-n junction diode is shown



The width of depletion layer (a) decreases in forward bias.
(b) increases in reverse bias.
(ii)(a)Differences between forward and reverse biases are given below:

Forward bias	Reverse bias
Positive terminal of battery is connected to *p*-type and negative terminal to *n*-type semiconductor.	Positive terminal of battery connected to *n*-type and negative terminal to *p*-type semiconductor.
Depletion layer is very thin.	Depletion layer is thick.
p-n junction offers very low resistance.	*p-n* junction offers very high resistance.
An ideal diode have zero resistance.	An ideal diode have infinite resistance.

(*b*)



Reverse bias characteristic curve **(1)**

At the critical voltage, the holes in the n-side and conduction electrons in the p-side are accelerated due to the reverse bias voltage. These minority carriers acquire sufficient kinetic energy from the electric field and collide with a valence electron.

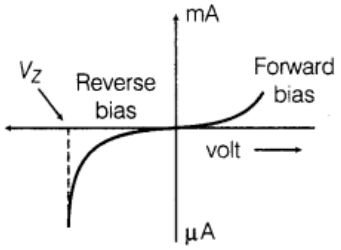
Thus, the bond is finally broken and the valence electrons move into the conduction band resulting in enormous flow of electrons and thus, formation of hole-electron pairs. Thus, there is a sudden increase in the current at the critical voltage.

Zener diode is a semiconductor device which operates under the reverse bias in the breakdown region.

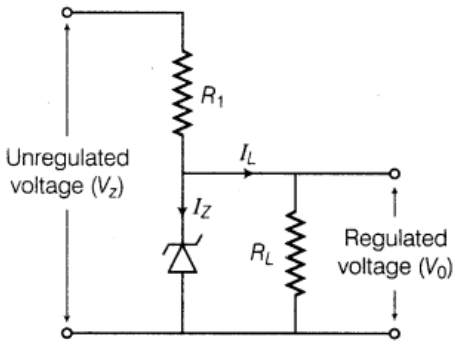
41.Explain with the help of a circuit diagram how a Zener diode works as a DC voltage regulator? Draw its I-V characteristic s.[All India 2009]

Ans. Zener diode is used as voltage regulator.

Principle Zener diode is operated in the reverse breakdown region. The voltage across it remains constant, equal to the breakdown voltage for large charge in reverse current



Characteristic of a Zener diode



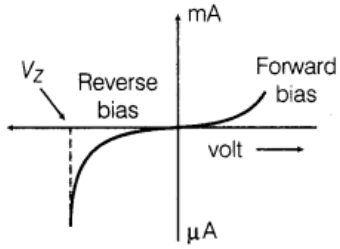
(1)

42.How is a Zener diode fabricated so as to make it a special purpose semiconductor diode? Draw the circuit diagram of a Zener diode as a voltage regulator and explain its working. [All India 2009 C]

Ans.Zener diode fabrication Zener diode is made by heavily doping of both p and n-type semiconductors and hence, the width of depletion layer becomes thin which lead to produce large electric field to increase the current even on applying reverse voltage of 4 or 5 V.

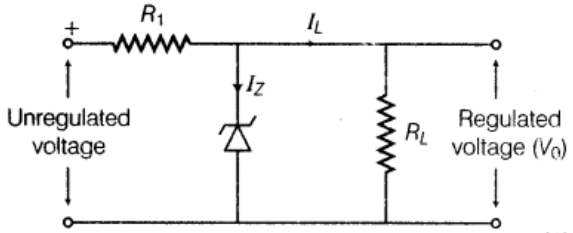
(i)Zener diode is used as voltage regulator.

Principle Zener diode is operated in the reverse breakdown region. The voltage across it remains constant, equal to the breakdown voltage for large charge in reverse current



Characteristic of a Zener diode

(ii) From the figure, it is clear that the device, X is a full-wave rectifier. Circuit diagram as shown in figure below:



(1)

Zener diode connected with unregulated DC voltage in reverse bias. When the input voltage increases, then current through R, increase and hence, voltage drop across R_p increases while voltage across the Zener diode remains constant. The voltage across Zener diode remains constant beyond Zener voltage and hence, same/constant regulated voltage is obtained across R_L.

(*iii*) In *n*-type semiconductor,

$$n_e > n_h \qquad \ldots(i)$$

On incidence of light of suitable frequency, there is equal rise in number of electrons and holes [i.e. Δn (say)]

$$\Rightarrow \quad \frac{1}{n_e} < \frac{1}{n_h} \text{ or } \frac{\Delta n}{n_e} < \frac{\Delta n}{n_h}$$

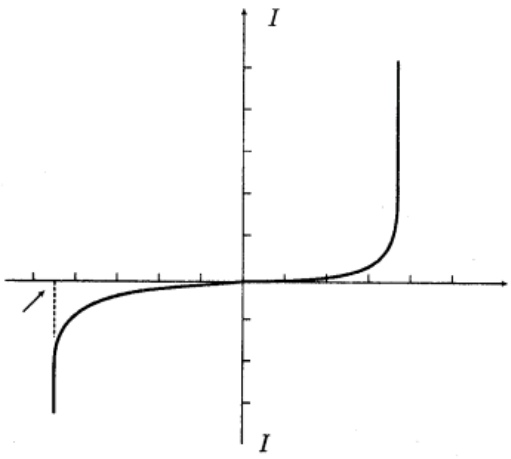
where, Δn = change in electron or hole charge carrier.

Thus, fractional change in minority charge carrier (hole) is much higher than fraction change in majority charge carrier (electron). Also, minority charge carrier contribute in drift current in reverse bias.

Thus, with incidence of light, fractional change in minority charge carrier is significant.

Therefore, photo diode should be connected in reverse bias for measuring light intensity.

43.The figure below, shows the V-I characteristics of a semiconductor diode.



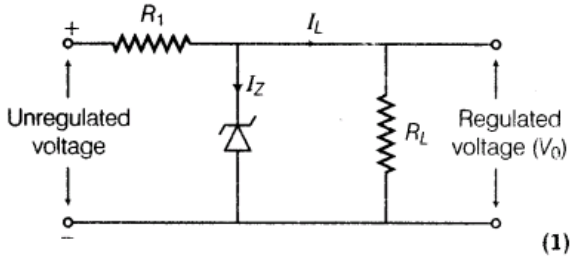
(i)Identify the semiconductor diode used.

(ii) Draw the circuit diagram to obtain the given characteristic of this device.

(iii) Briefly explain, how this diode can be used as a voltage regulator.[Delhi 2008]

Ans.(i) Zener diode

(ii) From the figure, it is clear that the device, X is a full-wave rectifier. Circuit diagram as shown in figure below:

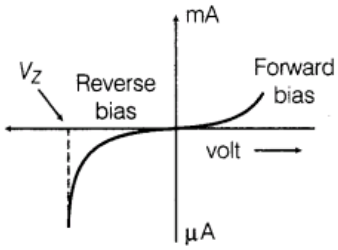


(1)

Zener diode connected with unregulated DC voltage in reverse bias. When the input voltage increases, then current through R, increase and hence, voltage drop across R_p increases while voltage across the Zener diode remains constant. The voltage across Zener diode remains constant beyond Zener voltage and hence, same/constant regulated voltage is obtained across R_L.

(iii) Zener diode is used as voltage regulator.

Principle Zener diode is operated in the reverse breakdown region. The voltage across it remains constant, equal to the breakdown voltage for large charge in reverse current



Characteristic of a Zener diode

5Marks Questions

44.(i)State briefly the processes involved in the formation of p-n junction, explaining clearly how the

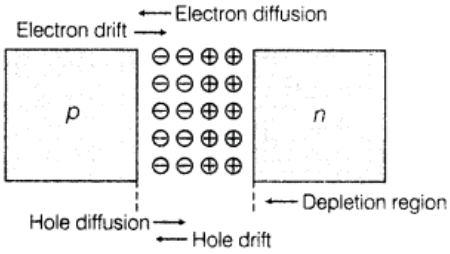
depletion region is formed.

(ii)Using the necessary circuit diagrams, show how the V-I characteristics of a p-n junction are obtained in (a) forward biasing (b) reverse biasing How are these characteristics made use of in rectification? [Delhi 2014]

Ans.(i) **p-n Junction** A p-n junction is an arrangement made by a close contact of n-type semiconductor and p-type semiconductor.There are various methods of forming p-n junction diode. In one method, an n-type germanium crystal is cut into thin slices called wafers. An aluminium film is laid on an n-type wafer which is then heated in an oven at a temperature of

about 600°C. Aluminium then diffuses into the surface of wafer. In this way, a p-type semiconductor is formed on n-type semiconductor.

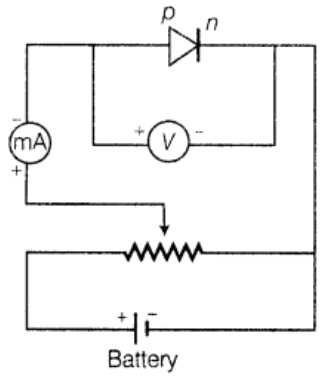
Formation of Depletion Region in p-n Junction In an n-type semiconductor, the concentration of electrons is more than concentration of holes. Similarly, in a p-type semiconductor, the concentration of holes is more than that of concentration of electrons. During formation of p-n junction and due to the concentration gradient across p and n-sides, holes diffuse from p-side to n-side (p—> n) and electrons diffuse from n-side to p-side (n —> p).



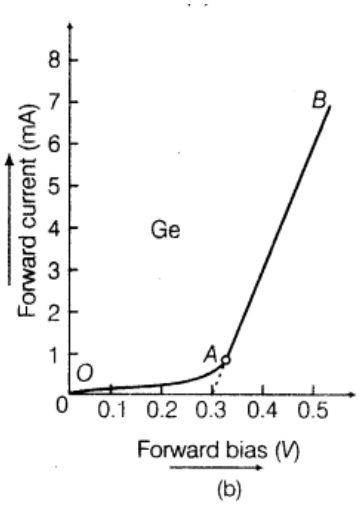
The diffused charge carriers combine with their counterparts in the immediate vicinity of the junction and neutralise each other, (l) Thus, near the junction, positive charge is built on n-side and negative charge on p-side This sets up potential difference across the junction and an internal electric field Ej directed from n-side to p-side. The equilibrium is established when the field £, becomes strong enough to stop further diffusion of the majority charge carriers (however, it helps the minority charge carriers to diffuse across the junction).The region on either side of the junction which becomes depleted (free) from the mobile charge carriers is called depletion region or **depletion layer**. The width of depletion region is of the order of 10^{-6} m.The potential difference developed across the depletion region is called the potential barrier. Potential barrier depends on dopant concentration in the semiconductor and temperature of the junction.

(ii) (a) **Forward Biased Characteristics**

The circuit diagram for studying forward biased characteristics is shown in the figure. Starting from a low value, forward bias voltage is increased step by step (measured by voltmeter) and forward current is noted (by ammeter). A graph is plotted between voltage and current. The curve so obtained is the forward characteristic of the diode.



(a)

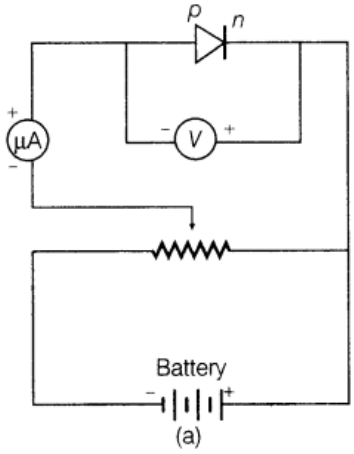


(b)

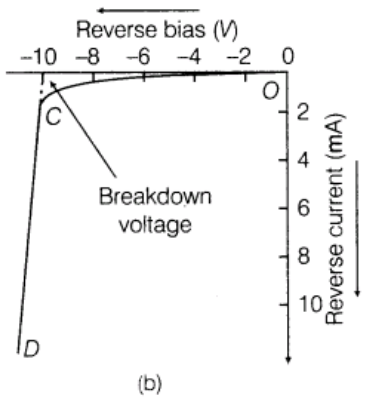
At the start when applied voltage is low, the current through the diode is almost zero. It is because of the potential barrier, which opposes the applied voltage. Till the applied voltage exceeds the potential barrier, the current increases very slowly with increase in applied voltage (OA portion of the graph).With further increase in applied voltage, the current increases very rapidly (AB portion of the graph), in this situation, the diode behaves like a conductor. The forward voltage beyond which the current through the junction starts increasing rapidly with voltage is called knee voltage. If line AB is extended back, it cuts the voltage axis at potential barrier voltage.

(b) **Reverse Biased Characteristics**

The circuit diagram for studying reverse biased characteristics is shown in the figure.



(a)



(b)

In reverse biased, the applied voltage supports the flow of minority charge carriers across the junction. So, a very small current flows across the junction due to minority charge carriers. Motion of minority charge carriers is also supported by internal potential barrier, so all the minority carriers cross over the junction.Therefore, the small reverse current remains almost constant over a sufficiently long range of reverse bias, increasing very little with increasing voltage (OC portion of the graph). This reverse current is voltage independent upto certain voltage known as **breakdown voltage** and this voltage independent current – is called reverse

saturation current.

Use of p-n Junction Characteristics in Rectification

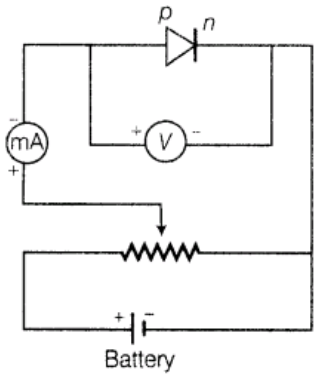
From forward and reverse characteristics, it is clear that current flows through the junction diode only in forward bias not in reverse bias i.e. current flows only in one direction

45.(a) Draw the circuit arrangement for studying the V-I characteristics of a p-n junction diode in (i) forward and (ii) reverse bias. Briefly explain how the typical V- I characteristics of a diode are obtained and draw these characteristics.

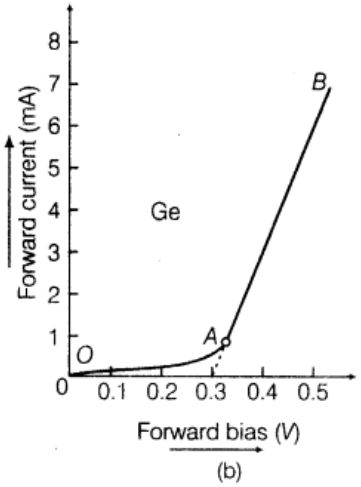
(b)With the help of necessary circuit diagram, explain the working of a photo diode used for detecting optical signals. [All India 2014 C]

Ans. (a) **Forward Biased Characteristics**

The circuit diagram for studying forward biased characteristics is shown in the figure. Starting from a low value, forward bias voltage is increased step by step (measured by voltmeter) and forward current is noted (by ammeter). A graph is plotted between voltage and current. The curve so obtained is the forward characteristic of the diode.



(a)

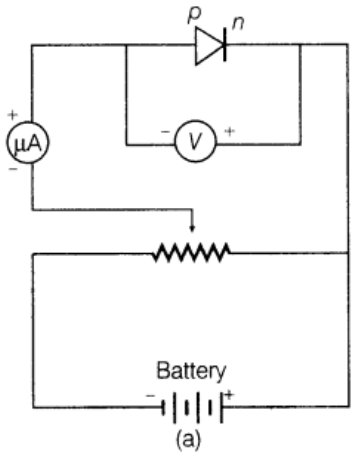


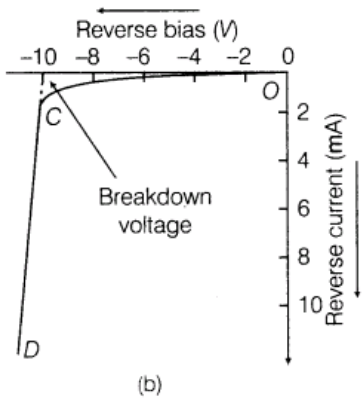
(b)

At the start when applied voltage is low, the current through the diode is almost zero. It is because of the potential barrier, which opposes the applied voltage. Till the applied voltage exceeds the potential barrier, the current increases very slowly with increase in applied voltage (OA portion of the graph).With further increase in applied voltage, the current increases very rapidly (AB portion of the graph), in this situation, the diode behaves like a conductor. The forward voltage beyond which the current through the junction starts increasing rapidly with voltage is called knee voltage. If line AB is extended back, it cuts the voltage axis at potential barrier voltage.

(b) **Reverse Biased Characteristics**

The circuit diagram for studying reverse biased characteristics is shown in the figure.



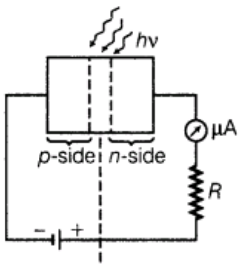


In reverse biased, the applied voltage supports the flow of minority charge carriers across the junction. So, a very small current flows across the junction due to minority charge carriers. Motion of minority charge carriers is also supported by internal potential barrier, so all the minority carriers cross over the junction.Therefore, the small reverse current remains almost constant over a sufficiently long range of reverse bias, increasing very little with increasing voltage (OC portion of the graph). This reverse current is voltage independent upto certain voltage known as **breakdown voltage** and this voltage independent current – is called reverse saturation current.

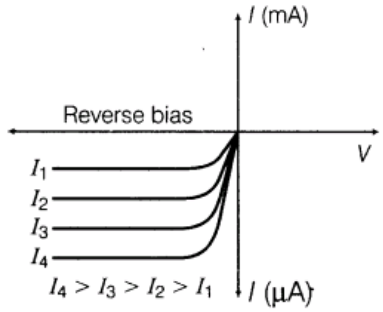
Use of p-n Junction Characteristics in Rectification

From forward and reverse characteristics, it is clear that current flows through the junction diode only in forward bias not in reverse bias i.e. current flows only in one direction

(b)Circuit diagram of illuminated photo diode in reverse bias is shown below:



A reverse biased photodiode



Reverse bias currents through a photodiode

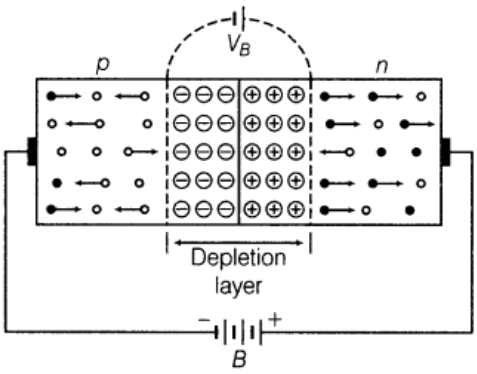
Hence, frequency of light ν such that $h\nu > E_g$, where E_g is band gap of increasing intensity I_1, I_2, I_3, etc. The value of reverse saturation current increases with the increase of intensity of light.

Thus, the measurement of charge in the reverse saturation current can give the intensity of incident light. **(1)**

46.(a) Explain with the help of diagram, how a depletion layer and barrier potential are formed in a junction diode.

(b) Draw a circuit diagram of a full-wave rectifier. Explain its working and draw input and output waveforms. [Delhi 2014 c]

Ans.(a)



During formation of p-n junction, diffusion of charge takes place. As, soon as p-type semiconductor is joined with n-type semiconductor, diffusion of free charges across the junction starts.

For explanation of formation p-n junction

With the formation of p-n junction, the holes from p-region diffuse into the n-region and electrons from n-region diffuse into p-region and electron-hole pair combine and get annihilated.

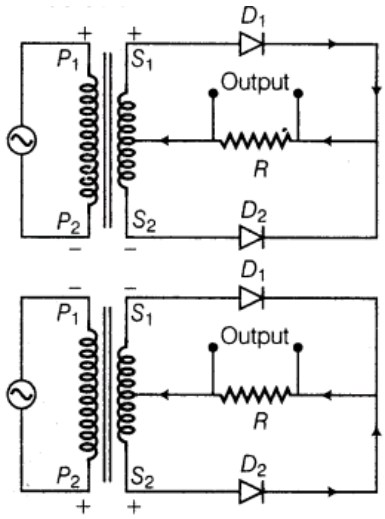
This input produces potential barrier, V_B across in junction which opposes the further diffusion through the junction. Thus, small region forms in the vicinity of the junction which is depleted of free charge carrier and has only immotile ions is called the depletion region.

Potential barrier The potential distribution near the p-n junction is known as potential barrier

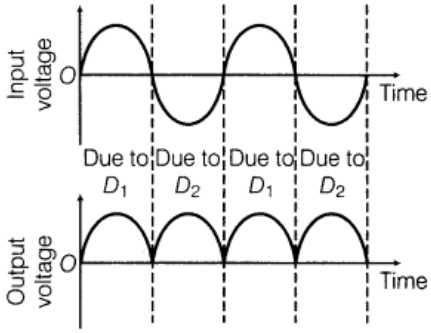
(b)

In these type of questions, we have to mind that in full-wave rectifier, full cycle of the input will be used.

The circuit diagram of full-wave rectifier is shown below:



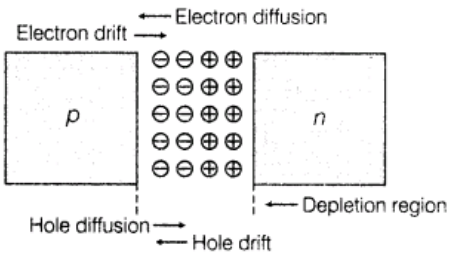
The input and output waveforms have been given below:



(2)

Its working based on the principle that junction diode offer very low resistance in forward bias and very high resistance in reverse bias. **(1)**

47.(i) How is a depletion region formed in p-n junction?
(ii)With the help of a labelled circuit diagram. Explain how a junction diode is used as a full-wave rectifier. Draw its input, output wave forms.
(iii)How do you obtain steady DC output from the pulsating voltage?[Delhi 2013 C]
Ans.(i) p-n Junction A p-n junction is an arrangement made by a close contact of n-type semiconductor and p-type semiconductor.There are various methods of forming p-n junction diode. In one method, an n-type germanium crystal is cut into thin slices called wafers. An aluminium film is laid on an n-type wafer which is then heated in an oven at a temperature of about 600°C. Aluminium then diffuses into the surface of wafer. In this way, a p-type semiconductor is formed on n-type semiconductor.
Formation of Depletion Region in p-n Junction In an n-type semiconductor, the concentration of electrons is more than concentration of holes. Similarly, in a p-type semiconductor, the concentration of holes is more than that of concentration of electrons. During formation of p-n junction and due to the concentration gradient across p and n-sides, holes diffuse from p-side to n-side (p—> n) and electrons diffuse from n-side to p-side (n —> p).

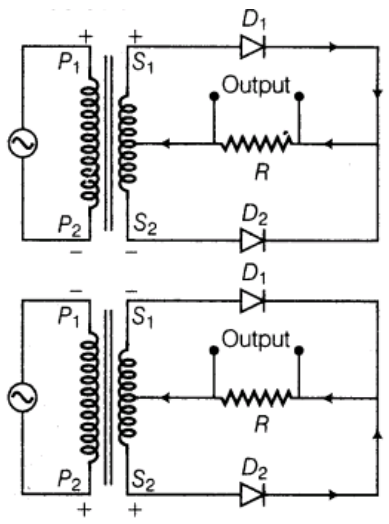


The diffused charge carriers combine with their counterparts in the immediate vicinity of the junction and neutralise each other, (l) Thus, near the junction, positive charge is built on n-side and negative charge on p-side This sets up potential difference across the junction and an internal electric field Ej directed from n-side to p-side. The equilibrium is established when the field £, becomes strong enough to stop further diffusion of the majority charge carriers (however, it helps the minority charge carriers to diffuse across the junction).The region on either side of the junction which becomes depleted (free) from the mobile charge carriers is called depletion region or **depletion layer**. The width of depletion region is of the order of 10^{-6} m.The potential difference developed across the depletion region is called the potential barrier. Potential barrier depends on dopant concentration in the semiconductor and temperature of the junction.

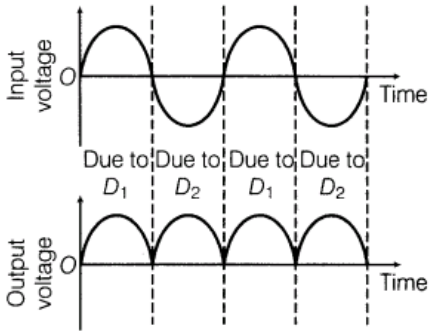
(ii)

In these type of questions, we have to mind that in full-wave rectifier, full cycle of the input will be used.

The circuit diagram of full-wave rectifier is shown below:



The input and output waveforms have been given below:



(2)

Its working based on the principle that junction diode offer very low resistance in forward bias and very high resistance in reverse bias. **(1)**

(iii) A full-wave bridge rectifier using four diodes (full-wave bridge rectifier) gives a continuous, unidirectional but pulsating output voltage or current.

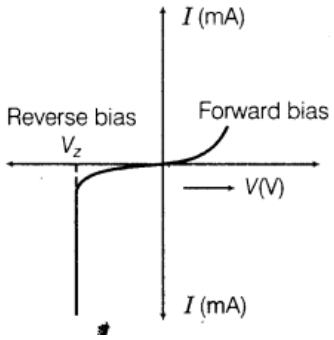
The rectified output is passed through a filter circuit which removes the ripple and an almost steady DC voltage (or current) is obtained.

48.Why is a Zener diode considered as a special purpose semiconductor diode? Draw the I-V characteristics of Zener diode and explain briefly, how reverse current suddenly

increase at the breakdown voltage? Describe briefly with the help of a circuit diagram, how a Zener diode work's to obtain a constant DC voltage from the unregulated DC output of a rectifier.[Delhi 2009 C; Foreign 2012]

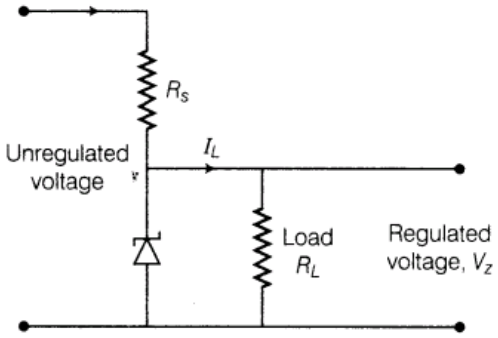
Ans. Zener diode works only in reverse breakdown region that is why it is considered as a special purpose semiconductor

I-V characteristics of Zener diode is given below: **(1)**



Reverse current is due to the flow of electrons from n —> p and holes from p —» n. As, the reverse biased voltage increase the elecHic field across the junction, increases signiffcantly and when reverse bias voltage V – V_z, then the electric field strength is high enough to pull the electrons from p-side and accelerated it to n-side.

These electrons are responsible for the high current at the breakdown.



Voltage regulator converts an unregulated DC output of rectifier into a constant regulated DC voltage, using Zener diode. The unregulated voltage is connected to the Zener diode through a series resistance R_s such that the Zener diode is reverse biased. If the input voltage increases, then current through R_s apd Zener diode increases. Thus, the voltage drop across R^ increases without any change in the voltage drop across Zener diode. This is because of the breakdown region, Zener voltage remain constant even though the current through Zener diode changes.

Similarly, if the input voltage decreases, the current through R_s and Zener diode decreases. The voltage drop across R_s, decreases without any change in the voltage across the Zener diode.

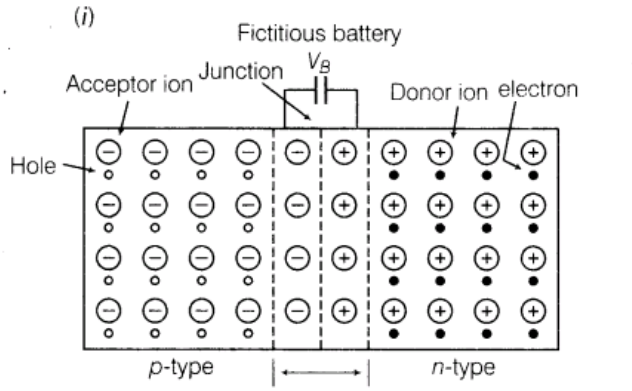
Now, any change in input voltage results the change in voltage drop across R_s, without any change in voltage across the Zener diode. Thus, Zener diode acts as a voltage regulator

49.(i) Describe briefly, with the help of a diagram, the role of the two important processes involved in the formation of a p-n junction.

(ii) Name the device which is used as a voltage regulator. Draw the necessary circuit diagram and explain its working.[HOTS; All India 2012]

Ans.

When we are dealing with depletion layer formation we have to keep in mind the majority charge carriers, diffusion will always happens from high concentration to low concentration.



The two process involved in the formation of p-n junction.

(a)Diffusion

(b)Drift

Holes and electrons diffuse from p to n and n to p respectively.

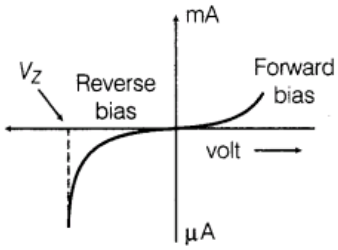
The majority charge carrier drifts under the influence of applied electric field such that

(a)holes along applied E and

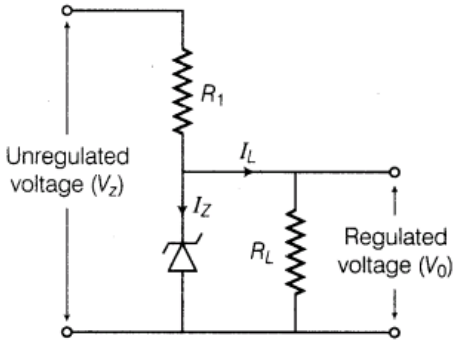
(b)electron opposite to E.

(ii) Zener diode is used as voltage regulator.

Principle Zener diode is operated in the reverse breakdown region. The voltage across it remains constant, equal to the breakdown voltage for large charge in reverse current



Characteristic of a Zener diode



(1)

50.(i) Draw the circuit diagram of a p-n junction diode in

(a)forward bias.

(b)reverse bias.

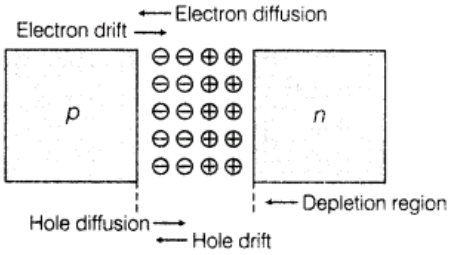
How are these circuits used to study the V-1 characteristics of a silicon diode? Draw the typical V-I characteristics.

(ii) What is a Light Emitting Diode (LED)? Mention two important advantage of LEDs over conventional lamps.[Delhi 2010 C; All India 2010]

Ans.(i) p-n Junction A p-n junction is an arrangement made by a close contact of n-type semiconductor and p-type semiconductor.There are various methods of forming p-n junction diode. In one method, an n-type germanium crystal is cut into thin slices called wafers. An aluminium film is laid on an n-type wafer which is then heated in an oven at a temperature of about 600°C. Aluminium then diffuses into the surface of wafer. In this way, a p-type semiconductor is formed on n-type semiconductor.

Formation of Depletion Region in p-n Junction In an n-type semiconductor, the

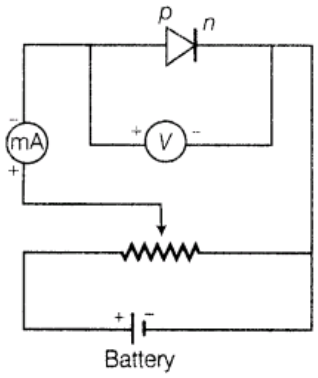
concentration of electrons is more than concentration of holes. Similarly, in a p-type semiconductor, the concentration of holes is more than that of concentration of electrons. During formation of p-n junction and due to the concentration gradient across p and n-sides, holes diffuse from p-side to n-side (p—> n) and electrons diffuse from n-side to p-side (n —> p).



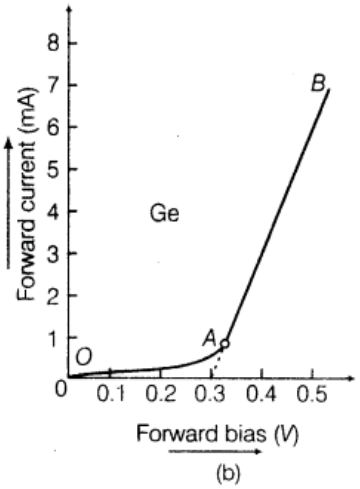
The diffused charge carriers combine with their counterparts in the immediate vicinity of the junction and neutralise each other, (l) Thus, near the junction, positive charge is built on n-side and negative charge on p-side This sets up potential difference across the junction and an internal electric field Ej directed from n-side to p-side. The equilibrium is established when the field £, becomes strong enough to stop further diffusion of the majority charge carriers (however, it helps the minority charge carriers to diffuse across the junction).The region on either side of the junction which becomes depleted (free) from the mobile charge carriers is called depletion region or **depletion layer**. The width of depletion region is of the order of 10^{-6} m.The potential difference developed across the depletion region is called the potential barrier. Potential barrier depends on dopant concentration in the semiconductor and temperature of the junction.

(a) **Forward Biased Characteristics**

The circuit diagram for studying forward biased characteristics is shown in the figure. Starting from a low value, forward bias voltage is increased step by step (measured by voltmeter) and forward current is noted (by ammeter). A graph is plotted between voltage and current. The curve so obtained is the forward characteristic of the diode.



(a)



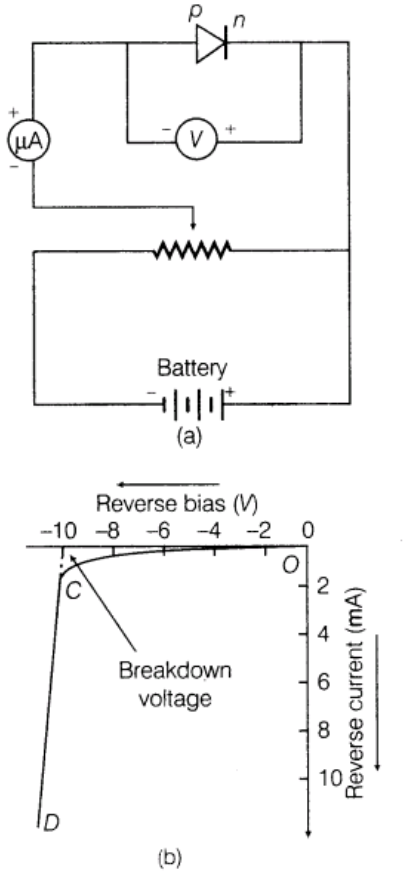
(b)

At the start when applied voltage is low, the current through the diode is almost zero. It is

because of the potential barrier, which opposes the applied voltage. Till the applied voltage exceeds the potential barrier, the current increases very slowly with increase in applied voltage (OA portion of the graph).With further increase in applied voltage, the current increases very rapidly (AB portion of the graph), in this situation, the diode behaves like a conductor. The forward voltage beyond which the current through the junction starts increasing rapidly with voltage is called knee voltage. If line AB is extended back, it cuts the voltage axis at potential barrier voltage.

(b) **Reverse Biased Characteristics**

The circuit diagram for studying reverse biased characteristics is shown in the figure.



In reverse biased, the applied voltage supports the flow of minority charge carriers across the junction. So, a very small current flows across the junction due to minority charge carriers. Motion of minority charge carriers is also supported by internal potential barrier, so all the minority carriers cross over the junction.Therefore, the small reverse current remains almost constant over a sufficiently long range of reverse bias, increasing very little with increasing voltage (OC portion of the graph). This reverse current is voltage independent upto certain voltage known as **breakdown voltage** and this voltage independent current – is called reverse saturation current.

Use of p-n Junction Characteristics in Rectification

From forward and reverse characteristics, it is clear that current flows through the junction diode only in forward bias not in reverse bias i.e. current flows only in one direction

(ii) (a) Working of LED LED is a forward biased p-n junction which converts electrical energy into optical energy of infrared and visible light region.

Being in forward bias, thin depletion layer and low potential barrier facilitate diffusion of electron and hole through the junction when high energy electron of conduction band combines with the low energy holes in valence band, then energy is released in the form of photon, may be seen in the form of light.

(b)Uses of LEDs (a) LED can operate at very low voltage and consumes less power in comparison to incandescent lamps. Unlike the lamps, they take very less operational time and have long life.

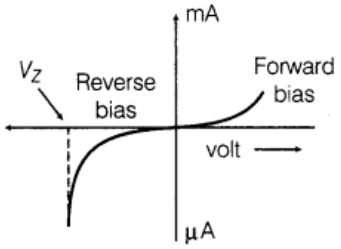
51.(i) Draw I-V characteristics of a Zener diode.

(ii)Explain with the help of a circuit diagram, the use of a Zener diode as a voltage regulator.

(iii)A photo diode is operated under reverse bias although in the forward bias, the current is known to be more than the current in the reverse bias. Explain, giving reason. [HOTS; Foreign 2010]

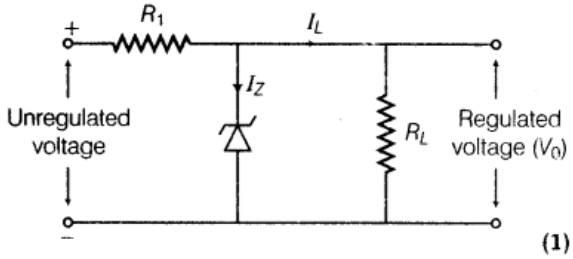
Ans. (i)Zener diode is used as voltage regulator.

Principle Zener diode is operated in the reverse breakdown region. The voltage across it remains constant, equal to the breakdown voltage for large charge in reverse current



Characteristic of a Zener diode

(ii) From the figure, it is clear that the device, X is a full-wave rectifier. Circuit diagram as shown in figure below:



(1)

Zener diode connected with unregulated DC voltage in reverse bias. When the input voltage increases, then current through R, increase and hence, voltage drop across R_p increases while voltage across the Zener diode remains constant. The voltage across Zener diode remains constant beyond Zener voltage and hence, same/constant regulated voltage is obtained across R_L.

(*iii*) In *n*-type semiconductor,

$$n_e > n_h \qquad \ldots(i)$$

On incidence of light of suitable frequency, there is equal rise in number of electrons and holes [i.e. Δn (say)]

$$\Rightarrow \quad \frac{1}{n_e} < \frac{1}{n_h} \text{ or } \frac{\Delta n}{n_e} < \frac{\Delta n}{n_h}$$

where, Δn = change in electron or hole charge carrier.

Thus, fractional change in minority charge carrier (hole) is much higher than fraction change in majority charge carrier (electron). Also, minority charge carrier contribute in drift current in reverse bias.

Thus, with incidence of light, fractional change in minority charge carrier is significant.

Therefore, photo diode should be connected in reverse bias for measuring light intensity.

52.(i) Draw a circuit arrangement for studying V-I characteristics of a p-n junction diode in(a)forward bias and (b) reverse bias.

Show typical V-I characteristics of a silicon diode.

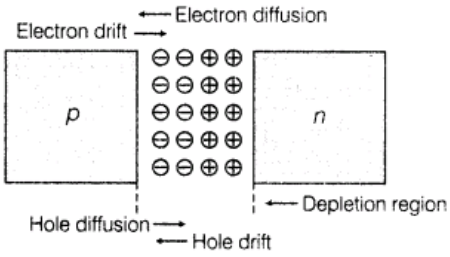
(ii) State the main practical application of LED. Explain, giving reason, why the semiconductor used for

fabrication of visible light LEDs must have a band gap of at least (nearly) 1.8 eV. [Delhi 2010 C]

Ans.**(i) p-n Junction** A p-n junction is an arrangement made by a close contact of n-type semiconductor and p-type semiconductor.There are various methods of forming p-n junction

diode. In one method, an n-type germanium crystal is cut into thin slices called wafers. An aluminium film is laid on an n-type wafer which is then heated in an oven at a temperature of about 600°C. Aluminium then diffuses into the surface of wafer. In this way, a p-type semiconductor is formed on n-type semiconductor.

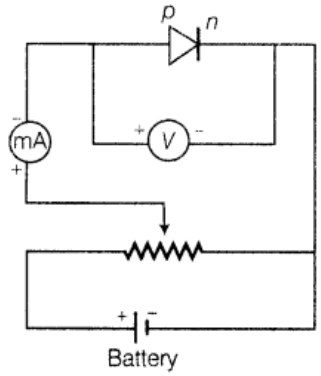
Formation of Depletion Region in p-n Junction In an n-type semiconductor, the concentration of electrons is more than concentration of holes. Similarly, in a p-type semiconductor, the concentration of holes is more than that of concentration of electrons. During formation of p-n junction and due to the concentration gradient across p and n-sides, holes diffuse from p-side to n-side (p—> n) and electrons diffuse from n-side to p-side (n —> p).



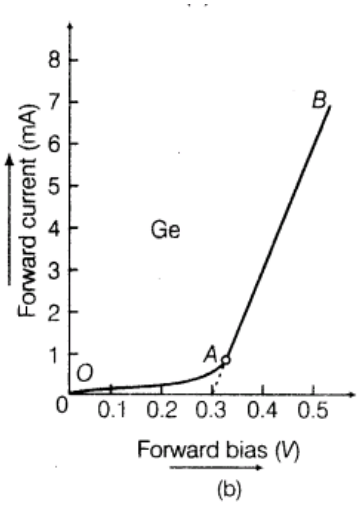
The diffused charge carriers combine with their counterparts in the immediate vicinity of the junction and neutralise each other, (l) Thus, near the junction, positive charge is built on n-side and negative charge on p-side This sets up potential difference across the junction and an internal electric field Ej directed from n-side to p-side. The equilibrium is established when the field £, becomes strong enough to stop further diffusion of the majority charge carriers (however, it helps the minority charge carriers to diffuse across the junction).The region on either side of the junction which becomes depleted (free) from the mobile charge carriers is called depletion region or **depletion layer**. The width of depletion region is of the order of 10^{-6} m.The potential difference developed across the depletion region is called the potential barrier. Potential barrier depends on dopant concentration in the semiconductor and temperature of the junction.

(a) **Forward Biased Characteristics**

The circuit diagram for studying forward biased characteristics is shown in the figure. Starting from a low value, forward bias voltage is increased step by step (measured by voltmeter) and forward current is noted (by ammeter). A graph is plotted between voltage and current. The curve so obtained is the forward characteristic of the diode.



(a)

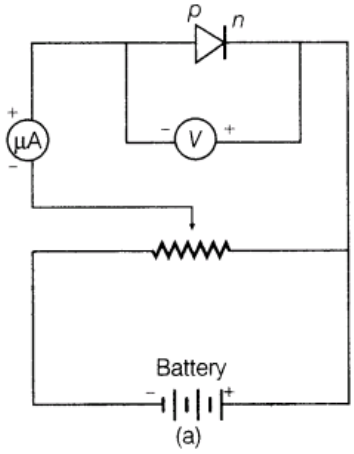


(b)

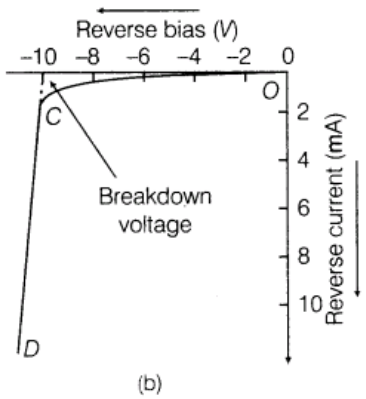
At the start when applied voltage is low, the current through the diode is almost zero. It is because of the potential barrier, which opposes the applied voltage. Till the applied voltage exceeds the potential barrier, the current increases very slowly with increase in applied voltage (OA portion of the graph).With further increase in applied voltage, the current increases very rapidly (AB portion of the graph), in this situation, the diode behaves like a conductor. The forward voltage beyond which the current through the junction starts increasing rapidly with voltage is called knee voltage. If line AB is extended back, it cuts the voltage axis at potential barrier voltage.

(b) **Reverse Biased Characteristics**

The circuit diagram for studying reverse biased characteristics is shown in the figure.



(a)



(b)

In reverse biased, the applied voltage supports the flow of minority charge carriers across the junction. So, a very small current flows across the junction due to minority charge carriers. Motion of minority charge carriers is also supported by internal potential barrier, so all the minority carriers cross over the junction.Therefore, the small reverse current remains almost constant over a sufficiently long range of reverse bias, increasing very little with increasing voltage (OC portion of the graph). This reverse current is voltage independent upto certain voltage known as **breakdown voltage** and this voltage independent current – is called reverse

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Use of p-n Junction Characteristics in Rectification

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(ii) Working of LED LED is a forward biased p-n junction which converts electrical energy into optical energy of infrared and visible light region.

Being in forward bias, thin depletion layer and low potential barrier facilitate diffusion of electron and hole through the junction when high energy electron of conduction band combines with the low energy holes in valence band, then energy is released in the form of photon, may be seen in the form of light.

(a) Semiconductors with appropriate band gap (E_g) close to 1.5 eV are preferred to make LED size GaAs, CdTe, etc.the other reasons to select these materials e high optical absorption, availability of raw material and low cost

(b) Uses of LEDs

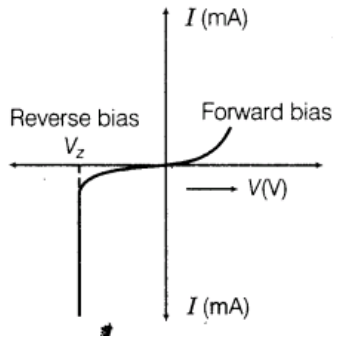
(i) LED can operate at very low voltage and consumes less power in comparison to incandescent lamps

(ii) Unlike the lamps, they take very less operational time and have long life.

53.How is a Zener diode fabricated so as to make it a special purpose diode? Draw 7-V characteristics of Zener diode and explain the significance of breakdown voltage, (ii) Explain briefly, with the help of a circuit diagram, how a p-n junction diode works as a half-wave rectifier. [Delhi 2009c]

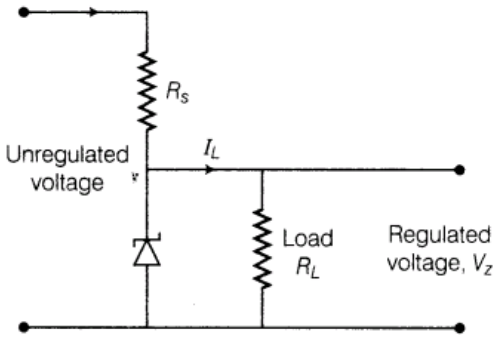
Ans.(i) Zener diode works only in reverse breakdown region that is why it is considered as a special purpose semiconductor

I-V characteristics of Zener diode is given below: **(1)**



Reverse current is due to the flow of electrons from n —> p and holes from p —» n. As, the reverse biased voltage increase the elecHic field across the junction, increases signiffcantly and when reverse bias voltage V – V_z, then the electric field strength is high enough to pull the electrons from p-side and accelerated it to n-side.

These electrons are responsible for the high current at the breakdown.



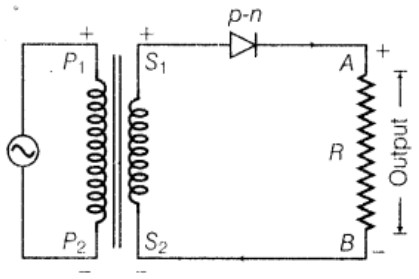
Voltage regulator converts an unregulated DC output of rectifier into a constant regulated DC voltage, using Zener diode. The unregulated voltage is connected to the Zener diode through a series resistance R_s such that the Zener diode is reverse biased. If the input voltage increases, then current through R_s apd Zener diode increases. Thus, the voltage drop across R^

increases without any change in the voltage drop across Zener diode. This is because of the breakdown region, Zener voltage remain constant even though the current through Zener diode changes.

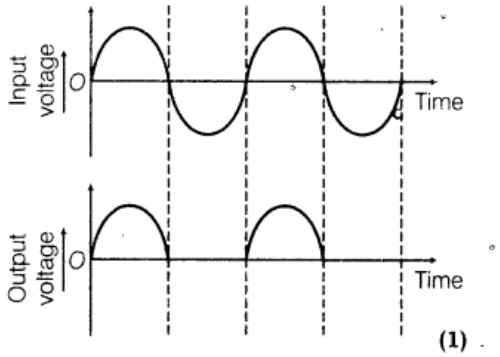
Similarly, if the input voltage decreases, the current through R_s and Zener diode decreases. The voltage drop across R_s, decreases without any change in the voltage across the Zener diode.

Now, any change in input voltage results the change in voltage drop across R_s, without any change in voltage across the Zener diode. Thus, Zener diode acts as a voltage regulator

(ii) Circuit diagram of p-n junction diode as half-wave rectifier is shown below



Diode conducts corresponding to positive half cycle and does not conduct during negative half cycle hence, AC is converted by diode into unidirectional pulsating DC. This action is known as half-wave rectification.



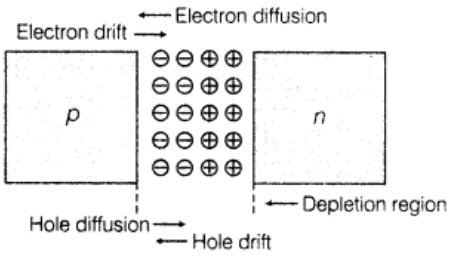
(1)

54.(i) Draw the typical shape of the V-I characteristics of a p-n junction diode both in (a) forward(b)reverse bias configuration. How do we infer, from these characteristics that a diode can be used to rectify alternating voltages?

(ii) Draw the circuit diagram of a full-wave rectifier using a centre-tap transformer and two p-n junction diodes. Give a brief description of the working of this circuit. [Delhi 2009 C]

Ans.**(i) p-n Junction** A p-n junction is an arrangement made by a close contact of n-type semiconductor and p-type semiconductor.There are various methods of forming p-n junction diode. In one method, an n-type germanium crystal is cut into thin slices called wafers. An aluminium film is laid on an n-type wafer which is then heated in an oven at a temperature of about 600°C. Aluminium then diffuses into the surface of wafer. In this way, a p-type semiconductor is formed on n-type semiconductor.

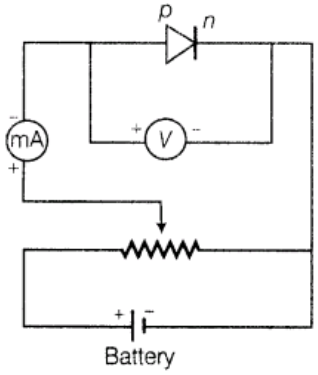
Formation of Depletion Region in p-n Junction In an n-type semiconductor, the concentration of electrons is more than concentration of holes. Similarly, in a p-type semiconductor, the concentration of holes is more than that of concentration of electrons. During formation of p-n junction and due to the concentration gradient across p and n-sides, holes diffuse from p-side to n-side (p—> n) and electrons diffuse from n-side to p-side (n —> p).



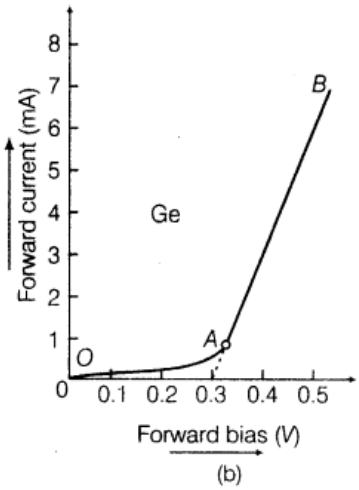
The diffused charge carriers combine with their counterparts in the immediate vicinity of the junction and neutralise each other, (l) Thus, near the junction, positive charge is built on n-side and negative charge on p-side This sets up potential difference across the junction and an internal electric field Ej directed from n-side to p-side. The equilibrium is established when the field £, becomes strong enough to stop further diffusion of the majority charge carriers (however, it helps the minority charge carriers to diffuse across the junction).The region on either side of the junction which becomes depleted (free) from the mobile charge carriers is called depletion region or **depletion layer**. The width of depletion region is of the order of 10^{-6} m.The potential difference developed across the depletion region is called the potential barrier. Potential barrier depends on dopant concentration in the semiconductor and temperature of the junction.

(a) **Forward Biased Characteristics**

The circuit diagram for studying forward biased characteristics is shown in the figure. Starting from a low value, forward bias voltage is increased step by step (measured by voltmeter) and forward current is noted (by ammeter). A graph is plotted between voltage and current. The curve so obtained is the forward characteristic of the diode.



(a)



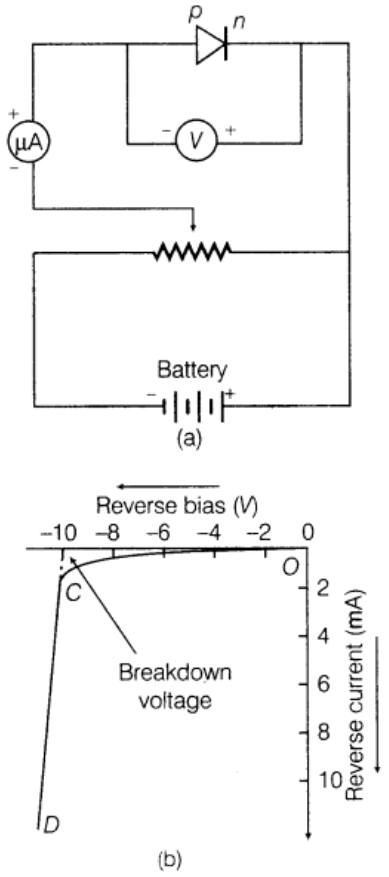
(b)

At the start when applied voltage is low, the current through the diode is almost zero. It is because of the potential barrier, which opposes the applied voltage. Till the applied voltage exceeds the potential barrier, the current increases very slowly with increase in applied voltage (OA portion of the graph).With further increase in applied voltage, the current increases very rapidly (AB portion of the graph), in this situation, the diode behaves like a conductor. The forward voltage beyond which the current through the junction starts increasing rapidly with

voltage is called knee voltage. If line AB is extended back, it cuts the voltage axis at potential barrier voltage.

(b) **Reverse Biased Characteristics**

The circuit diagram for studying reverse biased characteristics is shown in the figure.



In reverse biased, the applied voltage supports the flow of minority charge carriers across the junction. So, a very small current flows across the junction due to minority charge carriers. Motion of minority charge carriers is also supported by internal potential barrier, so all the minority carriers cross over the junction.Therefore, the small reverse current remains almost constant over a sufficiently long range of reverse bias, increasing very little with increasing voltage (OC portion of the graph). This reverse current is voltage independent upto certain voltage known as **breakdown voltage** and this voltage independent current – is called reverse saturation current.

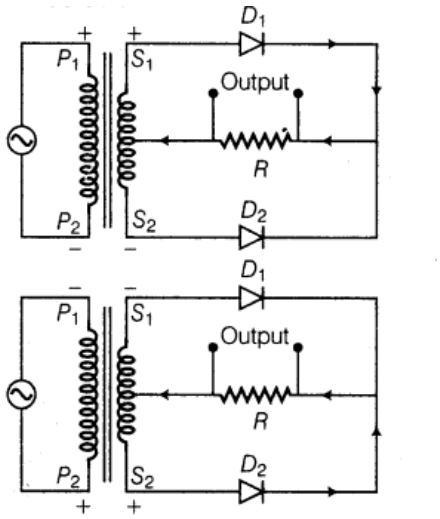
Use of p-n Junction Characteristics in Rectification

From forward and reverse characteristics, it is clear that current flows through the junction diode only in forward bias not in reverse bias i.e. current flows only in one direction

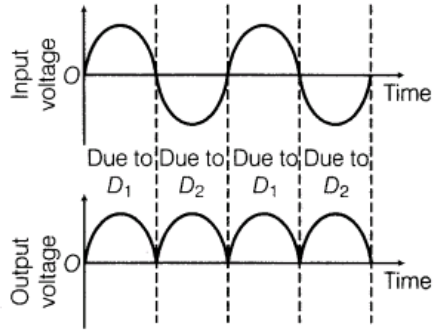
(ii)

In these type of questions, we have to mind that in full-wave rectifier, full cycle of the input will be used.

The circuit diagram of full-wave rectifier is shown below:



The input and output waveforms have been given below:



(2)

Its working based on the principle that junction diode offer very low resistance in forward bias and very high resistance in reverse bias. **(1)**

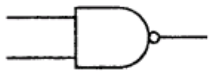
LogicGates, Transistors and its Applications

1 Mark Questions

1.In a transistor, doping level in base is increased slightly. How will it affect
(i)collector current and
(ii)base current? [Delhi 2011]
Ans.(i) Collector current decreases.
(ii) Base current increases

2.Draw the logic circuit of a NAND gate and write its truth table.[Foreign 20113]
Ans.

Logic circuit of a NAND gate



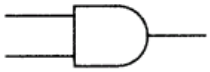
Truth table

A	B	$Y = \overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

(1/2 × 2 = 1)

3.Draw the logic circuit of AND gate and write its truth table.[Foreign 2011]
Ans.

Logic circuit of a AND gate

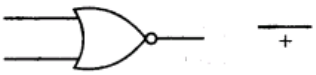


Truth table

A	B	Y = AB
0	0	0
0	1	0
1	0	0
1	1	1

4.Draw the logic circuit of NOT gate and write its truth table.[Foreign 2011]
Ans.

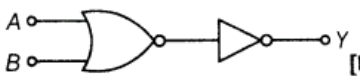
Logic circuit of a NOT gate



Truth table

A	$Y = \bar{A}$
0	1
1	0

5. Write the truth table for the following circuit. Name the equivalent gate that this circuit represents.



[Foreign 2010]

Ans.

The given combination consists of NOR gate and NOT gate, so equivalent gate is OR gate.

Truth table

A	B	$Y = A + B$
0	0	0
0	1	1
1	0	1
1	1	1

(1/2 × 2 = 1)

From the truth table, it is clear that the output is 1 only when at least one of the inputs is at the high state i.e. 1

6. The truth table of a logic gate has the form given here. Name this gate and draw its symbol.

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

[All India 2010C]

Ans.

Logic gate is NOR gate.

Symbol

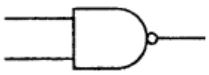
7. The truth table of a logic gate has the form given here. Name this gate and draw its symbol.

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

[All India 2010C]

Ans.

Logic circuit of a NAND gate



Truth table

A	B	$Y = \overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

(1/2 × 2 = 1)

8.Give the logic symbol of NOR gate.[All India 2009]

Ans.

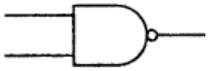
Logic gate is NOR gate.

Symbol

9.Give the logic symbol of NAND gate. [All India 2009]

Ans.

Logic circuit of a NAND gate



Truth table

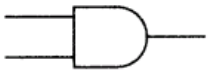
A	B	$Y = \overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

(1/2 × 2 = 1)

10.Give the logic symbol of AND gate.[All India 2009]

Ans.

Logic circuit of a AND gate



Truth table

A	B	$Y = AB$
0	0	0
0	1	0
1	0	0
1	1	1

11.Define current amplification factor in common-emitter mode of transistor. [Delhi 2009 C, All India 2010 C]

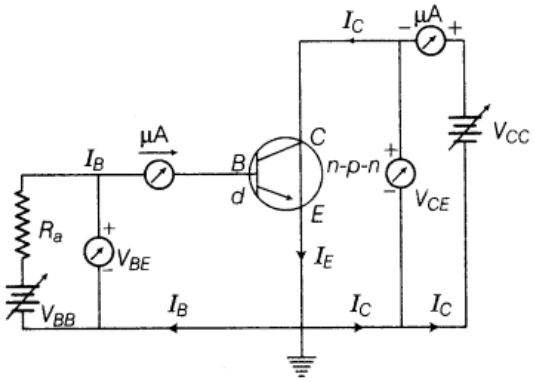
Ans.

Current amplification factor in common emitter mode, $\beta_{AC} = \left| \frac{\Delta I_C}{\Delta I_B} \right|_{V_{CE} = \text{constant}}$ **(1)**

2 Marks Questions

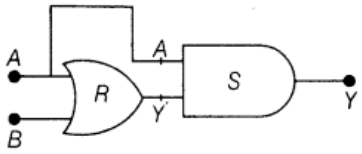
12.Draw a circuit diagram of n-p-n transistor amplifier in CE configuration. Under what condition does the transistor act as an amplifier? [All India 2014]

Ans. Circuit diagram of n-p-n transistor amplifier in CE configuration is given below



The condition for the amplifier to work is that the base-emitter junction should be forward biased and collector-base junction should be reversed biased

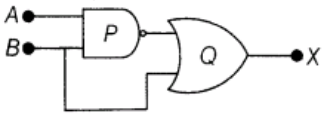
13. Write the truth table for the combination of the gates shown. Name the gates used. **[All India 2014]**



Ans.

A	B	$Y' = A + B$	$Y = A \cdot (A + B)$
0	0	0	0
0	1	1	0
1	0	1	1
1	1	1	1

14. Identify the logic gates marked *P* and *Q* in the given circuit. Write the truth table for the combination.



[Delhi 2014]

Ans.

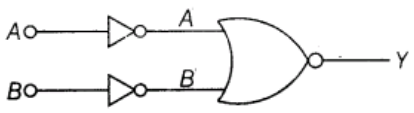
The logic gates are Pis NAND gate and Q is OR gate.

The truth table is given as shown in below:

A	B	$A \cdot B$	$\overline{A \cdot B}$	$X = B + \overline{A \cdot B}$
0	0	0	1	1
0	1	0	1	1
1	0	0	1	1
1	1	1	0	1

15.The outputs of two NOT gates are fed to a NOR gate. Draw the logic circuit of the combination of gates. Give its truth table. Identify the gate represented by this combination. [Delhi 2014 C]

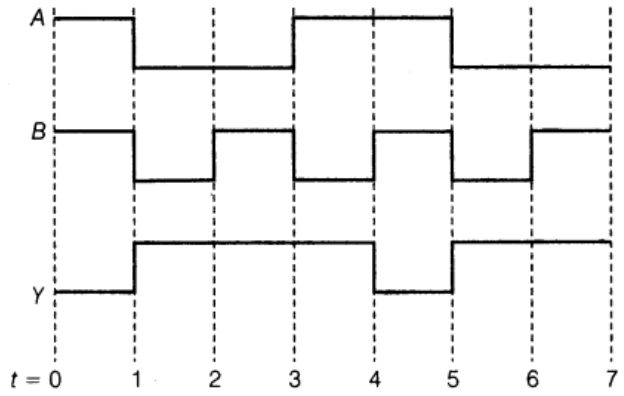
Ans.



16.The input wave forms A and B and the output waveform Y of a gate are shown below.

Name the gate it represents, write its truth table and draw the logic symbol of this gate.

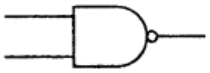
represents, write its truth table and draw the logic symbol of this gate.



[All India 2014C]

Ans.

Logic circuit of a NAND gate

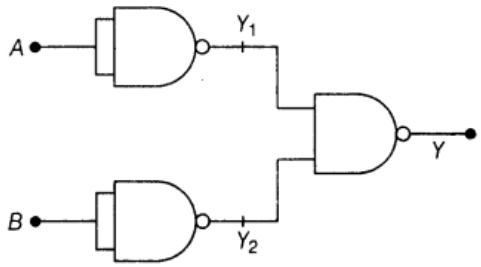


Truth table

A	B	$Y = \overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

(1/2 × 2 = 1)

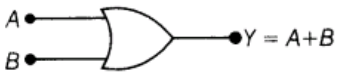
17. Identify the equivalent gate represented by the circuit shown in the figure. Draw its logic symbol and write the truth table.



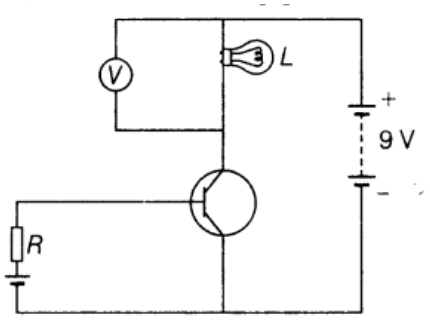
[Foreign 2014]

Ans.

and logic symbol is



18.In the given circuit diagram, a voltmeter V is connected across a lamp L. How would
(i)the brightness of the lamp and
(ii)voltmeter reading V be affected if the value of resistance R is decreased? Justify your answer.



Ans.

The given figure in question is common-emitter (*CE*) configuration of an *n-p-n* transistor. The input circuit is forward biased and collector circuit is reverse biased. **(1)**

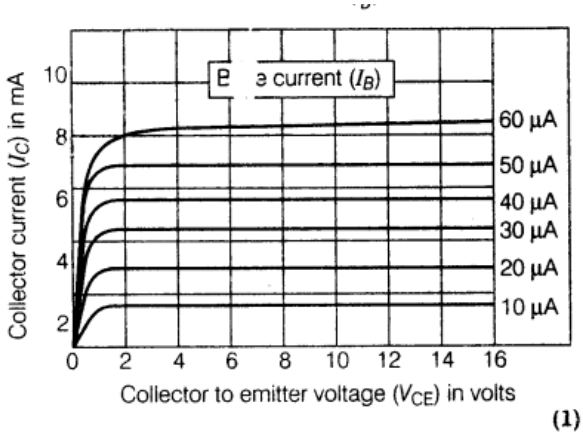
As, the base resistance *R* decreases, the input circuit will become more forward biased thus, decreasing the base current (I_B) and increasing the emitter current (I_E). This will increase the collector current (I_C) as $I_E = I_B + I_C$.

When I_C increases which flows through the lamp, the voltage across the bulb will also increase thus making the lamp brighter and as the voltmeter is connected in parallel with the lamp, the reading in the voltmeter will also increases. **(1)**

19.Draw a typical output characteristics of an n-p-n transistor in CE Show how these characteristics can be used to determine output resistance?[All India 2013]

Ans.

Output characteristics is the plot between collector-emitter voltage (V_{CE}) and the collector current (I_C) at different constant values of base current (I_B).



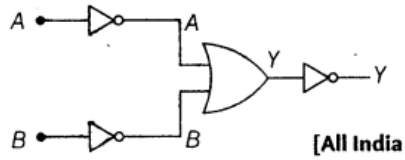
(1)

Output resistance is defined as the ratio of variation of collector-emitter voltage (ΔI_C) and corresponding change in collector current (ΔI_C) when base current remains constant. Initially with the increase in V_{CE} the collector current increases almost linearly, this is because the junction is not reverse biased. When the supply is more

than required to reverse bias, the base-collector junction, i_C increases very little with V_{CE}.

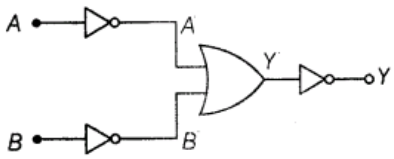
The reciprocal of slope of the linear part of the curve gives the value of output resistance, i.e. $r_0 = \left(\frac{\Delta V_{CE}}{\Delta I_C}\right)_{I_B}$ **(1)**

20. In the circuit shown in the figure, identify the equivalent gate of the circuit and make its truth table.



[All India 2013]

Ans.



$A' = \overline{A}, B' = \overline{B}$

$Y' = A'B'$

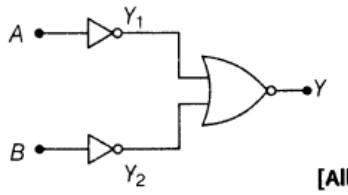
$Y = \overline{Y'} = \overline{A' + B'} \Rightarrow = \overline{\overline{A}.\overline{B}} = A.B$ **(1)**

The equivalent gate of the given circuit is AND gate.

Truth table

A	B	A′	B′	Y′	Y
1	1	0	0	0	1
1	0	0	1	1	0
0	1	1	0	1	0
0	0	1	1	1	0

21. In the circuit shown in the figure, identify the equivalent gate of the circuit and make its truth table.



[All India 2013]

Ans.

$Y_1 = \overline{A}$ and $Y_2 = \overline{B}$

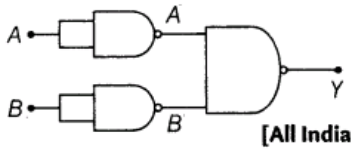
$\therefore \quad Y = \overline{Y_1 + Y_2} = \overline{Y}_1.\overline{Y}_2 = \overline{\overline{A}}.\overline{\overline{B}} = A.B$

The equivalent gate of the given circuit is AND gate. **(1)**

Truth table

A	B	Y_1	Y_2	Y
1	1	0	0	1
1	0	0	1	0
0	1	1	0	0
0	0	1	1	0

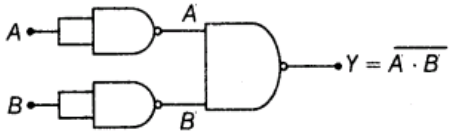
22. In the circuit shown in the figure, identify the equivalent gate of the circuit and make its truth table.



[All India 2013]

Ans.

$Y = \overline{A' \cdot B'} = \overline{\overline{A}} + \overline{\overline{B}} = A + B$



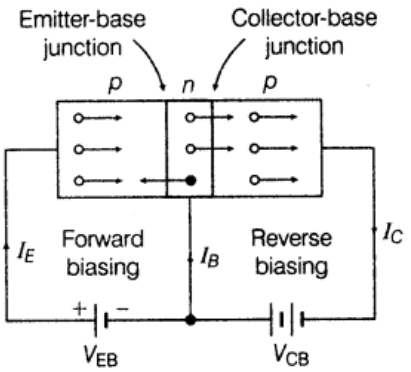
Truth table

A	B	$A' = \overline{A \cdot A}$	$B' = \overline{B \cdot B}$	$Y = \overline{A \cdot B} = A + B$
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	1

Thus, the equivalent gate is OR gate. **(1)**

23.Describe briefly with the help of a circuit diagram, how the flow of current carriers in a p-n-p transistor is regulated with emitter-base junction in forward biased and base-collector junction in reverse biased. [All India 2012]

Ans.

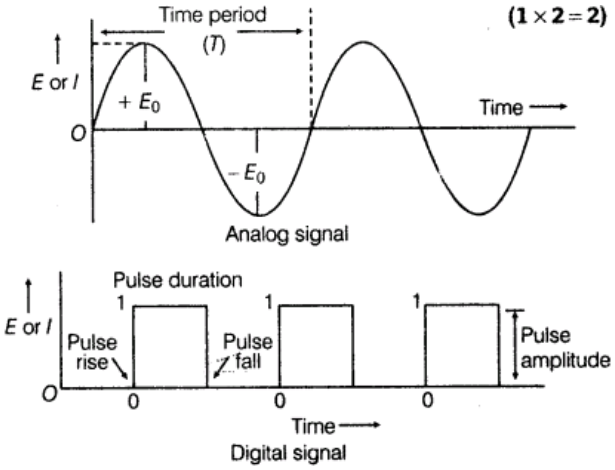


Heavily doped emitter is subjected to electric field by emitter-base battery and consequently, holes gets drifted towards collector through thin and lightly doped base region. Nearly 5% hole, which drifted from emitter combined with electron in base region and remaining nearly 95% hole reaches to collector under the influence V_{CE}.

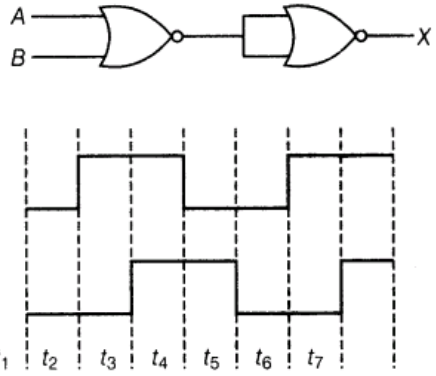
24.Distinguish between analog signal and digital signal. [All India 2012]

Ans.A signal in which current or voltage changes continuously with the time is called analog signals. A signal in which current or voltage can take only two discrete values is called a digital signal.

(1 × 2 = 2)

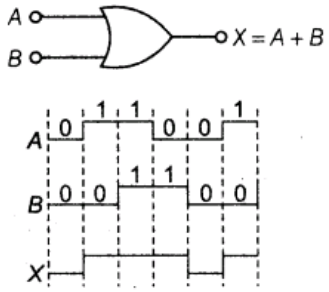


25.Draw the output waveform at X using the given inputs, A and B for the logic circuit shown below. Also, identify the logic operation performed by this circuit



[Delhi 2012; 2011]

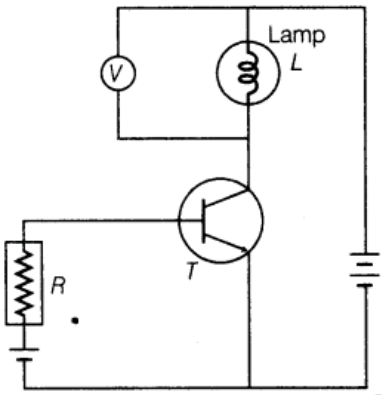
Ans. Equivalent gate is OR gate. If input A or B or both are 1, then the output of OR gate is 1.
Boolean expression of OR gate is given as A + B = X
Logic symbol of OR gate and the output waveform as shown below



Truth table

Inputs		Output
A	B	X = A + B
0	0	0
0	1	1
1	0	1
1	1	1

26.In the given circuit, a voltmeter V is connected across lamp L What changes would you observe in the lamp L and the voltmeter V if the value of resistor R is reduced?

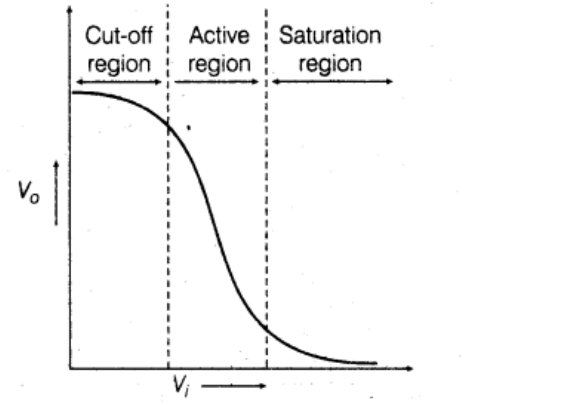


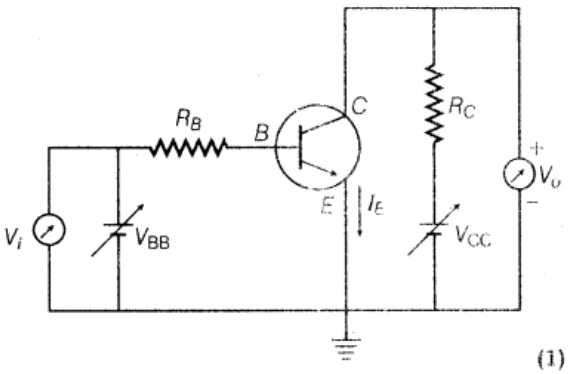
[Delhi 2011C]

Ans. Lamp glows brighter and voltmeter reading increases with the decrease of R. Input current increase which in turn by transistor action lead to increase collector current. This makes lamp brighter and hence, voltmeter reading goes up.

27.Draw the transfer characteristic curve of a base-biased transistor in CE Explain clearly how the active region of the V_0 versus Vi. curve, in a transistor is used as an amplifier? [Delhi 2011]

Ans.The transfer characteristic curve of base biased transistor in CE configuration as shown below:





(1)

As, V_i increases slightly above 0.6 V, a current I_C flows in the output circuit and the transistor arrives in active state.

$$\therefore \quad V_o = V_{CC} - I_C R_C$$

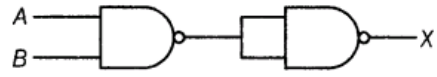
with the growth of I_C, V_C decrease linearly.

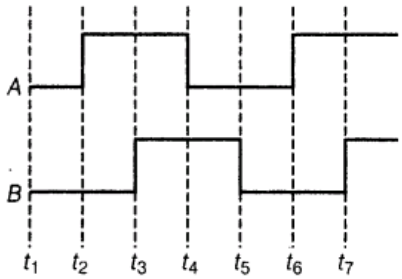
Also, voltage gain in active state is given by

$$A_V = -\frac{\Delta V_o}{\Delta V_i} \qquad (\because \Delta V_o > \Delta V_i)$$

There is voltage gain and hence amplification of voltage takes place. Thus, transistor used as an amplifier. (3)

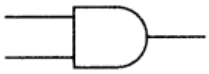
28.Draw the output waveform at X using the given inputs, A and B for the logic circuit shown below. Also, identify the logic operation performed by this circuit.[Delhi 2011; 2008]





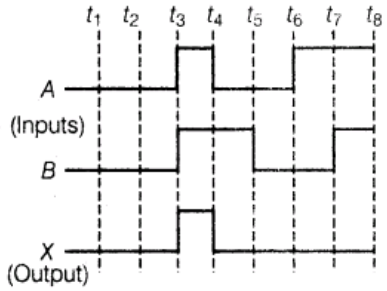
Ans.

Logic circuit of a AND gate



Truth table

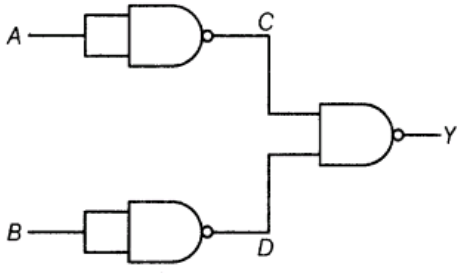
A	B	Y = AB
0	0	0
0	1	0
1	0	0
1	1	1



Logic operation of the graphic circuit

$$X = \overline{\overline{A \cdot B}} = AB$$

29.Write the truth table for the logic circuit shown below and identify the logic operation performed by this Circuit. [Delhi 2011]



Ans.

The truth table of given system is as follows:

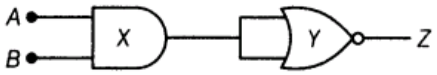
(1/2)

A	B	$C = A \cdot \overline{A}$	$D = \overline{A} \cdot \overline{B}$	$Y = \overline{C} \cdot \overline{D}$
0	0	1	1	0
1	1	0	0	1
1	0	0	1	1
0	1	1	0	1

(1½)

The correct performs the logic operation of OR gate.

30.Identify the logic gates X and Y in the figure. Write down the truth table of output Z for all possible inputs A and [All India 2011 c]



Ans.

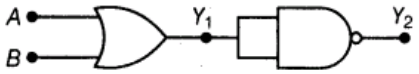
X : AND gate

Y : NOT gate

Z : $Y = \overline{A \cdot B}$

A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

31. (*i*) For the digital circuit given below, write the truth table showing outputs Y_1 and Y_2 for all possible inputs of A and B.



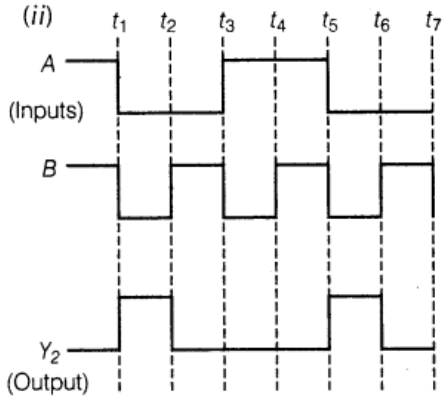
(ii) Show output waveform for all possible inputs of A and B.[All India 2011 C]

Ans.

(*i*) As, $Y_1 = A + B$, $Y_2 = \overline{A + B}$

A	B	Y_1	Y_2
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

(*ii*)

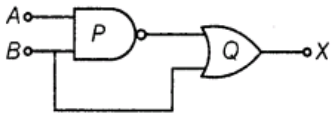


32. (*i*) Identify the logic gates marked *P* and *Q* in the given logic circuit.

(*ii*) Write down the output at *X* for the inputs,

$A = 0, B = 0$ and $A = 1, B = 1$.

[All India 2010]



Ans.

(*i*) *P* : NAND gate

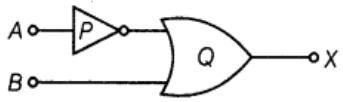
Q : OR gate

(*ii*) $X = \overline{A \cdot B} + B$ **(1/2 × 2 = 1)**

For $A = 0, B = 0, X = \overline{0.0} + 0 = 1 + 0 = 1$

For $A = 1, B = 1, X = \overline{1.1} + 1 = 0 + 1 = 1$h. **(1)**

33. (*i*) Identify the logic gates marked *P* and *Q* in the given logic circuit.



(*ii*) Write down the output at *X* for the inputs $A = 0, B = 0$ and $A = 1, B = 1$, **[All India 2010]**

Ans.

(*i*) *P* : NOT gate and *Q* : OR gate

(*ii*) $X = (\overline{A} + B)$ **(1/2 × 2 = 1)**

For $A = B = 0, X = \overline{0} + 0 = 1 + 0 = 1$

For $A = 1, B = 1, X = \overline{1} + 1 = 0 + 1 = 1$ **(1)**

34. Define the following terms.

(*i*) Input resistance r_i.

(*ii*) Current amplification factor β of a transistor used in its *CE* configuration. **[All India 2010C]**

Ans.

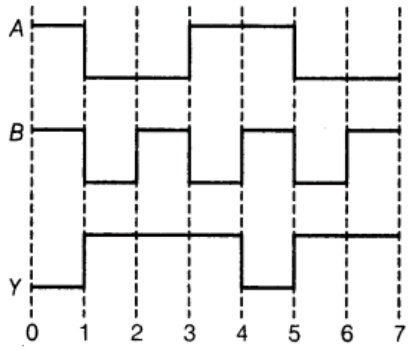
(*i*) The input resistance, r_i of transistor in *CE* configuration is defined as the ratio of small change in base-emitter voltage to the corresponding small change in the base current, when the collector emitter voltage is kept constant, i.e.

$$r_i = \left(\frac{\Delta V_{EB}}{\Delta I_B}\right)_{V_{CE}\text{ = constant}}$$ **(1)**

(*ii*) The current amplification factor of a transistor in *CE* configuration is equal to the ratio of the small change in the collector current (ΔI_C) to the small change in base current when collector-emitter voltage is kept constant, i.e.

$$\beta = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}\text{ = constant}} \quad \textbf{(1)}$$

35. The following figure shows the input waveforms A, B and the output waveform Y of a gate. Identify the gate, write its truth table and draw its logic symbol. **[Delhi 2009]**



Ans.

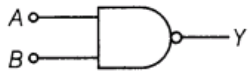
Gate From the given output waveform, it is clear that output is zero only when both inputs are 1, so the gate is NAND gate. **(1/2)**

Truth table

A	*B*	*Y*
0	0	1
0	1	1
1	0	1
1	1	0

(1)

Logic symbol



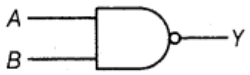
$Y = \overline{A \cdot B}$ **(1/2)**

36.The output of a 2-input AND gate is fed to a NOT gate. Give the name of the combination and its logic symbol. Write down its truth table.[Foreign 2008, Delhi 2009]

Ans.

When output of a two inputs AND gate is fed to a NOT gate, then the combination is called NAND gate

Logic symbol



(1)

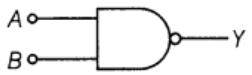
Gate From the given output waveform, it is clear that output is zero only when both inputs are 1, so the gate is NAND gate. **(1/2)**

Truth table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

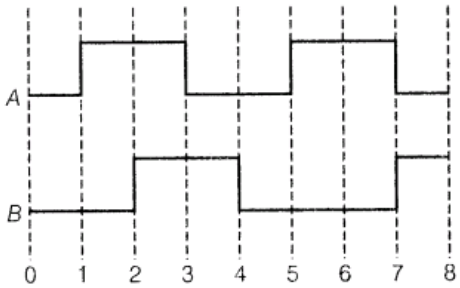
(1)

Logic symbol



$Y = \overline{A \cdot B}$ **(1/2)**

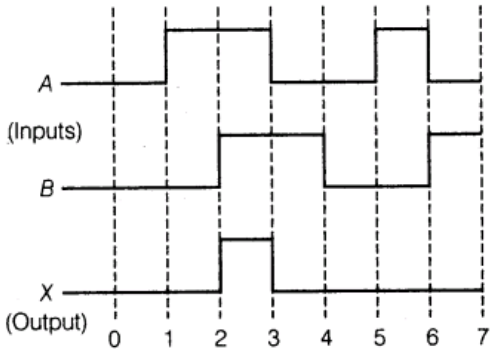
37. (*i*) Sketch the output waveform from an AND gate for the inputs, *A* and *B* shown in the figure.



(*ii*) If the output of the above AND gate is fed to a NOT gate, name the gate of the combination, so formed. **[Delhi 2009]**

Ans.

(*i*) Output of AND gate is $Y = A \cdot B$. In this case, output will be 1 only when both inputs are 1.



38. Draw the logic symbol of the gate whose truth table is given as below:

Inputs		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

If this, logic gate is connected to NOT gate, what will be the output when

(i)A = 0, B = 0 and

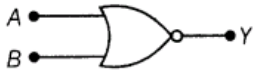
(ii)A = 1 B = 1?

Draw the logic symbol of the Combination.[Foreign 2009]

Ans.

NOR gate

Symbol



(1)

On connecting the given gate with NOT gate, the output

$$Y = \overline{\overline{A + B}} = A + B$$

(*i*) If $A = 0, B = 0 \Rightarrow Y = A + B = 0 + 0 = 0$

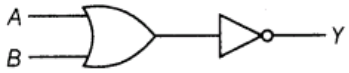
(*ii*) If $A = 1, B = 1$

$Y = 1 + 1 = 1.$ **(1)**

39.A logic gate is obtained by applying output of OR gate to a NOT gate.Name the gate so formed. Write the symbol and truth table of this gate.[Foreign 2009]

Ans.

Logic gate



Equivalent so formed gate is NOR gate.

Symbol

(1)

Truth table $Y = \overline{A + B}$

A	$\bar{A}$	B	$\bar{B}$	$Y = \bar{A} \cdot \bar{B}$
0	1	0	1	1
0	1	1	0	0
1	0	0	1	0
1	0	1	0	0

40.A logic gate is obtained by applying output of AND gate to a NOT gate. Name the gate so formed. Write the symbol and truth table of this gate.[Foreign 2009]

Ans.

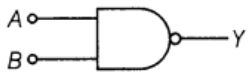
Gate From the given output waveform, it is clear that output is zero only when both inputs are 1, so the gate is NAND gate. **(1/2)**

Truth table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

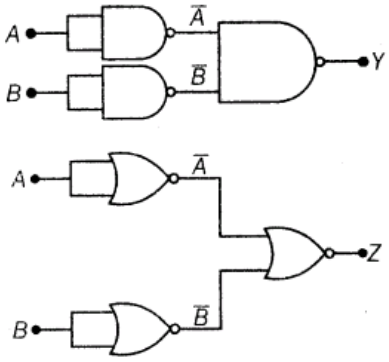
(1)

Logic symbol



$Y = \overline{A \cdot B}$ **(1/2)**

41.The two circuits shown here are a combination



(i)Three NAND gates.

(ii)Three NOR gates.

Write truth tables for each of these combinations. [Delhi 2009 c]

Ans.

(*i*)

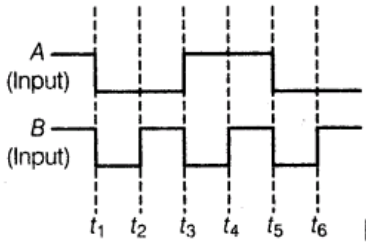
A	$\overline{A}$	B	$\overline{B}$	$Y = \overline{\overline{A} + \overline{B}} = A + B$
0	1	0	1	0
0	1	1	0	1
1	0	0	1	1
1	0	1	0	1

(1)

(*ii*)

A	$\overline{A}$	B	$\overline{B}$	$Y = \overline{\overline{A} + \overline{B}} = A \cdot B$
0	1	0	1	0
0	1	1	0	0
1	0	0	1	0
1	0	1	0	1

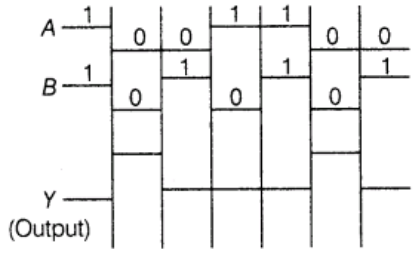
42.The given inputs A, B are fed to a 2-input NAND gate. Draw the output waveform of the gate.



[Delhi 2008]

Ans.

Output of NAND gate is $Y = \overline{A \cdot B}$, the output will be 1 only when both inputs are zero.



(2)

43.In the output of a 2-input NOR gate is fed as both inputs, A and B to another NOR gate,

write down a truth table to find the final output, for all combinations of A, B.[Delhi 2008]

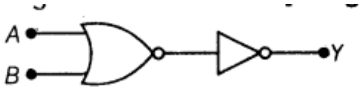
Ans.

Equivalent gate is OR gate.

Truth table

A	B	Y = A + B
0	0	0
0	1	1
1	0	1
1	1	1

44.Write the truth table and draw the logic symbol of the gate for the circuit given as below: [Foreign 2008]



Ans.

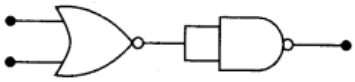
Equivalent gate is OR gate.

Symbol

Truth table

A	B	Y = A + B
0	0	0
0	1	1
1	0	1
1	1	1

45. Write the truth table and draw the logic symbol of the gate for the circuit given as below: [Foreign 2008]



Ans.

Equivalent gate is AND gate

Symbol

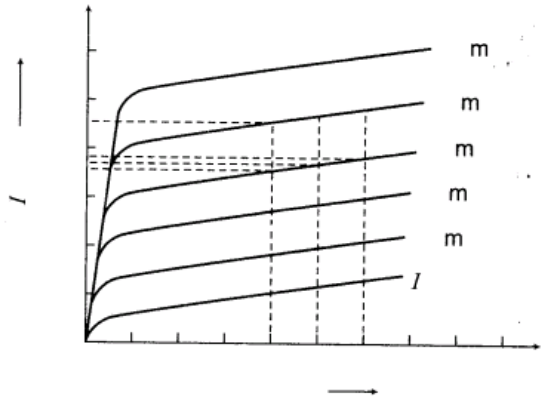
AND gate

Truth table

A	B	Y = A
0	0	0
0	1	0
1	0	0
1	1	1

3 Marks Questions

46.Output characteristics of an n-p-n transistor in CE configuration is -shown in the figure. Determine



(*i*) dynamic output resistance

(*ii*) DC current gain and

(*iii*) AC current gain at an operating point $V_{CE} = 10$ V, when $I_B = 30$ μA. **[Delhi 2013]**

Ans.

(*i*) Dynamic output resistance is given as

$$R_{out} = \left(\frac{\Delta V_{CE}}{\Delta I_C}\right)_{I_B = \text{constant}} = \frac{12 - 8}{(3.6 - 3.4) \times 10^{-3}}$$

$$= \frac{4}{0.2 \times 10^{-3}} = 20\ \text{k}\Omega \qquad \textbf{(1)}$$

(*ii*) DC current gain,

$$\beta_{DC} = \frac{I_C}{I_B} = \frac{3.5\,\text{mA}}{30\,\mu\text{A}} = \frac{3.5 \times 10^{-3}}{30 \times 10^{-6}}$$

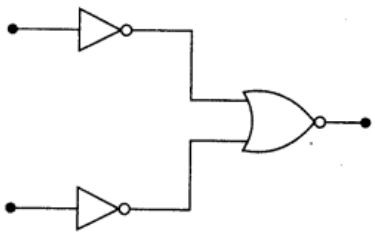
$$= \frac{350}{3} = 116.67 \qquad \textbf{(1)}$$

(*iii*) AC current gain,

$$\beta_{DC} = \frac{\Delta I_C}{\Delta I_B} = \frac{(4.7 - 3.5)\,\text{mA}}{(40 - 30)\,\mu\text{A}}$$

$$= \frac{1.2 \times 10^{-3}}{10 \times 10^{-6}} = 120$$

47.You are given a circuit below. Write its truth table. Hence, identify the logic operation carried out by this circuit. Draw the logic symbol of the gate which Corresponds to [All India 2011]



Ans.

Truth table of given circuit is as shown below:

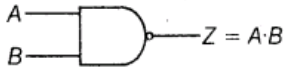
A	B	$X = \bar{A}$	$Y = \bar{B}$	$Z = \overline{X + Y}$
0	0	1	1	0
1	0	0	1	0
0	1	1	0	0
1	1	0	0	1

This circuit carries out by the logic operation of AND gate which can also be verified by De-Morgan's theorem

$$Z = \overline{X + Y} = \overline{\bar{A} + \bar{B}} = \bar{\bar{A}} + \bar{\bar{B}} = A \cdot B$$

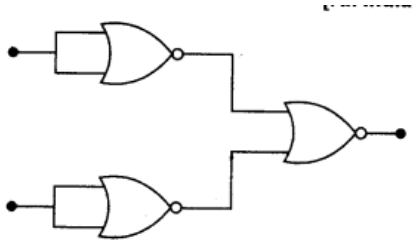
So, the circuit corresponds to AND gate. **(2)**

Symbol



(1)

48.You are given a circuit below. Write its truth table. Hence, identify the logic operation carried out by this circuit. Draw the logic symbol of the gate which corresponds to[All India 2011]



Ans.

$$Z = \overline{\bar{A} + \bar{B}} = \bar{\bar{A}} \cdot \bar{\bar{B}} = AB$$

Truth table of given circuit is as shown below:

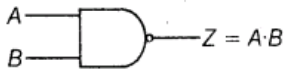
A	B	$X = \bar{A}$	$Y = \bar{B}$	$Z = \overline{X + Y}$
0	0	1	1	0
1	0	0	1	0
0	1	1	0	0
1	1	0	0	1

This circuit carries out by the logic operation of AND gate which can also be verified by De-Morgan's theorem

$$Z = \overline{X + Y} = \overline{\bar{A} + \bar{B}} = \bar{\bar{A}} + \bar{\bar{B}} = A \cdot B$$

So, the circuit corresponds to AND gate. **(2)**

Symbol



(1)

49.Draw transfer characteristics of a common-emitter n-p-n Point out the region in which the transistor operates as an amplifier.

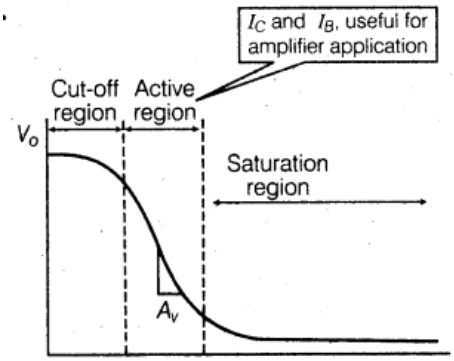
Define the following terms used in transistor amplifiers:

(i)Input resistance

(ii)Output resistance

(iii)Current amplification factor.[Foreign 2011]

Ans.



(*i*) The input resistance, r_i of transistor in *CE* configuration is defined as the ratio of small change in base-emitter voltage to the corresponding small change in the base current, when the collector emitter voltage is kept constant, i.e.

$$r_i = \left(\frac{\Delta V_{EB}}{\Delta I_B}\right)_{V_{CE}\text{ = constant}} \quad \textbf{(1)}$$

(*ii*) **Output resistance** The ratio of variation of collector emitter voltage (V_{CE}) and corresponding change in collector current (ΔI_C) when base current remains constant is called output characteristic curve.

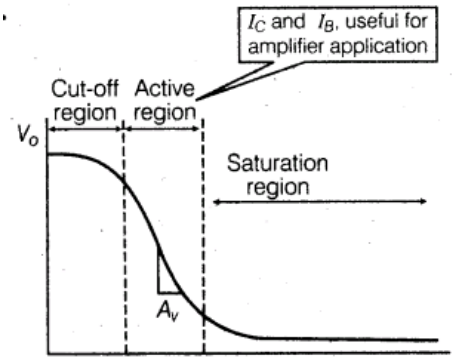
$$\therefore \quad R_{out} = \left(\frac{\Delta V_{CE}}{\Delta I_C}\right)_{I_B\text{ = constant}}$$

(*ii*) The current amplification factor of a transistor in *CE* configuration is equal to the ratio of the small change in the collector current (ΔI_C) to the small change in base current when collector-emitter voltage is kept constant, i.e.

$$\beta = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}\text{ = constant}} \quad \textbf{(1)}$$

50.Draw the general shape of the transfer characteristics of a transistor in its CE Which regions of this characteristic of a transistor are used when it works as an amplifier?[All India 2010 C]

Ans.



(*i*) The input resistance, r_i of transistor in *CE* configuration is defined as the ratio of small change in base-emitter voltage to the corresponding small change in the base current, when the collector emitter voltage is kept constant, i.e.

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(*ii*) The current amplification factor of a transistor in *CE* configuration is equal to the ratio of the small change in the collector current (ΔI_C) to the small change in base current when collector-emitter voltage is kept constant, i.e.

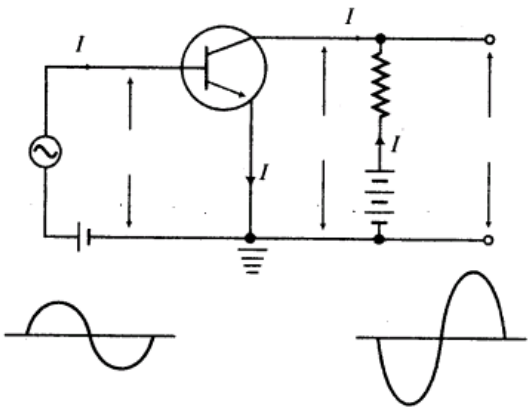
$$\beta = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}\text{ = constant}} \quad \textbf{(1)}$$

51.Give the circuit diagram of a common-emitter amplifier using an n-p-n transistor. Draw the input and output wave forms of the signal. Write the expression for its voltage gain. [HOTS, All India 2010]

Ans.

Whenever *CE* circuit is used as an amplifier the output should be 180° out of phase with the input. The output will also be amplified that is amplitude of output will be more than that of input.

Circuit diagram of a common-emitter amplfier **(1/2)**



Voltage gain It is equal to the ratio of small change in output voltage at the collector to that of change in input voltage, i.e.

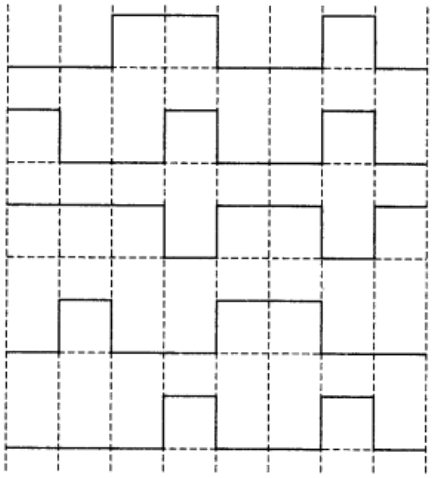
$$A_V = \frac{\text{Output voltage}}{\text{Input voltage}}$$

$$= \frac{\Delta V_{CE}}{\Delta V_{EB}} = \frac{(\Delta I_C) R_{out}}{\Delta I_B R_{in}} = \beta_{AC} \times \frac{R_{out}}{R_{in}} \quad \left(1\frac{1}{2}\right)$$

$$\Rightarrow \text{ Voltage gain} = \beta_{AC} \times \frac{R_{out}}{B_{in}}$$

where, β_{AC} is AC current gain.

52.The inputs A and B shown here are used as the inputs for three different gates G_1, G_2 and G_3. The outputs obtained in the three cases have the forms shown. Identify the three gates and write their truth tables. [All India 2009 c]



Ans.

For G_1

Gate : NAND gate

Truth table

A	B	$G_1 = \overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

For G_2

Gate : NOR gate

Truth table

A	B	$G_2 = \overline{A + B}$
0	0	1
0	1	0
1	0	0
1	1	0

(1/2 × 2 = 1)

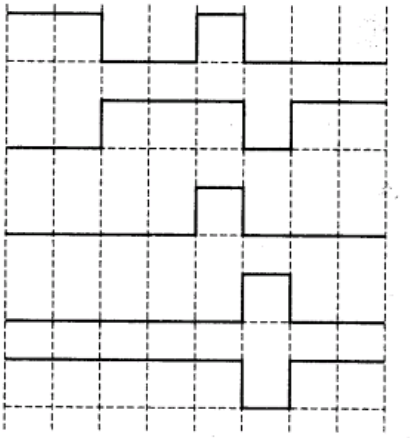
For G_3

Gate : AND gate

Truth table

A	B	$G_3 = A \cdot B$
0	0	0
0	1	0
1	0	0
1	1	1

53.The inputs A and B shown here are used as the inputs for' three different gates G_1, G_2 and G_3 one by one. The outputs obtained in the three cases have the forms shown. Identify the three gates and write their symbols. [All India 2009 C]



Ans.

(*i*) G_1 : AND gate (ii) G_2 : NOR gate

(*iii*) G_3 : OR gate. **(1/2 × 3 = 1½)**

Truth table

A	B	G_1	G_2	G_3
0	0	0	1	0
0	1	0	0	1
1	0	0	0	1
1	1	1	0	1

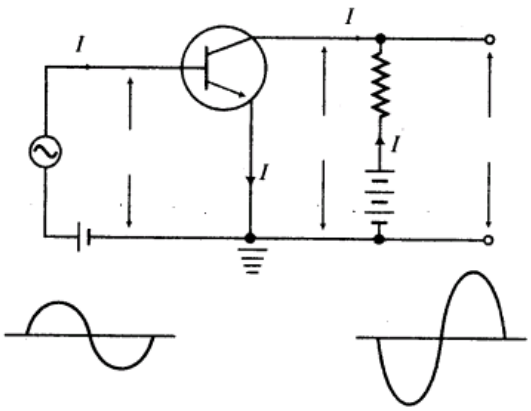
(1½)

54.Draw the labelled circuit diagram of a common-emitter transistor amplifier. Explain clearly, how the input and output signals are in opposite phase?[All India 2009]

Ans.

Whenever CE circuit is used as an amplifier the output should be 180° out of phase with the input. The output will also be amplified that is amplitude of output will be more than that of input.

Circuit diagram of a common-emitter amplfier **(1/2)**



Voltage gain It is equal to the ratio of small change in output voltage at the collector to that of change in input voltage, i.e.

$$A_V = \frac{\text{Output voltage}}{\text{Input voltage}}$$

$$= \frac{\Delta V_{CE}}{\Delta V_{EB}} = \frac{(\Delta I_C) R_{out}}{\Delta I_B R_{in}} = \beta_{AC} \times \frac{R_{out}}{R_{in}} \qquad \left(1\frac{1}{2}\right)$$

$$\Rightarrow \text{ Voltage gain} = \beta_{AC} \times \frac{R_{out}}{B_{in}}$$

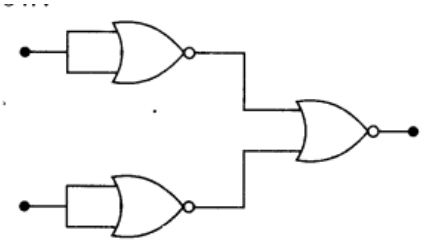
where, β_{AC} is AC current gain.

Relationship between input and output signals of *n*-*p*-*n* transistor amplifier. When positive half cycle is fed into input circuit, forward bias of emitter base circuit decreases. This lead to decrease I_E and by transistor action, collector current decreases.

Since, output voltage, $V_o = V_{CE} - I_C R_L$, therefore, decrease in collector current, increases the output voltage. As, the collector is connected with the negative terminal of battery V_{CC}, the increase in collector voltage imply that negatively of collector increases.

Thus, corresponding to positive half cycle of input AC, a negative amplified cycle is obtained at collector and vice-versa. This shows that output and input signals are in opposite phase

55.The inputs A and B are inverted by using two NOT gates and their outputs are fed to the NOR gate as shown below:
Analyse the action of the gates (1) and (2) and identify the logic gate of the complete circuit so obtained. Give its symbol and the truth table.[All India 2009]



Ans.

The gates 1 and 2 are NOR gates acting as NOT gate.

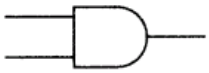
For 1 and 2,

When $A = 0, A = 0, Y = \overline{0 + 0} = \bar{0} = 1$

Similarly, $B = 0, B = 0, Y = \overline{0 + 0} = \bar{0} = 1$ **(1)**

Logic gate of complete circuit AND gate

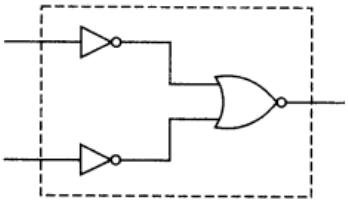
Logic circuit of a AND gate

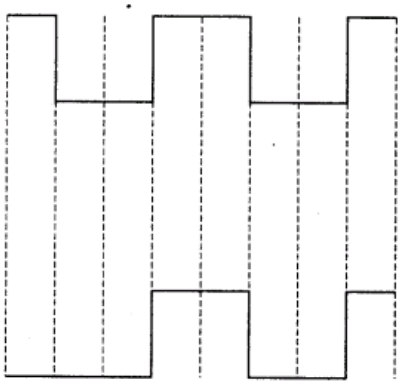


Truth table

A	*B*	*Y = AB*
0	0	0
0	1	0
1	0	0
1	1	1

56.Identify the gate equivalent to the dotted box shown here and give its symbol and truth table The input A shown here is used with another unknown input B in this set up. If the output Y has the form shown, give the intervals over which the input B is in its high state. [Delhi 2008 C]



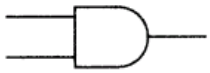


Ans.

$Y = \overline{\bar{A} + \bar{B}} = A \cdot B$

The gate equivalent to dotted box is AND gate. **(1)**

Logic circuit of a AND gate



Truth table

A	*B*	*Y = AB*
0	0	0
0	1	0
1	0	0
1	1	1

B is in high state in the interval 3 to 4, 4 to 5 and **7** to **8.**

5 Marks Questions

57.(i) Differentiate between three segments of a transistor on the basis of their size and level of doping.

(ii)How is a transistor biased to be in active state?

(iii)With the help of necessary circuit diagram, describe briefly, how n-p-n transistor in CE configuration amplifies a small sinusoidal input voltage. Write the expression for the AC current gain. [Delhi 2014]

Ans.(i) The base region of the transistor is physically located between the emitter and the collector region and is made from lightly doped high resistivity material. The emitter and collector regions are heavily doped. But the doping level in emitter is slightly greater than that of collector and the area of collector region is slightly more than that of emitter.

In term of doping level,

Emitter region > collector region > base region

In term of area of the region,

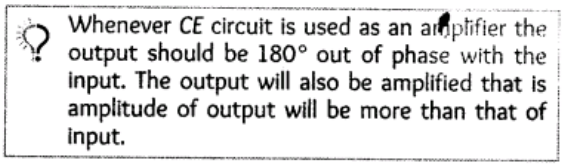
Collector region > emitter region > base region.The area of the collector region is greater than that of emitter. This is because the collector region has to handle more power than the emitter and also it has to collect more number of charge carriers to constituent the current. Emitter is heavily doped to provide large member of majority charge carriers, while base and collector are lightly doped to accept these charge carriers from emitter.

(ii) The conditions of a transistor for to be in active state are below:

(a)The input circuit should be forward biased by using a low voltage battery.

(b)The output circuit should be reverse biased by using a high voltage battery.

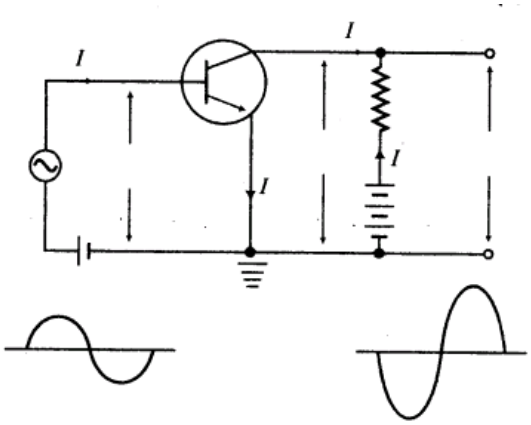
(iii) CE configuration While finding gain for CE configuration we should mind that it will depend upon the load resistance, input resistance as well as output will be inverted.



Whenever *CE* circuit is used as an amplifier the output should be 180° out of phase with the input. The output will also be amplified that is amplitude of output will be more than that of input.

Circuit diagram of a common-emitter amplfier

(1/2)



Voltage gain It is equal to the ratio of small change in output voltage at the collector to that of change in input voltage, i.e.

$$A_V = \frac{\text{Output voltage}}{\text{Input voltage}}$$

$$= \frac{\Delta V_{CE}}{\Delta V_{EB}} = \frac{(\Delta I_C) R_{out}}{\Delta I_B \, R_{in}} = \beta_{AC} \times \frac{R_{out}}{R_{in}} \qquad \left(1\frac{1}{2}\right)$$

$$\Rightarrow \text{ Voltage gain} = \beta_{AC} \times \frac{R_{out}}{B_{in}}$$

where, β_{AC} is AC current gain.

Working In the circuit, emitter is forward biased and collector is reversed biased. This makes input resistance (R_{in}) very low and output resistance (R_{out}) high. During the positive half cycle of input AC decrease the forward bias.

Hence, emitter current, I_E and by transistor action collector current decreases. This tend to increase the collector voltage which is given by

$$V_o = V_{CE} = V_{CC} - I_C R_L$$

The high value of R_L produces large change in V_o corresponding to low change in V_i. Thus, amplified pulse is obtained at collector. **(1)**

Voltage gain It is equal to the ratio of change in output voltage (V_{CE}) corresponding to the change in input voltage (ΔV_{BE}), i.e.

$$\text{Voltage gain } A_V = \frac{\Delta V_{CE}}{\Delta V_{BE}} = \frac{(\Delta I_C) \, R_L}{(\Delta I_B) \, V_i}$$

where, R_L and R_i are output resistances (load resistance) and input resistance of transistor respectively. **(1)**

$$\therefore \qquad A_V = \left(\frac{\Delta I_C}{\Delta I_B}\right) \frac{R_L}{r_i} = \beta_{AC} \frac{R_L}{r_i}$$

where, β_{AC} is AC current gain $= \frac{\Delta I_C}{\Delta I_B}$ **(1/2)**

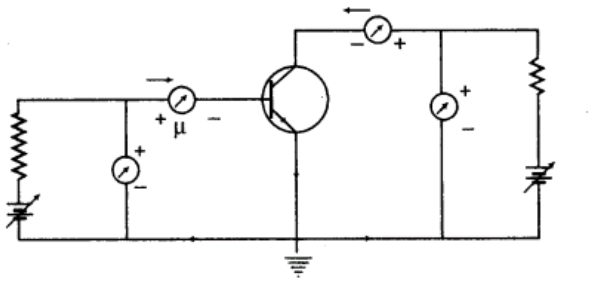
The output voltage of *CE* amplifier differ in phase from the input voltage by 180° or π rad. The opposite phase is represented by negative sign. **(1)**

$$\therefore \quad \text{Voltage gain} = -\beta_{AC} \frac{R_L}{r_i}$$ **(1/2)**

58.(i)Explain briefly with the help of a circuit diagram, how an n-p-n transistor in CE configuration is used to study input and output characteristics.
(ii) Describe briefly the underlying principle of a transistor amplifier working as an oscillator. Hence, use the necessary circuit diagram to explain how self sustained oscillations are achieved in the oscillator. [Delhi 2014 C]

Ans.(i) **Common-emitter Transistor Characteristics**

To study the characteristics of an **n-p-n** transistor in common-emitter mode, required circuit is shown in the figure. Here, base-emitter circuit is forward biased with battery V_{BE} and emitter-collector circuit is reverse biased with battery $\mathbf{V_{cc}}$.



From circuit diagram, we come across to know that it is made up of two sections, i.e. input and output.

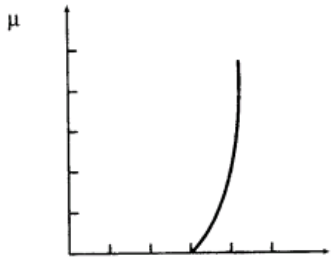
These two characteristics can be studied as shown below:

(a) **Emitter or Input Characteristics**

A graphical relation between the emitter voltage and the emitter current by keeping collector voltage constant is called input characteristics of the transistor.

Adjust collector-emitter voltage at a suitable high value V_{CE} (say = + 10 V). It is necessary so as to make the base-collector junction reverse biased.

Now, with the help of rheostat gradually increases, the value of base-emitter voltage $\mathbf{V_{BE}}$ in small steps and note the corresponding values of base current $\mathbf{I_B}$.



Input resistance It is defined as the ratio of change in base-emitter voltage (ΔV_{BE}) to the resulting change in the base current (ΔI_B) at constant collector-emitter voltage (V_{CE}). It is reciprocal of slope of I_B-V_{BE} curve.

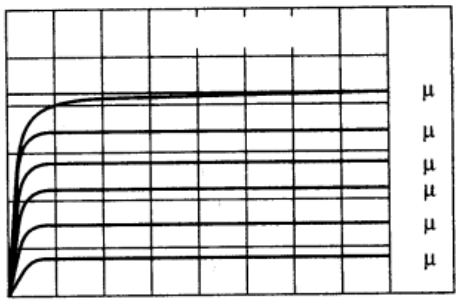
$$\text{Input resistance, } R_i = \left(\frac{\Delta V_{BE}}{\Delta I_B}\right)_{V_{CE} = \text{constant}}$$

(b) Collector or Output Characteristics

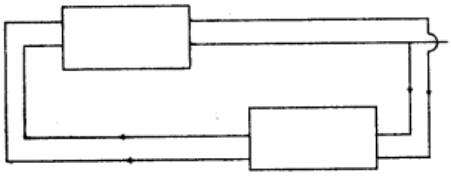
A graphical relation between the collector voltage and collector current by keeping base current constant is called **output characteristics** of the transistor. To study output characteristics of transistor we keep value of base current I_B fixed (say at 10 μA) with the help of V_{BE}. Now, gradually change the value of V_{CE} and note the values of collector current I_C.

Plot I_C V_{CE} graph. Repeat the process for different constant values of I_B.

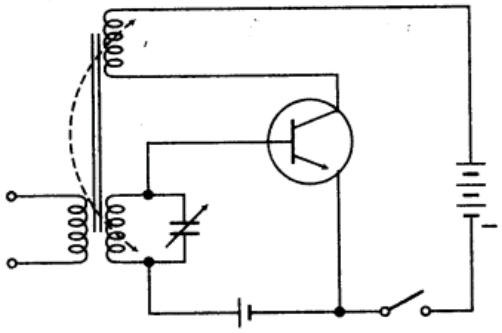
The output characteristics are as shown below:



(ii) **Feedback** When a portion of the output power is returned back to the input in phase this is termed as positive feedback.



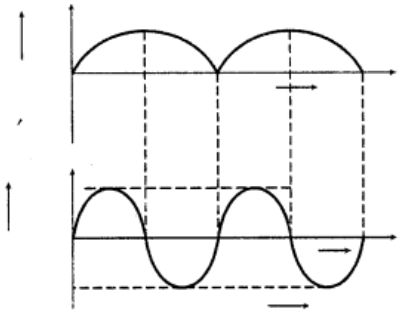
Feedback network The phenomenon of mutual inductance is used to take a part of output in coil **L'** back into input coil **L.** When the switch **K** is closed, collector current begin to flow through **L'**, which in turn increases the magnetic flux linked with **L'** and hence with L This leads to produce an induce emf in **L,** which increases the forward bias. This also increases the base current and hence collector current along with the charging of capacitor takes place with upper plate as positive. This phenomenon is repeated again and again till the collector current reaches to its maximum value.



At maximum value of I_c, current through **L'** does not change and therefore flux remains unchanged and emf in **L'** and **L** reduces to zero. Now, the discharging of capacitor begins through **L.** The positivity of upper plate decreases and forward bias decrease, which results in the form of decrease in base current and hence, decrease in collector current. This phenomenon repeats till collector current reduces to zero and emf in the coil **L** also reduces to zero.

Thus, the time duration in which collector current grows from zero to maximum, the current in coil L of tank circuit complete its half cycle. The duration in which collector current reduces

from maximum to zero, the current in L' completes its next half cycle



The frequency of oscillation is given by

$$\nu = \frac{1}{2\pi\sqrt{LC}}$$

Thus, the AC of desired frequency and amplitude can be obtained by taking appropriate value of inductance,capacitance and strength of battery B

59. (*i*) Draw the circuit diagram of an *n-p-n* transistor with emitter-base junction forward biased and collector-base junction reverse biased. Describe briefly, how the motion of charge carriers in the transistor constitutes the emitter current I_E, the base current I_B and the collector current I_C. Hence, deduce the relation, $I_E = I_B + I_C$.

(*ii*) Explain with the help of a circuit diagram, how a transistor works as an amplifier? **[All India 2014C]**

Ans. (i) In this transistor, the emitter-base junction is forward biased and its resistance is very low. So, the voltage of V_{EE} is quite small.

The collector-base junction is reverse biased. The resistance of this junction is very high. So, the voltage of V_{cc} (V_{CB}) is quite large (= 45 V). Electrons in emitter are repelled towards base by negative potential of V_{EE} on emitter, resulting emitter current I_E. The base being thin and lightly doped has low density of holes, thus when electrons enter the base region, then only a few holes get neutralised by electron hole combination, resulting in base current (I_B). The remaining electrons pass over to the collector, due to high positive potential of collector, resulting in collector current (I_c) . As,' e electron reaches to collector, it gets neutialised by the flow of one electron from the negative terminal of the battery V_{cc} to collector through connecting wire. Then, one electron flow from negative terminal of battery V_{cc} to positive terminal of battery V_{EE} and one electron flow from negative terminal of V_{EE} to emitter.

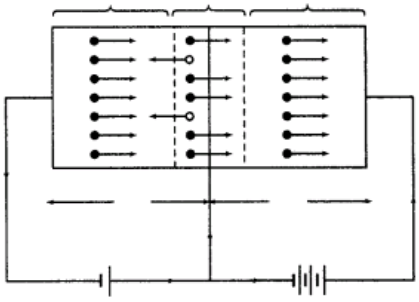
When the electron coming from emitter combines with the holes in base, then deficiency of hole in the base is compensated by the breaking of covalent bond there. The electron, so released flows to the positive terminal of battery V_{EE}, through connecting wire.

Thus, in n-p-n transistor, the current is carried inside as well as in external circuit by the electrons

Thus, in this case also,

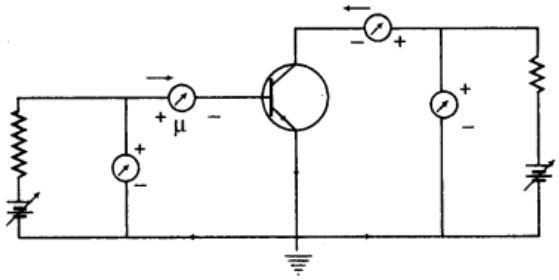
$$I_E = I_B + I_C$$ [Kirchhoff 's first law]

In the base, I_E and I_C flow in opposite direction.



(ii) **Common-emitter Transistor Characteristics**

To study the characteristics of an **n-p-n** transistor in common-emitter mode, required circuit is shown in the figure. Here, base-emitter circuit is forward biased with battery V_{BE} and emitter-collector circuit is reverse biased with battery $\mathbf{V_{cc}}$.



From circuit diagram, we come across to know that it is made up of two sections, i.e. input and output.

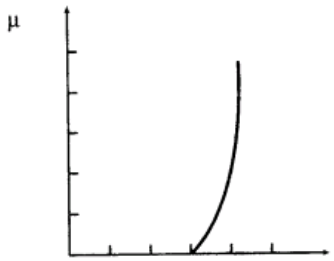
These two characteristics can be studied as shown below:

(a) **Emitter or Input Characteristics**

A graphical relation between the emitter voltage and the emitter current by keeping collector voltage constant is called input characteristics of the transistor.

Adjust collector-emitter voltage at a suitable high value V_{CE} (say = + 10 V). It is necessary so as to make the base-collector junction reverse biased.

Now, with the help of rheostat gradually increases, the value of base-emitter voltage $\mathbf{V_{BE}}$ in small steps and note the corresponding values of base current $\mathbf{I_B}$.



Input resistance It is defined as the ratio of change in base-emitter voltage (ΔV_{BE}) to the resulting change in the base current (ΔI_B) at constant collector-emitter voltage (V_{CE}). It is reciprocal of slope of I_B-V_{BE} curve.

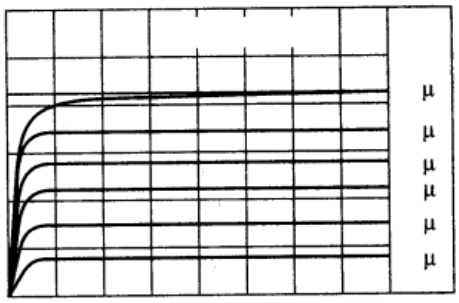
$$\text{Input resistance, } R_i = \left(\frac{\Delta V_{BE}}{\Delta I_B}\right)_{V_{CE} = \text{constant}}$$

(b) Collector or Output Characteristics

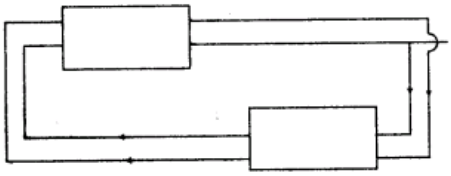
A graphical relation between the collector voltage and collector current by keeping base current constant is called **output characteristics** of the transistor. To study output characteristics of transistor we keep value of base current I_B fixed (say at 10 μA) with the help of V_{BE}. Now, gradually change the value of V_{CE} and note the values of collector current I_C.

Plot I_C V_{CE} graph. Repeat the process for different constant values of I_B.

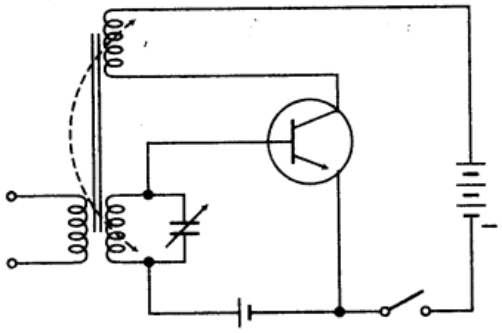
The output characteristics are as shown below:



(c) **Feedback** When a portion of the output power is returned back to the input in phase this is termed as positive feedback.



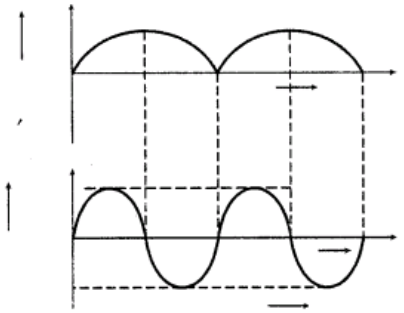
Feedback network The phenomenon of mutual inductance is used to take a part of output in coil **L'** back into input coil **L.** When the switch **K** is closed, collector current begin to flow through**L'**, which in turn increases the magnetic flux linked with **L'** and hence with L This leads to produce an induce emf in **L,** which increases the forward bias. This also increases the base current and hence collector current along with the charging of capacitor takes place with upper plate as positive. This phenomenon is repeated again and again till the collector current reaches to its maximum value.



At maximum value of I_c, current through **L'** does not change and therefore flux remains unchanged and emf in **L'** and **L** reduces to zero. Now, the discharging of capacitor begins through **L.** The positivity of upper plate decreases and forward bias decrease, which results in the form of decrease in base current and hence, decrease in collector current. This phenomenon repeats till collector current reduces to zero and emf in the coil **L** also reduces to zero.

Thus, the time duration in which collector current grows from zero to maximum, the current in coil L of tank circuit complete its half cycle. The duration in which collector current reduces

from maximum to zero, the current in L' completes its next half cycle



The frequency of oscillation is given by

$$\nu = \frac{1}{2\pi\sqrt{LC}}$$

Thus, the AC of desired frequency and amplitude can be obtained by taking appropriate value of inductance,capacitance and strength of battery B

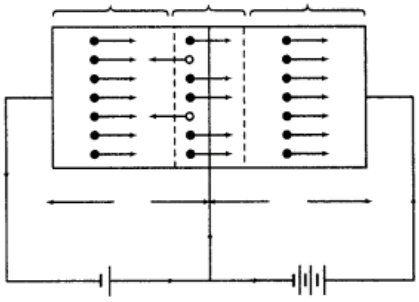
60.(i) Why is the base region of a transistor thin and lightly doped?
(ii) Draw the circuit diagram for studying the characteristics of an n-p-n transistor in common-emitter
configuration.Sketch the typical (a) input and (b) output characteristics in this configuration.
(iii)Describe briefly, how the output characteristics can be used to obtain the current gain in the transistor? [Delhi 2013 C]

Ans.(i) In this transistor, the emitter-base junction is forward biased and its resistance is very low. So, the voltage of V_{EE} is quite small.
The collector-base junction is reverse biased. The resistance of this junction is very high. So, the voltage of V_{cc} (V_{CB}) is quite large (= 45 V). Electrons in emitter are repelled towards base by negative potential of V_{EE} on emitter, resulting emitter current I_E. The base being thin and lightly doped has low density of holes, thus when electrons enter the base region, then only a few holes get neutralised by electron hole combination, resulting in base current (I_B). The remaining electrons pass over to the collector, due to high positive potential of collector, resulting in collector current (I_c) . As,' e electron reaches to collector, it gets neutialised by the flow of one electron from the negative terminal of the battery V_{cc} to collector through connecting wire. Then, one electron flow from negative terminal of battery V_{cc} to positive terminal of battery V_{EE} and one electron flow from negative terminal of V_{EE} to emitter.
When the electron coming from emitter combines with the holes in base, then deficiency of hole in the base is compensated by the breaking of covalent bond there. The electron, so released flows to the positive terminal of battery V_{EE}, through connecting wire.
Thus, in n-p-n transistor, the current is carried inside as well as in external circuit by the electrons

Thus, in this case also,

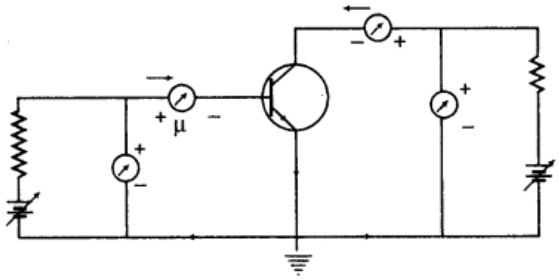
$$I_E = I_B + I_C$$ [Kirchhoff 's first law]

In the base, I_E and I_C flow in opposite direction.



(ii) **Common-emitter Transistor Characteristics**

To study the characteristics of an **n-p-n** transistor in common-emitter mode, required circuit is shown in the figure. Here, base-emitter circuit is forward biased with battery V_{BE} and emitter-collector circuit is reverse biased with battery $\mathbf{V_{cc}}$.



From circuit diagram, we come across to know that it is made up of two sections, i.e. input and output.

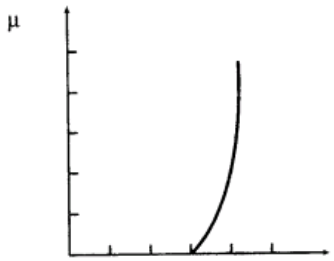
These two characteristics can be studied as shown below:

(a) **Emitter or Input Characteristics**

A graphical relation between the emitter voltage and the emitter current by keeping collector voltage constant is called input characteristics of the transistor.

Adjust collector-emitter voltage at a suitable high value V_{CE} (say = + 10 V). It is necessary so as to make the base-collector junction reverse biased.

Now, with the help of rheostat gradually increases, the value of base-emitter voltage $\mathbf{V_{BE}}$ in small steps and note the corresponding values of base current $\mathbf{I_B}$.



Input resistance It is defined as the ratio of change in base-emitter voltage (ΔV_{BE}) to the resulting change in the base current (ΔI_B) at constant collector-emitter voltage (V_{CE}). It is reciprocal of slope of I_B-V_{BE} curve.

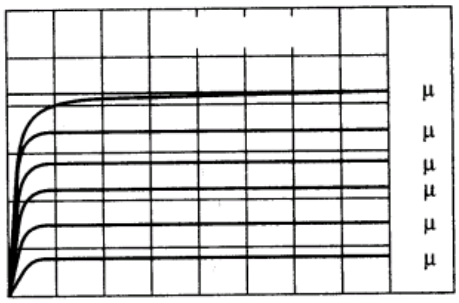
$$\text{Input resistance, } R_i = \left(\frac{\Delta V_{BE}}{\Delta I_B}\right)_{V_{CE} = \text{constant}}$$

(b) Collector or Output Characteristics

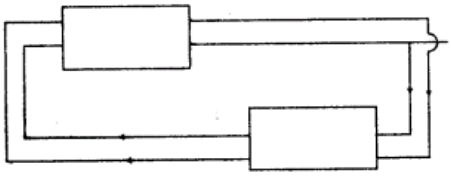
A graphical relation between the collector voltage and collector current by keeping base current constant is called **output characteristics** of the transistor. To study output characteristics of transistor we keep value of base current I_B fixed (say at 10 μA) with the help of V_{BE}. Now, gradually change the value of V_{CE} and note the values of collector current I_C.

Plot I_C V_{CE} graph. Repeat the process for different constant values of I_B.

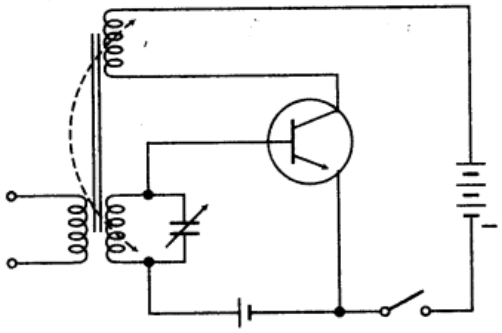
The output characteristics are as shown below:



(c) **Feedback** When a portion of the output power is returned back to the input in phase this is termed as positive feedback.



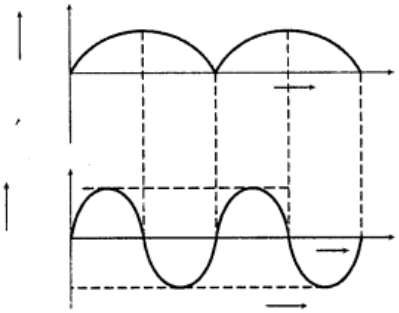
Feedback network The phenomenon of mutual inductance is used to take a part of output in coil **L'** back into input coil **L.** When the switch **K** is closed, collector current begin to flow through **L'**, which in turn increases the magnetic flux linked with **L'** and hence with L This leads to produce an induce emf in **L,** which increases the forward bias. This also increases the base current and hence collector current along with the charging of capacitor takes place with upper plate as positive. This phenomenon is repeated again and again till the collector current reaches to its maximum value.



At maximum value of I_c, current through **L'** does not change and therefore flux remains unchanged and emf in **L'** and **L** reduces to zero. Now, the discharging of capacitor begins through **L.** The positivity of upper plate decreases and forward bias decrease, which results in the form of decrease in base current and hence, decrease in collector current. This phenomenon repeats till collector current reduces to zero and emf in the coil **L** also reduces to zero.

Thus, the time duration in which collector current grows from zero to maximum, the current in coil L of tank circuit complete its half cycle. The duration in which collector current reduces

from maximum to zero, the current in L' completes its next half cycle

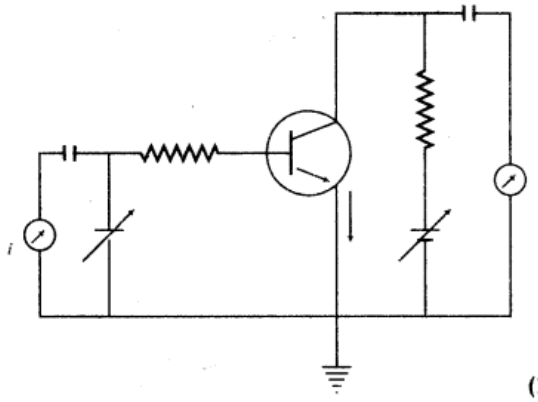


The frequency of oscillation is given by

$$\nu = \frac{1}{2\pi\sqrt{LC}}$$

Thus, the AC of desired frequency and amplitude can be obtained by taking appropriate value of inductance,capacitance and strength of battery B

(iii)**Circuit is as shown below:**

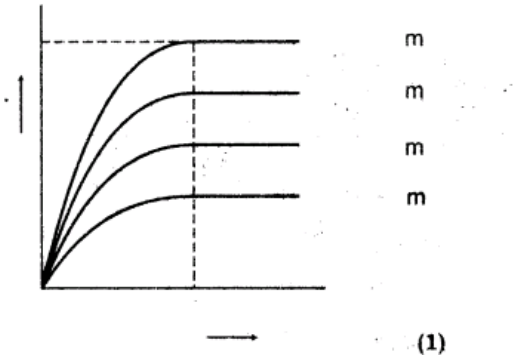


(1)

Current amplification factor (β_{AC}) is the ratio of change in collector current (ΔI_C) to the change is based current (ΔI_B) at constant collector voltage, i.e.

$$\beta_{AC} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}\ =\ \text{constant}} \qquad \textbf{(1)}$$

Output characteristics represent the variation of I_C with V_C, keeping I_B constant.

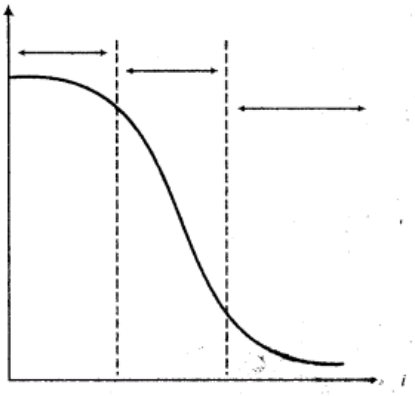


(1)

From above graph at $V_C = V$, the value of collector current increases with the increase in the base current, I_B. Thus,

$$\beta_{AC} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}\ =\ \text{constant}} \qquad \text{[AC current gain]}$$

(*ii*) **Transfer characteristics curve for a base-biased transistor in CE configuration.**



(2)

Hence, low input give high output and high input gives low output.

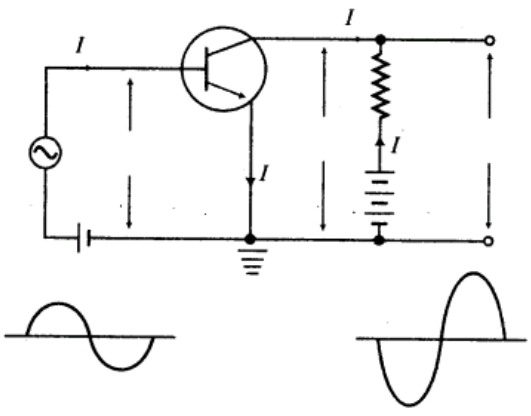
61. Draw a simple circuit of a *CE* transistor amplifier. Explain its working. Show that the voltage gain A_V of the amplifier is given by $A_V = \beta_{AC} R_L / r_i$, where β_{AC} is the current gain, R_L is the load resistance and r_i is the input resistance of the transistor. What is the significance of the negative sign in the expression for the voltage gain. **[HOTS]**

Ans. While finding gain for CE configuration we should mind that it will depend upon the load resistance, input resistance as well as output will be inverted.

Whenever *CE* circuit is used as an amplifier the output should be 180° out of phase with the input. The output will also be amplified that is amplitude of output will be more than that of input.

Circuit diagram of a common-emitter amplfier

(1/2)



Voltage gain It is equal to the ratio of small change in output voltage at the collector to that of change in input voltage, i.e.

$$A_V = \frac{\text{Output voltage}}{\text{Input voltage}}$$

$$= \frac{\Delta V_{CE}}{\Delta V_{EB}} = \frac{(\Delta I_C) R_{out}}{\Delta I_B \, R_{in}} = \beta_{AC} \times \frac{R_{out}}{R_{in}} \qquad \left(1\frac{1}{2}\right)$$

$$\Rightarrow \text{ Voltage gain} = \beta_{AC} \times \frac{R_{out}}{B_{in}}$$

where, β_{AC} is AC current gain.

Working In the circuit, emitter is forward biased and collector is reversed biased. This makes input resistance (R_{in}) very low and output resistance (R_{out}) high. During the positive half cycle of input AC decrease the forward bias.

Hence, emitter current, I_E and by transistor action collector current decreases. This tend to increase the collector voltage which is given by

$$V_o = V_{CE} = V_{CC} - I_C R_L$$

The high value of R_L produces large change in V_o corresponding to low change in V_i. Thus, amplified pulse is obtained at collector. **(1)**

Voltage gain It is equal to the ratio of change in output voltage (V_{CE}) corresponding to the change in input voltage (ΔV_{BE}), i.e.

$$\text{Voltage gain } A_V = \frac{\Delta V_{CE}}{\Delta V_{BE}} = \frac{(\Delta I_C) R_L}{(\Delta I_B) V_i}$$

where, R_L and R_i are output resistances (load resistance) and input resistance of transistor respectively. **(1)**

$$\therefore \qquad A_V = \left(\frac{\Delta I_C}{\Delta I_B}\right) \frac{R_L}{r_i} = \beta_{AC} \frac{R_L}{r_i}$$

where, β_{AC} is AC current gain $= \frac{\Delta I_C}{\Delta I_B}$ **(1/2)**

The output voltage of *CE* amplifier differ in phase from the input voltage by 180° or π rad. The opposite phase is represented by negative sign. **(1)**

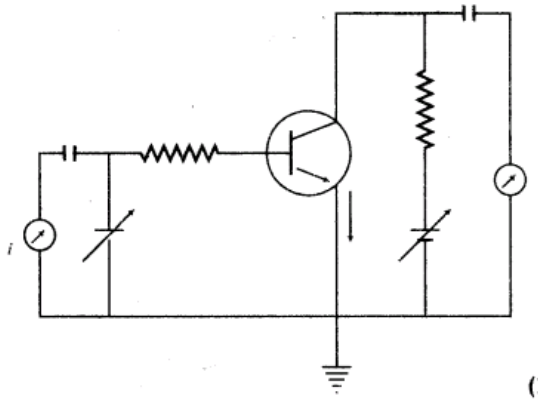
$$\therefore \quad \text{Voltage gain} = -\beta_{AC} \frac{R_L}{r_i}$$ **(1/2)**

62. (*i*) Draw the circuit for studying the input and output characteristics of a transistor in *CE* configuration. Show how from the output characteristics the information about the current amplification factor (β_{AC}) can be obtained.

(*ii*) Draw a plot of the transfer characteristics (V_o *versus* V_i) for a base-biased transistor in *CE* configuration.

[All India 2010; Foreign 2012]

Ans.Circuit is as shown below:

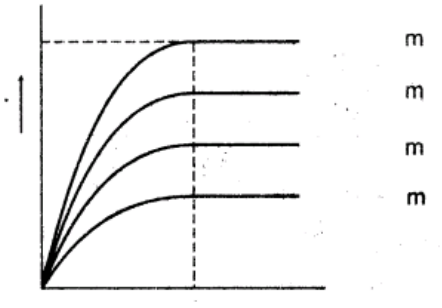


(1)

Current amplification factor (β_{AC}) is the ratio of change in collector current (ΔI_C) to the change is based current (ΔI_B) at constant collector voltage, i.e.

$$\beta_{AC} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}\ =\ \text{constant}} \qquad \textbf{(1)}$$

Output characteristics represent the variation of I_C with V_C, keeping I_B constant.

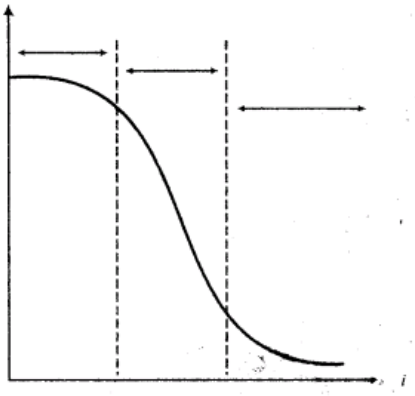


(1)

From above graph at $V_C = V$, the value of collector current increases with the increase in the base current, I_B. Thus,

$$\beta_{AC} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}\ =\ \text{constant}} \qquad \text{[AC current gain]}$$

(*ii*) **Transfer characteristics curve for a base-biased transistor in CE configuration.**

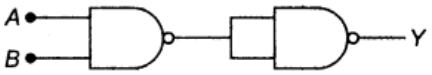


(2)

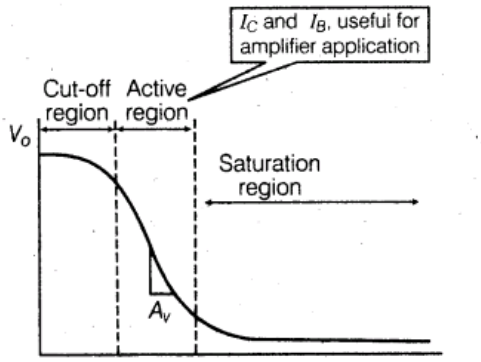
Hence, low input give high output and high input gives low output.

63.(i)Using the necessary circuit diagram, draw the transfer characteristics of a base-biased transistor in CE configuration. With the help of these characteristics, explain briefly how the transistor can be used as an amplifier?

(ii) Why are NAND gate called universal gates? Identify the logical operations carried out by the circuit given as below:



Ans.(i)



(*i*) The input resistance, r_i of transistor in *CE* configuration is defined as the ratio of small change in base-emitter voltage to the corresponding small change in the base current, when the collector emitter voltage is kept constant, i.e.

$$r_i = \left(\frac{\Delta V_{EB}}{\Delta I_B}\right)_{V_{CE}\text{ = constant}}$$ **(1)**

(*ii*) **Output resistance** The ratio of variation of collector emitter voltage (V_{CE}) and corresponding change in collector current (ΔI_C) when base current remains constant is called output characteristic curve.

$$\therefore \quad R_{out} = \left(\frac{\Delta V_{CE}}{\Delta I_C}\right)_{I_B\text{ = constant}}$$

(*ii*) The current amplification factor of a transistor in *CE* configuration is equal to the ratio of the small change in the collector current (ΔI_C) to the small change in base current when collector-emitter voltage is kept constant, i.e.

$$\beta = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}\text{ = constant}} \quad \textbf{(1)}$$

The active region of a transfer characteristics curve can be used to explain the transistor as an amplifier.

The resistance of output circuit is large being in reverse bias and resistance of input circuit is low being in forward bias.

When input voltage, V_{BE} comes in active region, I_C flows in output and V_o varies significantly as

$$V_o = V_{CE} = V_{CC} - I_C R_L$$

This change in output voltage is obtained as amplified form. **(1)**

(*ii*) NAND gates are termed as universal gates because all three basic gates namely AND, OR and NOT can be made using NAND gate. **(1)**

The given circuit perform the logic operations of AND gate as

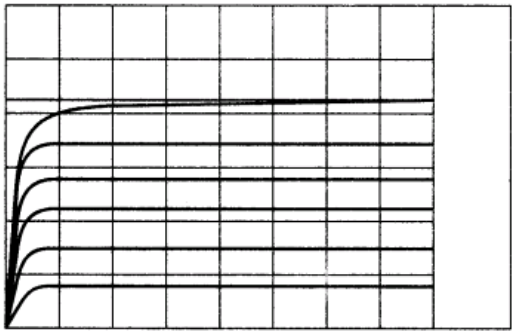
$$Y = \overline{(A \cdot B)} = A \cdot B \quad \textbf{(1)}$$

64. (*i*) Draw the circuit diagram of a base-biased *n*-*p*-*n* transistor in *CE* configuration. Explain, how this circuit is used to obtain the transfer characteristic V_o - V_i characteristic.

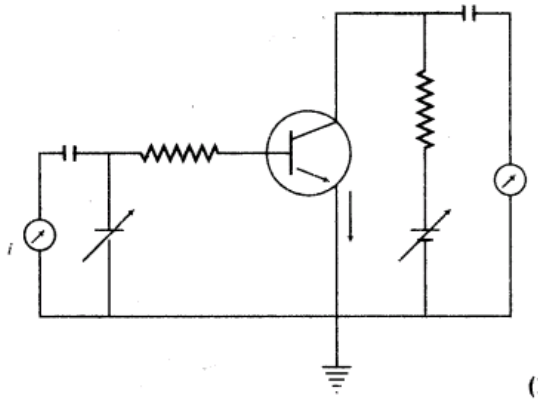
(*ii*) The typical output characteristics I_C *versus* V_{CE} of an *n*-*p*-*n* transistor in *CE* configuration is shown in the figure. Calculate

(*a*) the output resistance r_o and

(*b*) the current amplification factor β_{AC}. **[Foreign 2010]**

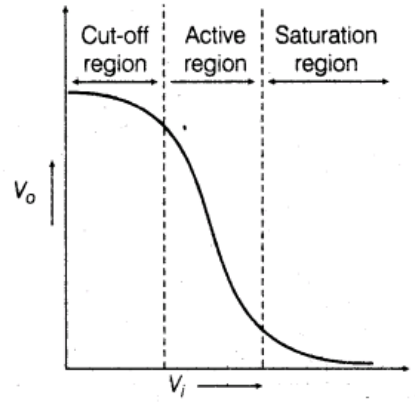


Ans. (i) For n-p-n transistor in CE configuration circuit diagram



(1)

The transfer characteristic curve of base biased transistor in CE configuration as shown below:



(*ii*) (*a*) The output resistance (r_o)

$$= \left(\frac{\Delta V_{CE}}{\Delta I_C}\right)_{I_B = \text{constant}}$$

From the given graph, at $I_B = 60\ \mu A$,

$V_{CE} = 2\ V$, $V_{CE} = 16\ V$

Collector current changes from 8 mA to 8.5 mA,

i.e. $\Delta V_{CE} = 16 - 2 = 14\ V$

$\Delta I_C = 8.5 - 8 = 0.5\ mA = 5 \times 10^{-4}\ A$

$$\therefore \quad r_o = \left(\frac{\Delta V_C}{\Delta I_C}\right)_{I_B = 60\ \mu A} = \frac{14}{5 \times 10^{-4}}$$

$r_o = 2.8 \times 10^4\ \Omega$

$r_o = 28\ k\Omega$ **(1)**

(*b*) The current amplification factor,

$$\therefore \quad \beta_{AC} = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE} = \text{constant}}$$

At $V_{CE} = 2\ V,\ I_B = 10\ \mu A$ to $60\ \mu A$

$\therefore \quad \Delta I_B = (60 - 10) = 50\ \mu A$

I_C changes from 1.5 mA to 8 mA

$\therefore \quad \Delta I_C = 8 - 1.5 = 6.5\ mA$

$$\Rightarrow \beta_{AC} = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}} = \frac{6.5 \times 10^{-3}\ A}{50 \times 10^{-6}\ A}$$

$$\beta_{AC} = \frac{6.5 \times 10^3}{50} = 1.3 \times 10^2$$

$$\Rightarrow \beta_{AC} = 130 \qquad \textbf{(1)}$$

65.(i)Draw the circuit diagram used for studying the input and output characteristics of an n-p-n transistor in the CE configuration. Show the typical shapes of these two characteristics.

(ii) How are the

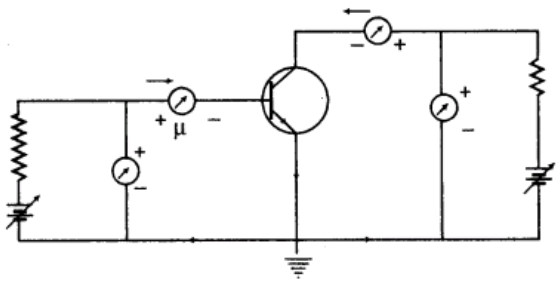
(a)input resistance

(b)current amplification factor of the transistor determined from these characteristics?

[Delhi 2010 C]

Ans.(i) Common-emitter Transistor Characteristics

To study the characteristics of an n-p-n transistor in common-emitter mode, required circuit is shown in the figure. Here, base-emitter circuit is forward biased with battery V_{BE} and emitter-collector circuit is reverse biased with battery V_{cc}.



From circuit diagram, we come across to know that it is made up of two sections, i.e. input and output.

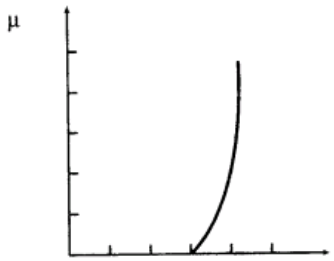
These two characteristics can be studied as shown below:

(a) Emitter or Input Characteristics

A graphical relation between the emitter voltage and the emitter current by keeping collector voltage constant is called input characteristics of the transistor.

Adjust collector-emitter voltage at a suitable high value V_{CE} (say = + 10 V). It is necessary so as to make the base-collector junction reverse biased.

Now, with the help of rheostat gradually increases, the value of base-emitter voltage V_{BE} in small steps and note the corresponding values of base current I_B.



Input resistance It is defined as the ratio of change in base-emitter voltage (ΔV_{BE}) to the resulting change in the base current (ΔI_B) at constant collector-emitter voltage (V_{CE}). It is reciprocal of slope of I_B-V_{BE} curve.

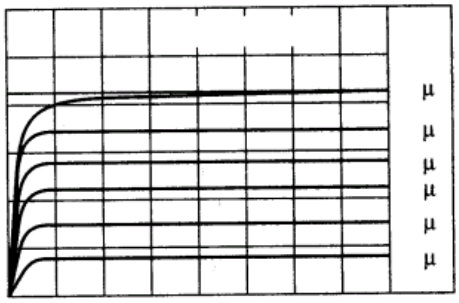
$$\text{Input resistance, } R_i = \left(\frac{\Delta V_{BE}}{\Delta I_B}\right)_{V_{CE} = \text{constant}}$$

(b) Collector or Output Characteristics

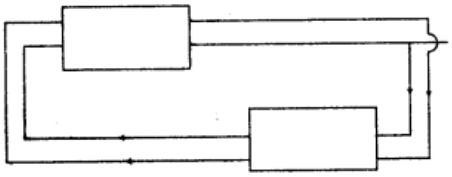
A graphical relation between the collector voltage and collector current by keeping base current constant is called **output characteristics** of the transistor. To study output characteristics of transistor we keep value of base current I_B fixed (say at 10 μA) with the help of V_{BE}. Now, gradually change the value of V_{CE} and note the values of collector current I_C.

Plot I_C V_{CE} graph. Repeat the process for different constant values of I_B.

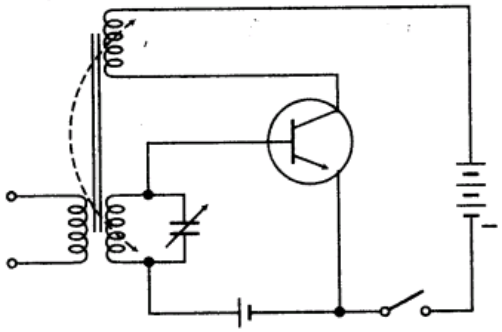
The output characteristics are as shown below:



(ii) Feedback When a portion of the output power is returned back to the input in phase this is termed as positive feedback.



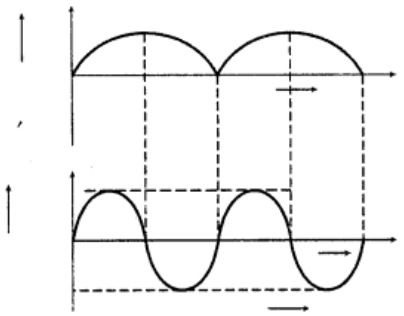
Feedback network The phenomenon of mutual inductance is used to take a part of output in coil L' back into input coil L. When the switch K is closed, collector current begin to flow through //, which in turn increases the magnetic flux linked with L' and hence with L This leads to produce an induce emf in L, which increases the forward bias. This also increases the base current and hence collector current along with the charging of capacitor takes place with upper plate as positive. This phenomenon is repeated again and again till the collector current reaches to its maximum value.



At maximum value of I_c, current through L' does not change and therefore flux remains

unchanged and emf in L' and L reduces to zero. Now, the discharging of capacitor begins through L. The positivity of upper plate decreases and forward bias decrease, which results in the form of decrease in base current and hence, decrease in collector current. This phenomenon repeats till collector current reduces to zero and emf in the coil L also reduces to zero.

Thus, the time duration in which collector current grows from zero to maximum, the current in coil L of tank circuit complete its half cycle. The duration in which collector current reduces from maximum to zero, the current in L' completes its next half cycle



The frequency of oscillation is given by

$$\nu = \frac{1}{2\pi\sqrt{LC}}$$

Thus, the AC of desired frequency and amplitude can be obtained by taking appropriate value of inductance,capacitance and strength of battery B.

(ii)

(*i*) The input resistance, r_i of transistor in *CE* configuration is defined as the ratio of small change in base-emitter voltage to the corresponding small change in the base current, when the collector emitter voltage is kept constant, i.e.

$$r_i = \left(\frac{\Delta V_{EB}}{\Delta I_B}\right)_{V_{CE}\text{ = constant}} \quad \textbf{(1)}$$

(*ii*) The current amplification factor of a transistor in *CE* configuration is equal to the ratio of the small change in the collector current (ΔI_C) to the small change in base current when collector-emitter voltage is kept constant, i.e.

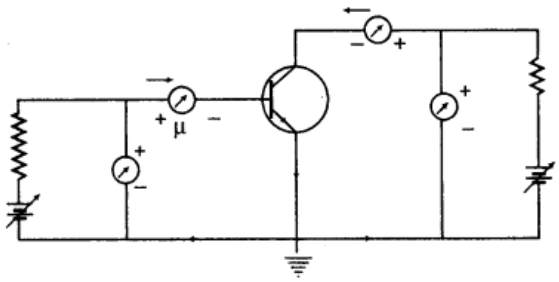
$$\beta = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}\text{ = constant}} \quad \textbf{(1)}$$

66.(i)Draw a circuit diagram to study the input and output characteristics of an n -p- n transistor in its common- emitter configuration. Draw the typical input and output characteristics.

(ii) Explain with the help of a circuit diagram, the working of an n-p-n transistor as a common-emitter amplifier. [Delhi 2009 C]

Ans.(i) Common-emitter Transistor Characteristics

To study the characteristics of an n-p-n transistor in common-emitter mode, required circuit is shown in the figure. Here, base-emitter circuit is forward biased with battery V_{BE} and emitter-collector circuit is reverse biased with battery V_{cc}.



From circuit diagram, we come across to know that it is made up of two sections, i.e. input and output.

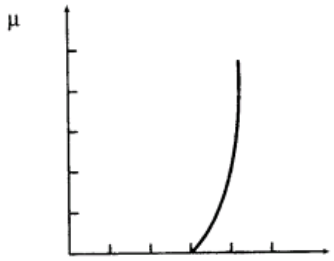
These two characteristics can be studied as shown below:

(a) Emitter or Input Characteristics

A graphical relation between the emitter voltage and the emitter current by keeping collector voltage constant is called input characteristics of the transistor.

Adjust collector-emitter voltage at a suitable high value V_{CE} (say = + 10 V). It is necessary so as to make the base-collector junction reverse biased.

Now, with the help of rheostat gradually increases, the value of base-emitter voltage V_{BE} in small steps and note the corresponding values of base current I_B.



Input resistance It is defined as the ratio of change in base-emitter voltage (ΔV_{BE}) to the resulting change in the base current (ΔI_B) at constant collector-emitter voltage (V_{CE}). It is reciprocal of slope of I_B-V_{BE} curve.

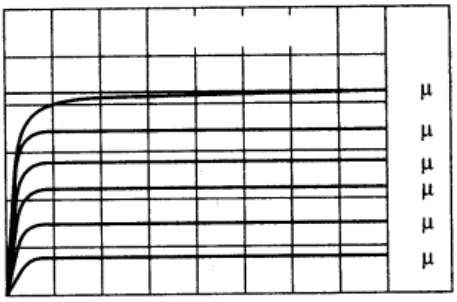
$$\text{Input resistance, } R_i = \left(\frac{\Delta V_{BE}}{\Delta I_B}\right)_{V_{CE} = \text{constant}}$$

(b) Collector or Output Characteristics

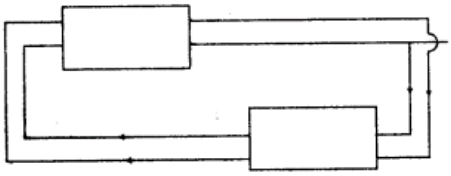
A graphical relation between the collector voltage and collector current by keeping base current constant is called **output characteristics** of the transistor. To study output characteristics of transistor we keep value of base current I_B fixed (say at 10 μA) with the help of V_{BE}. Now, gradually change the value of V_{CE} and note the values of collector current I_C.

Plot I_C V_{CE} graph. Repeat the process for different constant values of I_B.

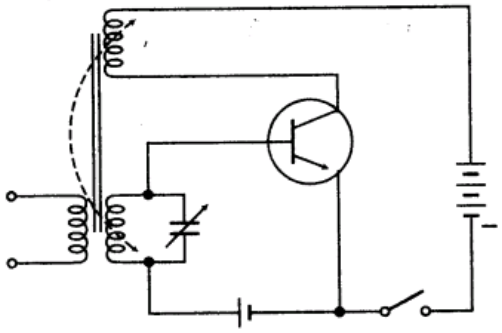
The output characteristics are as shown below:



(ii) Feedback When a portion of the output power is returned back to the input in phase this is termed as positive feedback.

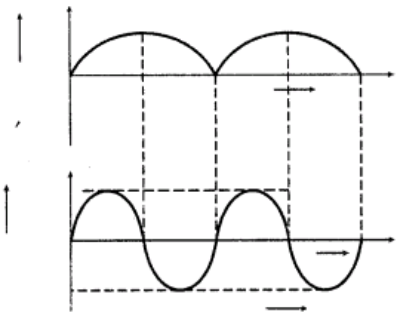


Feedback network The phenomenon of mutual inductance is used to take a part of output in coil L' back into input coil L. When the switch K is closed, collector current begin to flow through //, which in turn increases the magnetic flux linked with L' and hence with L This leads to produce an induce emf in L, which increases the forward bias. This also increases the base current and hence collector current along with the charging of capacitor takes place with upper plate as positive. This phenomenon is repeated again and again till the collector current reaches to its maximum value.



At maximum value of I_C, current through L' does not change and therefore flux remains unchanged and emf in L' and L reduces to zero. Now, the discharging of capacitor begins through L. The positivity of upper plate decreases and forward bias decrease, which results in the form of decrease in base current and hence, decrease in collector current. This phenomenon repeats till collector current reduces to zero and emf in the coil L also reduces to zero.

Thus, the time duration in which collector current grows from zero to maximum, the current in coil L of tank circuit complete its half cycle. The duration in which collector current reduces from maximum to zero, the current in L' completes its next half cycle



The frequency of oscillation is given by

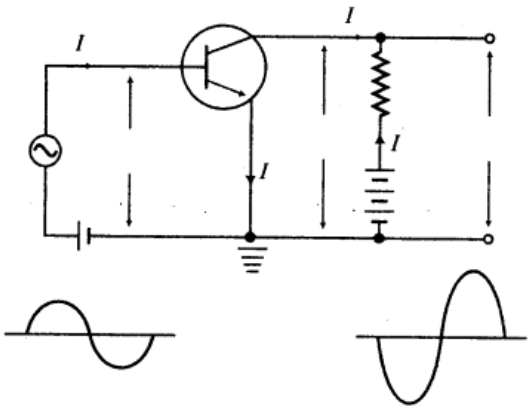
$$\nu = \frac{1}{2\pi\sqrt{LC}}$$

Thus, the AC of desired frequency and amplitude can be obtained by taking appropriate value of inductance,capacitance and strength of battery B.

(ii)

> Whenever *CE* circuit is used as an amplifier the output should be 180° out of phase with the input. The output will also be amplified that is amplitude of output will be more than that of input.

Circuit diagram of a common-emitter amplfier **(1/2)**



Voltage gain It is equal to the ratio of small change in output voltage at the collector to that of change in input voltage, i.e.

$$A_V = \frac{\text{Output voltage}}{\text{Input voltage}}$$

$$= \frac{\Delta V_{CE}}{\Delta V_{EB}} = \frac{(\Delta I_C)R_{out}}{\Delta I_B R_{in}} = \beta_{AC} \times \frac{R_{out}}{R_{in}} \qquad \left(1\frac{1}{2}\right)$$

$$\Rightarrow \text{ Voltage gain} = \beta_{AC} \times \frac{R_{out}}{B_{in}}$$

where, β_{AC} is AC current gain.

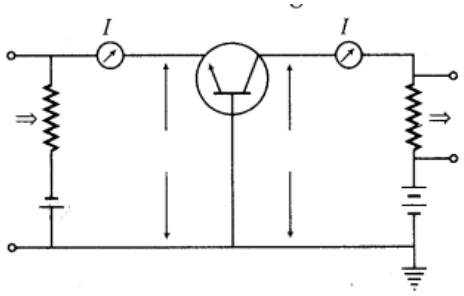
Working of *n-p-n* transistor as *CE* amplifier In the circuit, output resistance is very high whereas input resistance is very low being reverse and forward bias, respectively.

When current, I_C grows in output circuit, potential difference across the collector decreases significantly as per relation

$$V_o = V_{CE} = V_{CC} - I_C R_L$$

When input voltage is fed into input circuit, V_{EB} changes, which in turn change I_B and I_E. By transistor action, I_C change and thus, output voltage changes in amplified manner. **(1)**

67.Draw a circuit diagram of an n-p-n transistor with its emitter base junction forward biased and base- collector junction reverse biased. Describe briefly its working.
Explain, how a transistor in active state exhibits a low resistance at its emitter-base junction and high resistance at its base-collector junction? [Foreign 2009]
Ans. n-p-n transistor in CB configuration
Since, the base is common in input and output circuits, therefore transistor is connected in CB configuration.



(2½)

Working When input voltage, V_{BE} is sufficient to make flow of emitter current, collector current flows in output circuit. In this condition, the circuit is said to be in active state.
The small change in V_{EB}, produces sufficient change in emitter current and hence, in collector current. The input circuit offers very small resistance as ample change in emitter current occurs corresponding to small change in input voltage.
This lead to produce large change in output voltage inspite of smaller change in collector current ($I_E < I_c$). This shows that output circuit offer high resistance

68.Draw a labelled circuit diagram of a base-biased transistor in common-emitter configuration. Plot the transfer characteristics of this base biased transistor indicating the different regions of its operation.[Delhi 2009 c]
Ans.

(*ii*) (*a*) The output resistance (r_o)

$$= \left(\frac{\Delta V_{CE}}{\Delta I_C}\right)_{I_B = \text{constant}}$$

From the given graph, at $I_B = 60\ \mu A$,

$V_{CE} = 2\ V$, $V_{CE} = 16\ V$

Collector current changes from 8 mA to 8.5 mA,

i.e. $\Delta V_{CE} = 16 - 2 = 14\ V$

$\Delta I_C = 8.5 - 8 = 0.5\ mA = 5 \times 10^{-4}\ A$

$$\therefore \quad r_o = \left(\frac{\Delta V_C}{\Delta I_C}\right)_{I_B = 60\ \mu A} = \frac{14}{5 \times 10^{-4}}$$

$$r_o = 2.8 \times 10^4\ \Omega$$

$$r_o = 28\ k\Omega \qquad \textbf{(1)}$$

(*b*) The current amplification factor,

$$\therefore \quad \beta_{AC} = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE} = \text{constant}}$$

At $V_{CE} = 2\ V$, $I_B = 10\ \mu A$ to $60\ \mu A$

$\therefore \quad \Delta I_B = (60 - 10) = 50\ \mu A$

I_C changes from 1.5 mA to 8 mA

$\therefore \quad \Delta I_C = 8 - 1.5 = 6.5\ mA$

$$\Rightarrow \quad \beta_{AC} = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}} = \frac{6.5 \times 10^{-3}\ A}{50 \times 10^{-6}\ A}$$

$$\beta_{AC} = \frac{6.5 \times 10^3}{50} = 1.3 \times 10^2$$

$$\Rightarrow \quad \beta_{AC} = 130 \qquad \textbf{(1)}$$

69. (*i*) Draw the circuit arrangement needed for studying the input and output characteristics of an *n-p-n* transistor in its common- emitter configuration. Draw the typical shape of these input and output characteristics. Why is it, that it is usually enough to determine only one input characteristic?

(*ii*) The small signal current gain β_{AC} of a transistor can be taken as nearly equal to its DC current amplification factor β_{AC}. Why?

[All India 2008C]

Ans.(i)

The active region of a transfer characteristics curve can be used to explain the transistor as an amplifier.

The resistance of output circuit is large being in reverse bias and resistance of input circuit is low being in forward bias.

When input voltage, V_{BE} comes in active region, I_C flows in output and V_o varies significantly as

$$V_o = V_{CE} = V_{CC} - I_C R_L$$

This change in output voltage is obtained as amplified form. **(1)**

(*ii*) NAND gates are termed as universal gates because all three basic gates namely AND, OR and NOT can be made using NAND gate. **(1)**

The given circuit perform the logic operations of AND gate as

$$Y = \overline{\overline{(A \cdot B)}} = A \cdot B \quad \textbf{(1)}$$

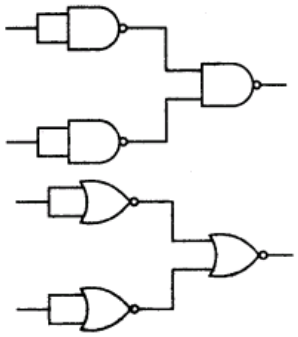
(*ii*) The AC current gain is equal to the ratio of change of collector current to the corresponding change in base current at given collector emitter voltage, i.e.

$$\beta_{AC} = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE} = \text{constant}}$$

and $\beta_{DC} = \left(\frac{I_C}{I_B}\right)_{V_{CE} = \text{constant}}$ **(1)**

Therefore, β_{AC} is nearly equal to β_{DC}. **(1)**

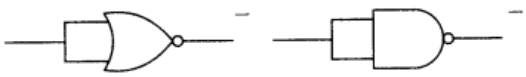
70.(i) The same input -a! is applied to both the (input) terminals of a given logic gate. If the output is(a)same as the (common) input signal.
(b)inverted with respect to the (common) input signal.
Identify the logic gates involved in each case.
(ii) Write the truth tables for each of the combinations shown below. Also identify the logic operations performed by them. [All India 2008 C]



Ans.

(*i*) (a) The logic gate involved may be OR or AND gate as for,
$A = B = 0$ or $A = B = 1$ **(1/2)**
$Y = D$ or 1 is OR and AND gate

(*ii*) The logic gate involved, may be NOR or NAND gates.



(1)

(*ii*) (a) The logic operation performed by the combination of gates is of OR gate

$$Y = \overline{\overline{A} \cdot \overline{B}} = A + B \quad \textbf{(1)}$$

Truth table

A	B	$Y = A + B$
0	0	0
0	1	1
1	0	1
1	1	1

(1/2)

(*b*) The logic operation performed by the combination of gates is of AND gate

$$Y = \overline{\overline{A} + \overline{B}} = A \cdot B$$ **(1/2)**

Truth table

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1