# Short Answer Questions – II (PYQ)

Q. 1. What are energy bands? Write any two distinguishing features between conductors, semiconductors and insulators on the basis of energy band diagrams.
[CBSE (AI) 2014, North 2016]

OR

Draw the necessary energy band diagrams to distinguish between conductors, semiconductors and insulators. How does the change in temperature affect the behaviour of these materials? Explain briefly.   [CBSE Patna 2015]

Ans. Energy Bands: In a solid, the energy of electrons lie within certain range. The energy levels of allowed energy are in the form of bands, these bands are separated by regions of forbidden energy called band gaps.
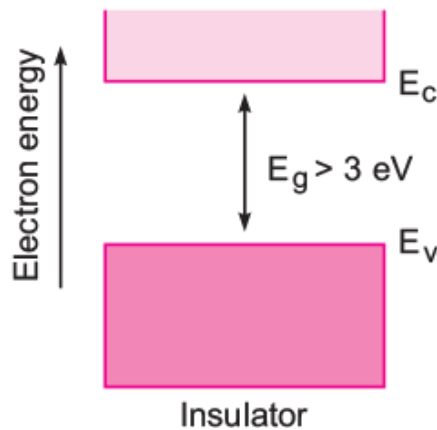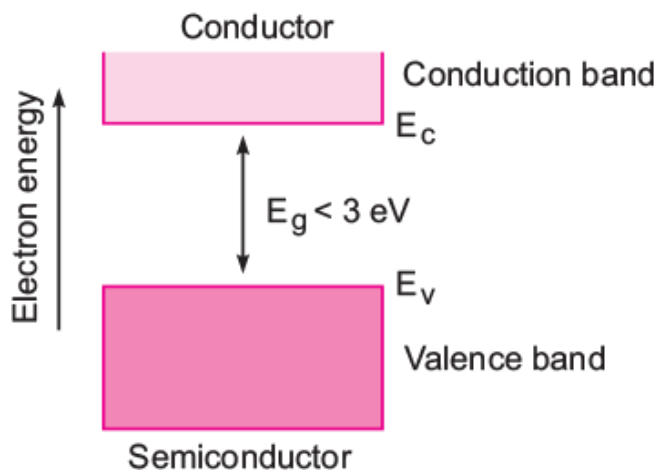
Distinguishing features:

(a) In conductors: Valence band and conduction band overlap each other.

In semiconductors: Valence band and conduction band are separated by a small energy gap.

In insulators: They are separated by a large energy gap.

(b) In conductors: Large number of free electrons are available in conduction band.

In semiconductors: A very small number of electrons are available for electrical conduction.

In insulators: Conduction band is almost empty i.e., no electron is available for conduction.

Effect of Temperature:

(i) In conductors: At high temperature, the collision of electrons become more frequent with the atoms/molecules at lattice site in the metals as a result the conductivity decreases (or resistivity increases).

(ii) In semiconductors: As the temperature of the semiconducting material increases, more electron hole pairs becomes available in the conduction band and valance band, and hence the conductivity increases or the resistivity decreases.

(iii) In insulators: The energy band between conduction band and valance band is very large, so it is unsurpassable for small temperature rise. So, there is no change in their behaviour.

**Q. 2. Distinguish between 'intrinsic' and 'extrinsic' semiconductors.
[CBSE Delhi 2015, (F) 2017]**

Ans.

|	**Intrinsic semiconductor**	**Extrinsic semiconductor**
(i)	It is a semiconductor in pure form.	It is a semiconductor doped with trivalent or pentavalent impurity atoms.
(ii)	Intrinsic charge carriers are electrons and holes with equal concentration.	The two concentrations are unequal in it. There is excess of electrons in n-type and excess of holes in p-type semiconductors.
(iii)	Current due to charge carriers is feeble (of the order of μ A).	Current due to charge carriers is significant (of the order of mA).

Q. 3. Distinguish between an intrinsic semiconductor and a p-type semiconductor. Give reason why a p-type semiconductor crystal is electrically neutral, although nh >> ne.   [CBSE (F) 2013]

Ans.

	Intrinsic semiconductor	Extrinsic semiconductor
(i)	It is a semiconductor in pure form.	It is a semiconductor doped with p-type (like Al, In) impurity.
(ii)	Intrinsic charge carriers are electrons and holes with equal concentration.	Majority charge carriers are holes and minority charge carriers are electrons.
(iii)	Current due to charge carriers is feeble (of the order of μ A).	Current due to charge carriers is significant (of the order of mA).

p-type semiconductor is electrically neutral because every atom, whether it is of pure semiconductor (Ge or Si) or of impurity (Al) is electrically neutral.

Q. 4. Name the important process that occurs during the formation of a p-n junction. Explain briefly, with the help of a suitable diagram, how a p-n junction is formed. Define the term 'barrier potential'.   [CBSE (F) 2011, Central 2016]

Depletion region
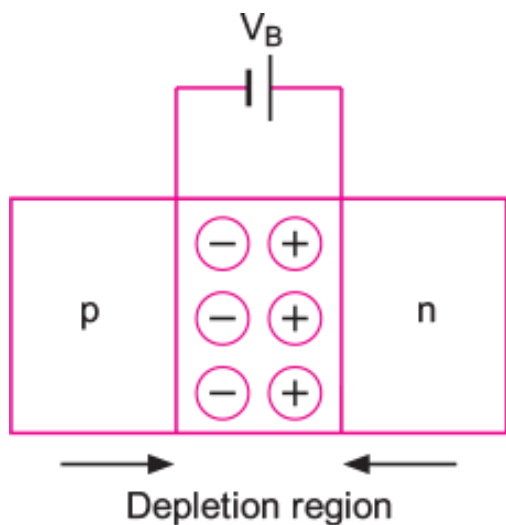
Ans. Potential barrier: During the formation of a p-n junction the electrons diffuse from n-region to p-region and holes diffuse from p-region to n-region. This forms recombination of charge carriers. In this process immobile positive ions are collected at a junction toward n-region and negative ions at a junction toward p-region. This causes a potential difference across the unbiased junction. This is called potential barrier.

Depletion region: It is a layer formed near the junction which is devoid of free charge carriers. Its thickness is about 1 μm.

Q. 5. Explain, with the help of a circuit diagram, the working of a photo-diode. Write briefly how it is used to detect the optical signals. [CBSE Delhi 2013]

OR

(a) How is photodiode fabricated?

(b) Briefly explain its working. Draw its V–I characteristics for two different intensities of illumination.   **[CBSE (F) 2014]**

OR

With what considerations in view, a photodiode is fabricated? State its working with the help of a suitable diagram.

Even though the current in the forward bias is known to be more than in the reverse bias, yet the photodiode works in reverse bias. What is the reason? [CBSE Delhi 2015, East 2016]

Ans. A photo-diode is fabricated using photosensitive Semiconducting material with a transparent window to allow light to fall on the junction of the diode.
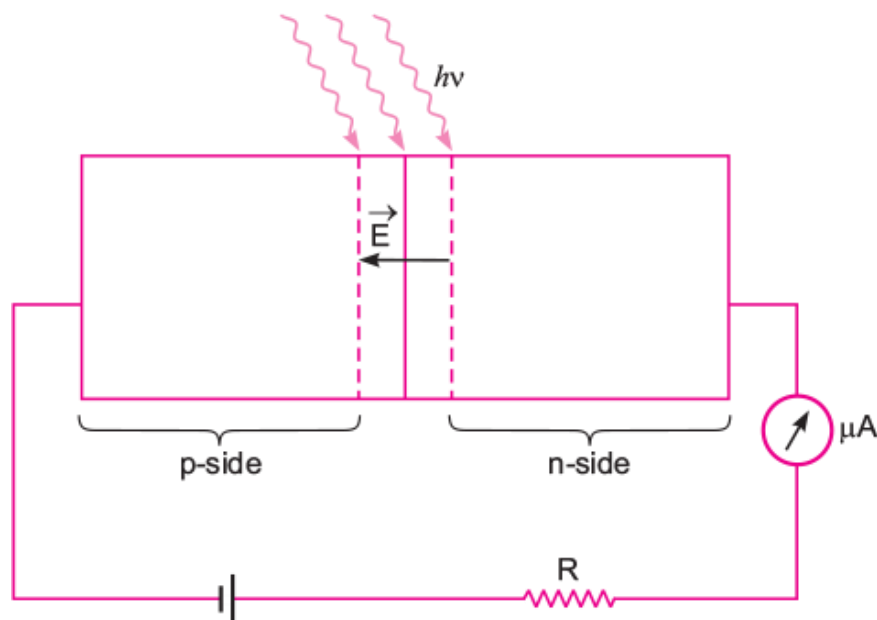
Working: In diode (any type of diode), an electric field 'E' exists across the junction from *n*-side to *p*-side, when light with energy hv greater than energy gap E_g ($h_v > E_g$) illuminates the junction, then electron- hole pairs are generated due to absorption of photons, in or near the depletion region of the diode. Due to existing electric field, electrons and holes get separated. The free electrons are collected on *n*-side and holes are collected on *p*-side, giving rise to an emf.

Due to the generated emf, an electric current of μ*A* order flows through the external resistance.
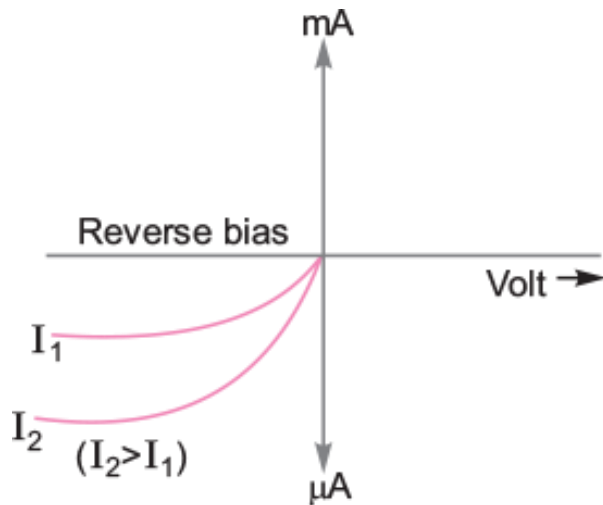
Detection of Optical Signals:

It is easier to observe the change in the current with change in the light intensity if a reverse bias is applied. Thus, photodiode can be used as a photodetector to detect optical signals.

The characteristic curves of a photodiode for two different illuminations I_1 and I_2 ($I_2 > I_1$) are shown.

Q. 6. Explain how the width of depletion layer in a p-n junction diode changes when the junction is (i) forward biased (ii) reverse biased. **[CBSE (AI) 2009]**

Ans. (i) Under forward biasing the applied potential difference causes a field which acts opposite to the potential barrier. This results in reducing the potential barrier, and hence the width of depletion layer decreases.


Forward current
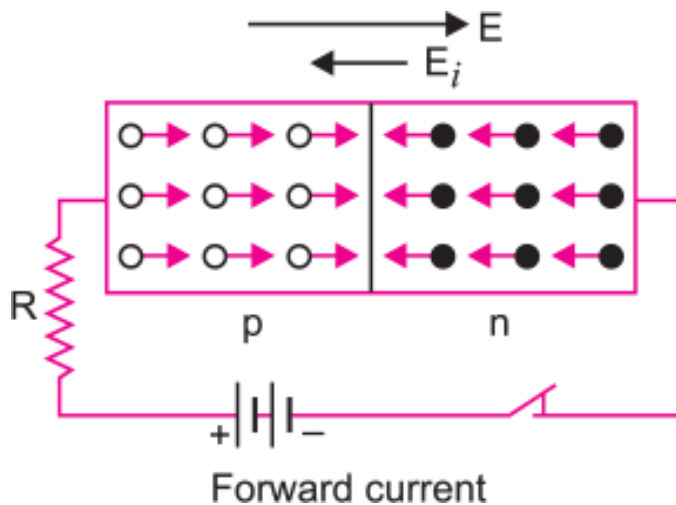
(ii) Under reverse biasing the applied potential difference causes a field which is in the same direction as the field due to internal potential barrier. This results in an increase in barrier voltage and hence the width of depletion layer increases.

Reverse current
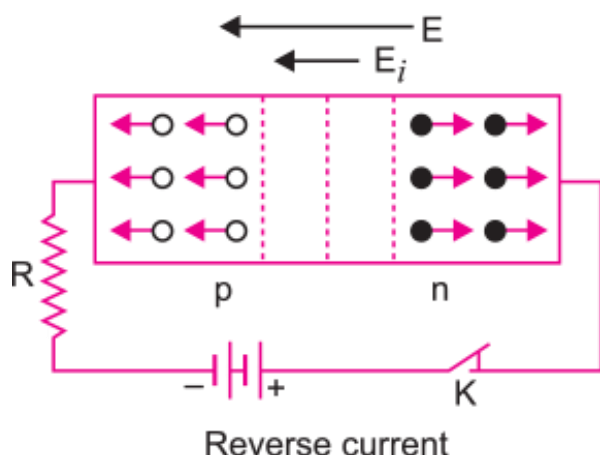
Q. 7. Describe briefly, with the help of a diagram, the role of the two important processes involved in the formation of a p-n junction. [CBSE (AI) 2012, Bhubaneshwar 2015]

Ans. Two important processes occurring during the formation of a p-n junction are (i) diffusion and (ii) drift.

(i) Diffusion: In n-type semiconductor, the concentration of electrons is much greater as compared to concentration of holes; while in p-type semiconductor, the concentration of holes is much greater than the concentration of electrons. When a p-n junction is formed, then due to concentration gradient, the holes diffuse from p-side to n-side (p → n) and electrons diffuse from n-side to p-side (n → p). This motion of charge carriers gives rise to diffusion current across the junction.
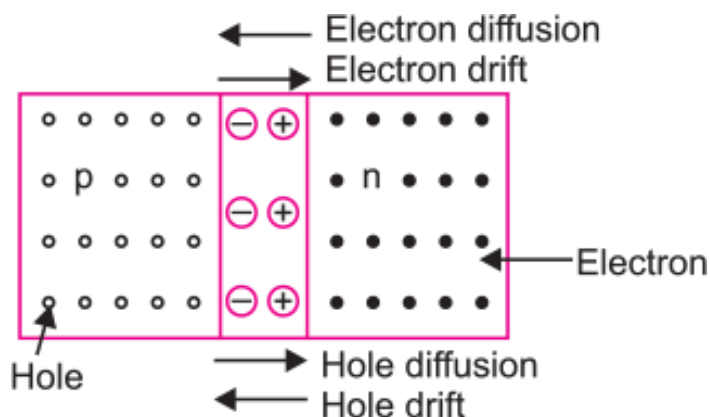
(ii) Drift: The drift of charge carriers occurs due to electric field. Due to built in potential barrier, an electric field directed from n-region to p-region is developed across the junction. This field causes motion of electrons on p-side of the junction to n-side and

motion of holes on n-side of junction to p-side. Thus a drift current starts. This current is opposite to the direction of diffusion current.
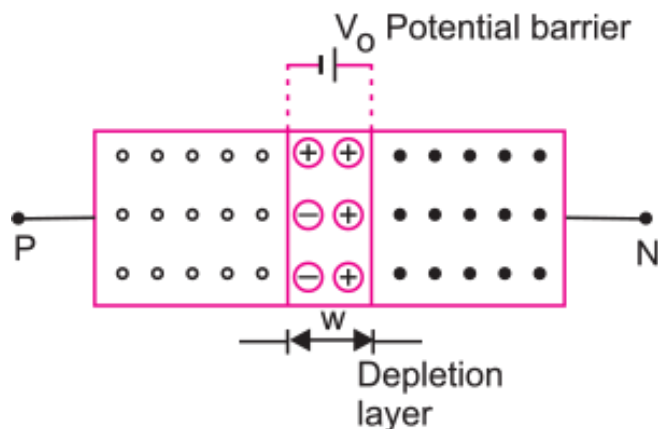
Q. 8. How is a light emitting diode fabricated? Briefly state its working. Write any two important advantages of LEDs over the conventional incandescent low power lamps.
[CBSE Bhubaneshwar 2015]

OR

(a) Explain briefly the process of emission of light by a Light Emitting Diode (LED).

(b) Which semiconductors are preferred to make LEDs and why?

(c) Give two advantages of using LEDs over conventional incandescent lamps.
[CBSE South 2016]

Ans. LED is fabricated by

(i) Heavy doping of both the *p* and *n* regions.

(ii) Providing a transparent cover so that light can come out.

Working: When the diode is forward biased, electrons are sent from $n \to p$ and holes from $p \to n$. At the junction boundary, the excess minority carriers on either side of junction recombine with majority carriers. This releases energy in the form of photon $hv = E_g$.

GaAs (Gallium Arsenide): Band gap of semiconductors used to manufacture LED's should be 1.8 eV to 3eV. These materials have band gap which is suitable to produce desired visible light wavelengths.

Advantages

(i) Low operational voltage and less power consumption.

(ii) Fast action and no warm-up time required.

(iii) Long life and ruggedness.

(iv) Fast on-off switching capability.

Q. 9. Describe briefly using the necessary circuit diagram, the three basic processes which take place to generate the emf in a solar cell when light falls on it. Draw the I – V characteristics of a solar cell. Write two important criteria required for the selection of a material for solar cell fabrication. [CBSE Guwahati 2015]

OR

(i) Describe the working principle of a solar cell. Mention three basic processes involved in the generation of emf.

(ii) Why are Si and GaAs preferred materials for solar cells? [CBSE (F) 2016]

Ans. Principle: It is based on photovoltaic effect (generation of voltage due to bombardment of light photons). When solar cell is illuminated with light photons of energy (hv) greater than the energy gap (E_g) of the semiconductor, then electron-hole pairs are generated due to absorption of photons.
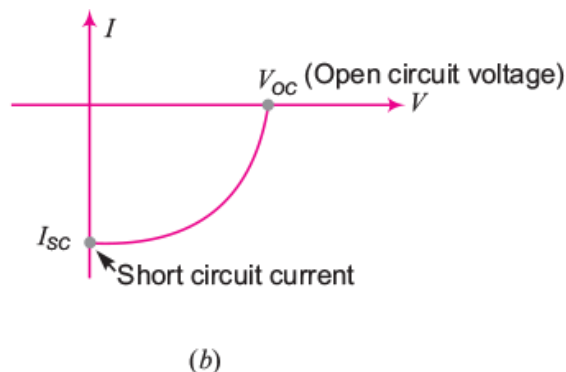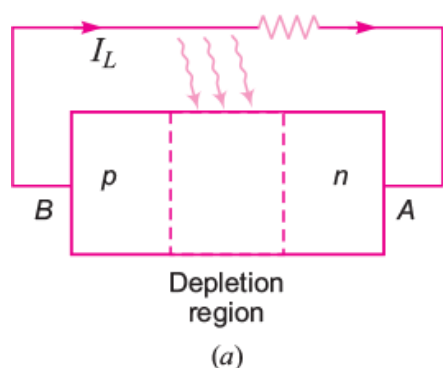
The three basic processes involved are: generation, separation and collection

    a. generation of electron-hole pairs due to light (with $h_v > E_g$) close to the junction
    b. Separation of electrons and holes due to electric field of the depletion region. Electrons are swept to *n*-side and holes to *p*-side
    c. the electrons reaching the *n*-side are collected by the front contact and holes reaching *p*-side are collected by the back contact. Thus, *p*-side becomes positive and *n*-side becomes negative giving rise to photo voltage.

Important criteria for the selection of a material for solar cell fabrication are:

i. band gap (~1.0 to 1.8 eV),
ii. high optical absorption (-10^4 cm^{-1}),
iii. electrical conductivity,
iv. availability of the raw material, and
v. cost

Solar radiation has maximum intensity of photons of energy = 1.5 eV

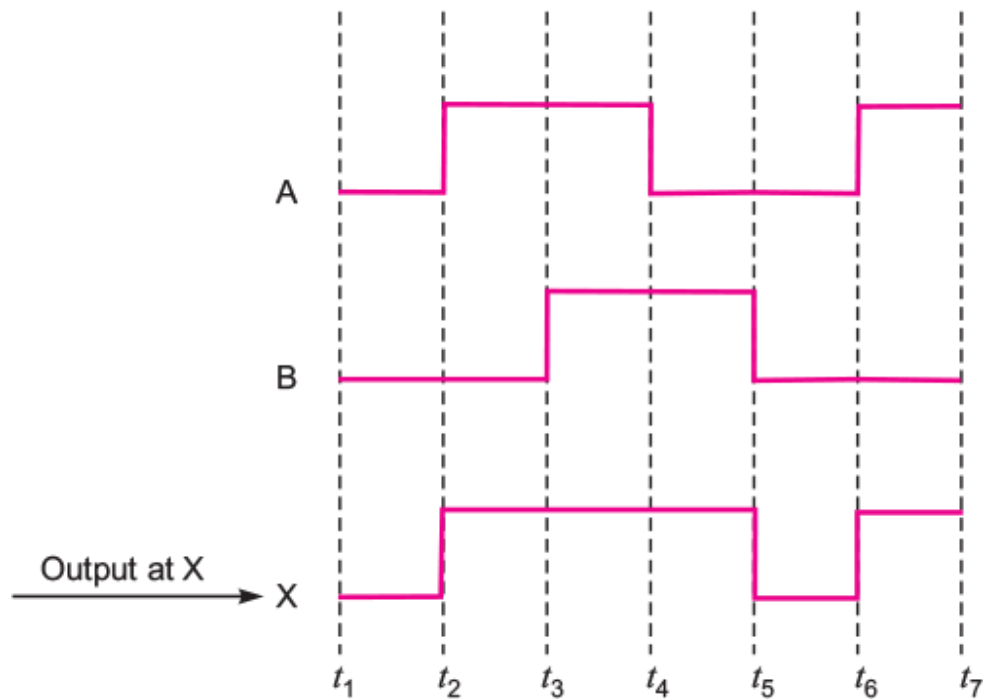Hence semiconducting materials Si and GaAs, with band gap ≈ 1.5 eV, are preferred materials for solar cells.

Q. 10. Draw the output waveform at X, using the given inputs A and B for the logic circuit shown below. Also, identify the logic operation performed by this circuit. [CBSE Delhi 2011]
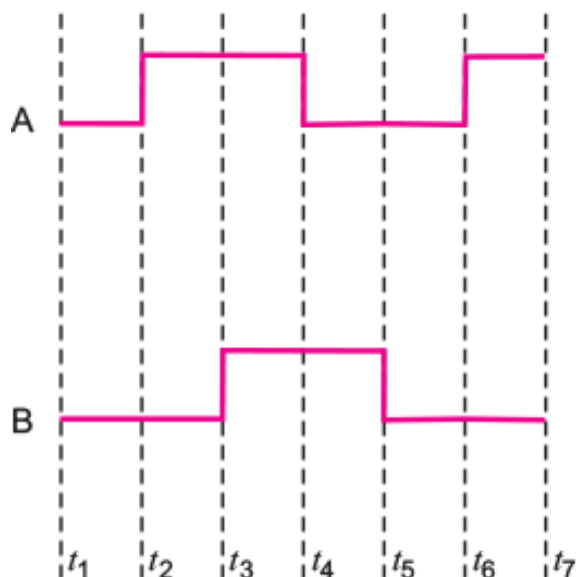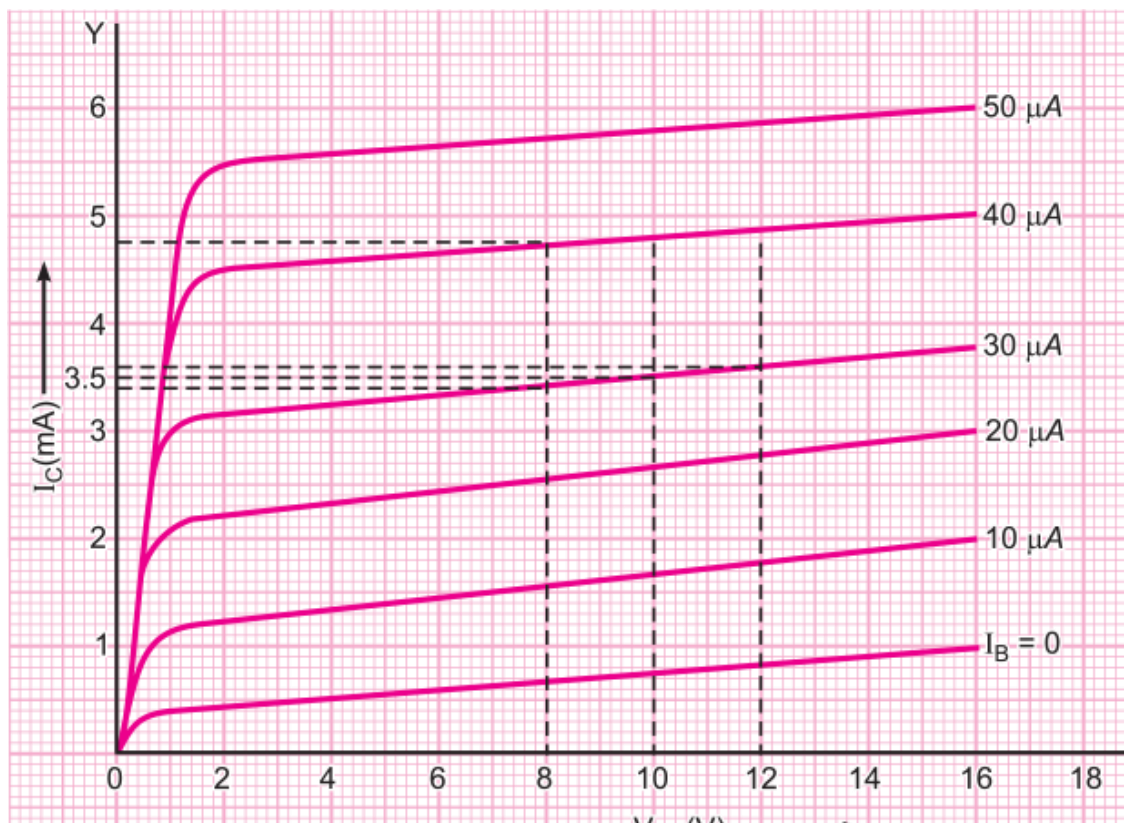

Ans. $X = \bar{Y} = A + B$

The given circuit performs OR operation

Q. 11. Output characteristics of an n-p-n transistor in CE configuration is shown in the figure. Determine: [CBSE Delhi 2013]

(i) Dynamic output resistance
(ii) Dc current gain and
(iii) ac current gain at an operating point V_{CE} = 10 V, when I_B = 30 µA.

Ans. (i) Dynamic output resistance is given by

$$r_o = \left(\frac{\Delta V_{CE}}{\Delta I_C} \right)_{I_B}$$

For I_B = 30 µA, ΔV_{CE} = $(12 - 8)$ = 4V and ΔI_C = $(3.6 - 3.4)$ = 0.2 mA

$$\therefore \quad r_o = \frac{4V}{0.2 \; mA} = \frac{4}{0.2 \times 10^{-3}} = 2 \times 10^4 \; ohm$$

(ii)

$$\beta_{dc} = \frac{I_C}{I_B}$$

At V_{CE} = 10 V and I_B = 30 µ A, the value of I_C = 3.5m A

$$\beta_{dc} = \frac{3.5 \; mA}{30 \; \mu A} = \frac{3.5 \times 10^{-3}}{30 \times 10^{-6}} \quad \Rightarrow \quad \beta_{dc} = 117$$

(iii)

$$\text{ac current gain } \beta_{dc} = \left(\frac{\Delta I_C}{\Delta I_B} \right)_{V_{CE}}$$

At V_{CE} =10 V, ΔI_C = $(3.5 - 2.5)$ mA = 1 mA

and ΔI_B = $(30 \; \mu A - 20 \; \mu A)$ = 10 µA

$$\therefore \quad \beta_{dc} = \frac{1 \; mA}{10 \mu A} = 100$$

Q. 12. Draw V – I characteristics of a p–n junction diode. Answer the following questions, giving reasons:

(i) Why is the current under reverse bias almost independent of the applied potential upto a critical voltage?

(ii) Why does the reverse current show a sudden increase at the critical voltage?

Name any semiconductor device which operates under the reverse bias in the breakdown region.   [CBSE (AI) 2013]

Ans. (i) In the reverse biasing, the current of order of µA is due to movement/drifting of minority charge carriers from one region to another through the junction.

A small applied voltage is sufficient to sweep the minority charge carriers through the junction. So, reverse current is almost independent of critical voltage.

(ii) At critical voltage (or breakdown voltage), a large number of covalent bonds break, resulting in the increase of large number of charge carriers. Hence, current increases at critical voltage.
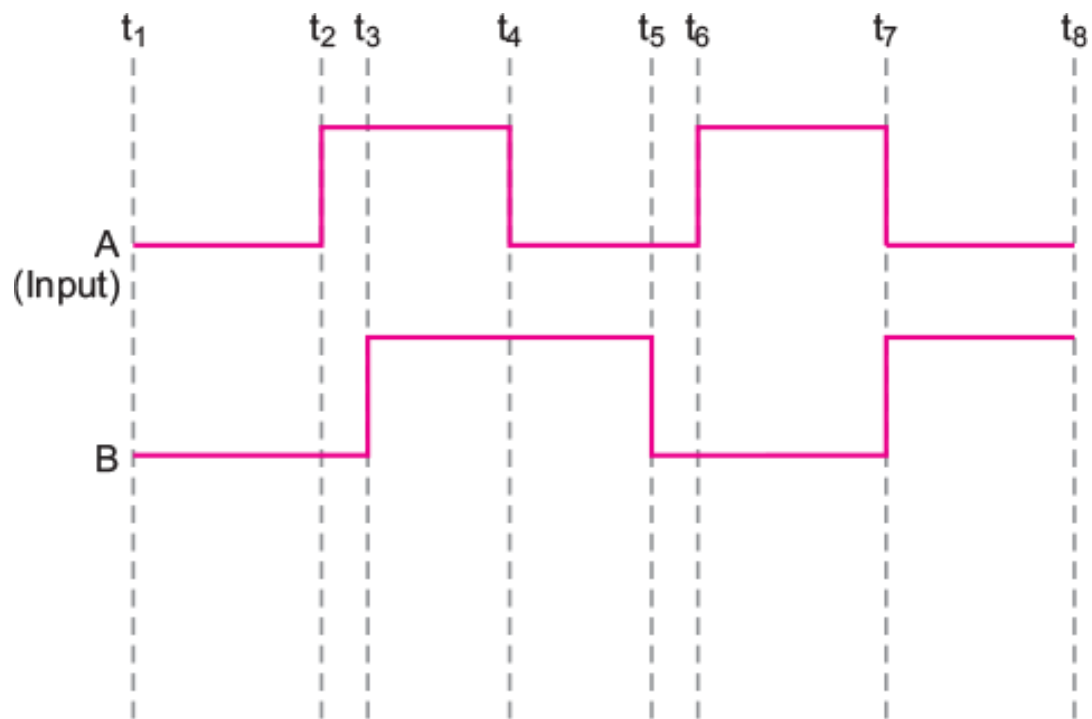
Semiconductor device that is used in reverse biasing is zener diode.
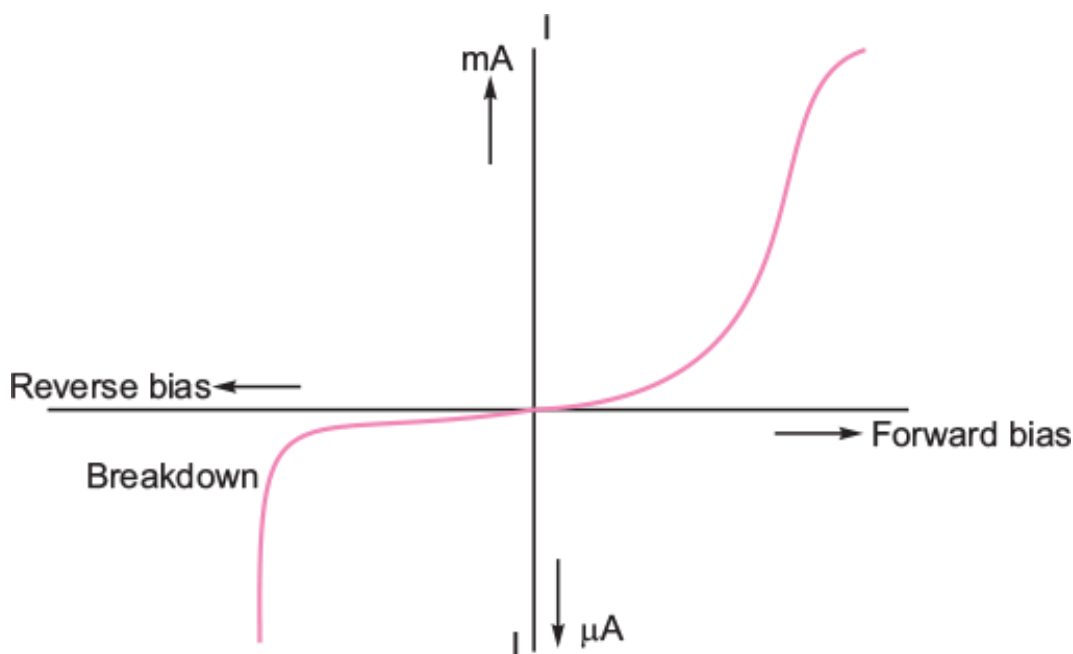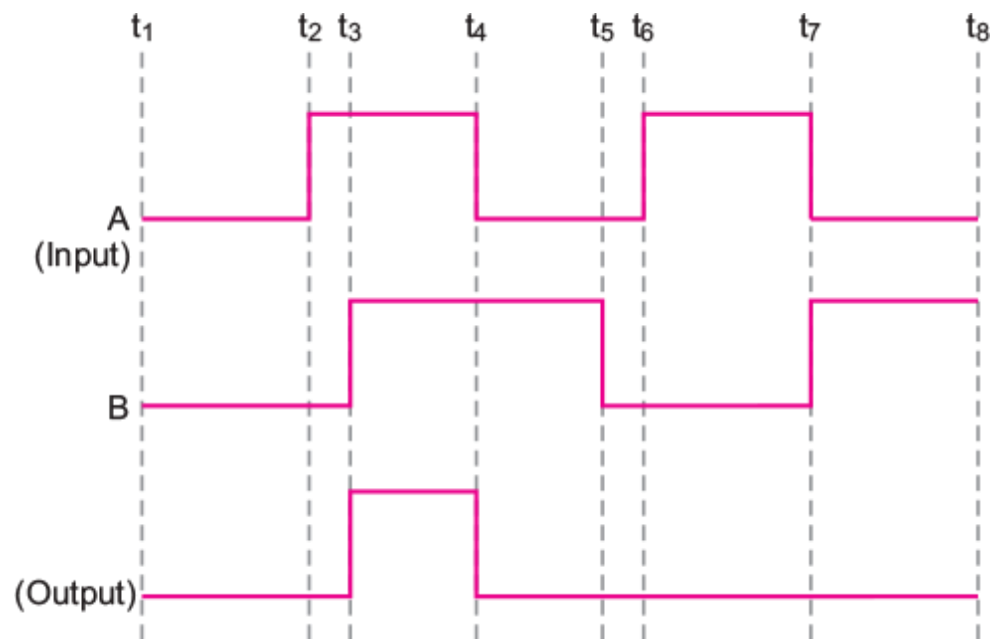

Q. 13. Answer the following question:

(i) Write the functions of the three segments of a transistor.

(ii) The figure shows the input waveforms A and B for 'AND' gate. Draw the output waveform and write the truth table for this logic gate.   CBSE (AI) 2017]

Ans. Output waveform for AND gate is

Truth Table

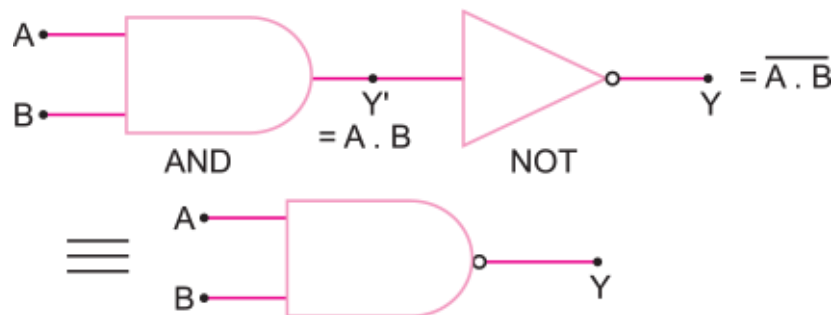| Input		Output
A	B	Y = A.B
0	0	0
0	1	0
1	0	0
1	1	1

Q. 14. The following figure shows the input waveforms (A, B) and the output waveform (Y) of a gate. Identify the gate, write its truth table and draw its logic symbol.
[CBSE North 2016]

Ans. Gate is **NAND** Gate.

Truth Table

Input		Output
A	B	$Y = \overline{A.B}$
0	0	1
1	0	1
0	1	1
1	1	0

Q. 15. In the circuit shown in the figure, identify the equivalent gate of the circuit and make its truth table. [CBSE (AI) 2013]
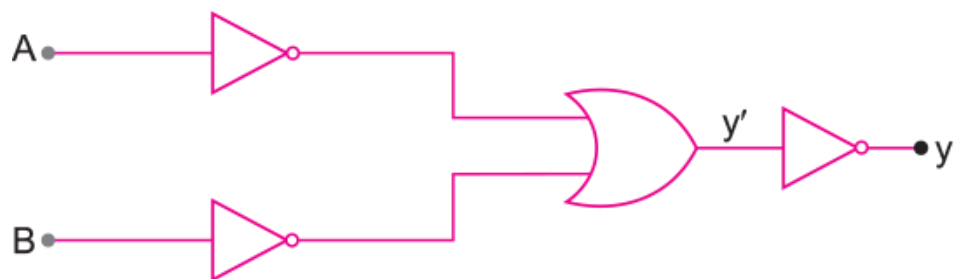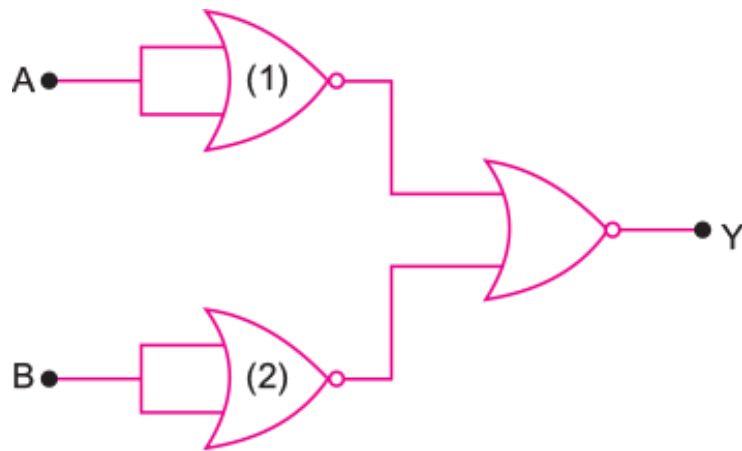
Ans. AND Gate

Truth Table

A	B	$Y = \bar{A}.\bar{B}$
0	0	0
1	0	0
0	1	0
1	1	1

Extended Truth Table

A	B	$\bar{A}$	$\bar{B}$	$Y' = \bar{A} + \bar{B}$	$y = \overline{\bar{A} + \bar{B}}$
0	0	1	1	1	0
1	0	0	1	1	0
0	1	1	0	1	0
1	1	0	0	0	1

Q. 16. The inputs A and B are inverted by using two NOT gates and their outputs are fed to the NOR gate as shown below. [CBSE (AI) 2011, (F) 2014]

Analyse the action of the gates (1) and (2) and identify the logic gate of the complete circuit so obtained. Give its symbol and truth table.

Ans.

Output of gate (1), $Y_1 = \overline{A+A} = \bar{A}$

Output of gate (2), $Y_2 = \overline{B+B} = \bar{B}$

Output $Y = \overline{Y_1 + Y_2} = \overline{\bar{A} + \bar{B}} = \overline{\bar{A}} . \overline{\bar{B}} = AB$

Thus, gates (1) and (2) act on '**NOT**' gates and the complete circuit acts as '**AND**' gate. The symbol and truth table of complete circuit are given below:
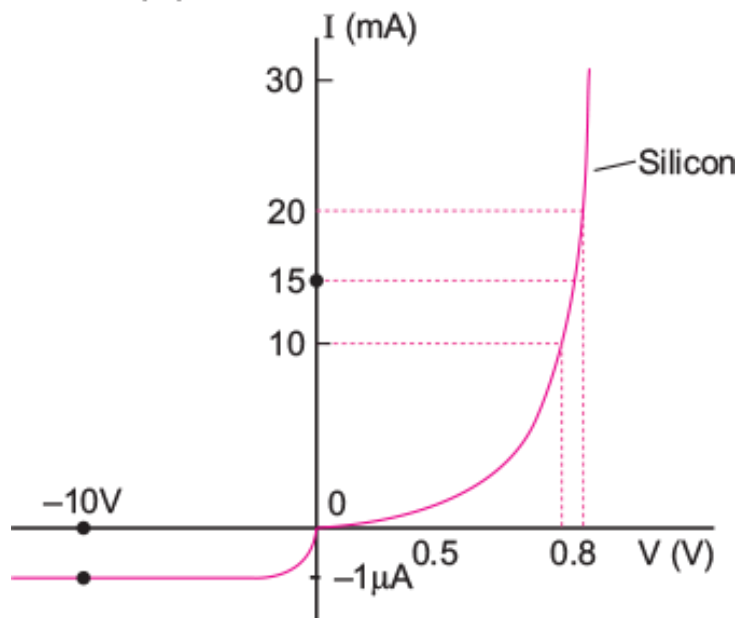

Truth Table

A	B	Y
0	0	0
1	0	0
0	1	0
1	1	1

Q. 17. The V – I characteristic of a silicon diode is as shown in the figure. Calculate the resistance of the diode at (i) I = 15 mA and (ii) V = – 10 V.   [CBSE (F) 2015]

Ans. (i) By considering straight line of V–I characteristic curve between 10 mA to 20 mA; and assuming passing through the origin, draw horizontal and vertical lines from 10 mA and 20 mA, we have

I_1 = 10 mA, V_1 = 0.7 V

and I_2 = 20 mA, V_2 = 0.8 V

Dynamic resistance in forward biasing can be given as

$$R = \frac{\Delta V}{\Delta I} = \frac{(0.8 - 0.7)V}{(20 - 10)\ \text{mA}}$$
$$= \frac{0.1V}{10\ \text{mA}} = \frac{0.1}{10} \times 10^3\ \Omega = 10\ \Omega$$

(ii) At – 10 V. The V–I characteristic graph is a straight line parallel to the voltage axis and not showing any variation. So, the static resistance can be given as

V = – 10 V and I = –1 μA

∴ Static resistance, $R = \frac{V}{I} = \frac{10\ V}{1\mu A} = \frac{10}{1 \times 10^{-6}} = 10^7 \Omega$

Q. 18. The current in the forward bias is known to be more (~mA) than the current in the reverse bias (~μA). What is the reason, then, to operate the photodiode in reverse bias?   [HOTS][CBSE Delhi 2012]

Ans. Consider the case of n-type semiconductor. The majority carrier (electron) density is larger than the minority hole density, i.e., n >> p.

On illumination, the no. of both types of carriers would equally increase in number as

n' = n + Δn, p' = p + Δp

But Δn = Δp and n >> p

Hence, the fractional change in majority carrier, i.e, $\frac{\Delta n}{n} << \frac{\Delta p}{p}$ (fractional change in minority carrier)

Fractional change due to photo-effects on minority carrier dominated reverse bias current is more easily measurable than the fractional change in majority carrier dominated forward bias current. Hence photodiodes are used in reverse bias condition for measuring light intensity.

Q. 19. Answer the following question : [CBSE (F) 2015]

(i) What is an 'integrated circuit (I.C.)'? Distinguish between (i) linear I.C. and (ii) Digital I.C.

(ii) Identify the equivalent gate for the following circuit and write its truth table.

The output of NOR gate is connected to both the inputs of NAND gate.
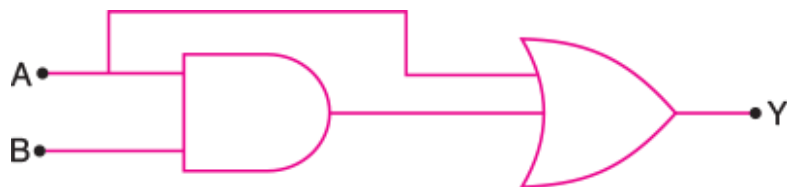
The equivalent gate is OR gate.

Input		Output	
A	**B**	**X**	**Y**
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

Short Answer Questions – II (OIQ)

Q. 1. Answer the following question :

(i) Write the truth table of the following gate.

(ii) What will be the values of inputs A and B for the Boolean expression
$(A \mp B).(A \mathbin{\overline{.}} B) = 1$

Ans. (i) Truth table of the given gate

Input			Output
A		B	$Y = A + AB$
0		0	0
1		0	1
0		1	0
1		1	1

(ii)

$A = 0,\ B = 0$

Other then $(A \mp B).(\overline{AB}) = (0 \mp 0)(0\,\overline{.}\,0) = \overline{0}\,.\,\overline{0} = 1\,.\,1 = 1$

Q. 2. The graph of potential barrier versus width of depletion region for an unbiased diode is shown in A. In comparison to A, graphs B and C are obtained after biasing the diode in different ways. Identify the type of biasing in B & C and justify your answer.
[CBSE Sample Paper 2016]
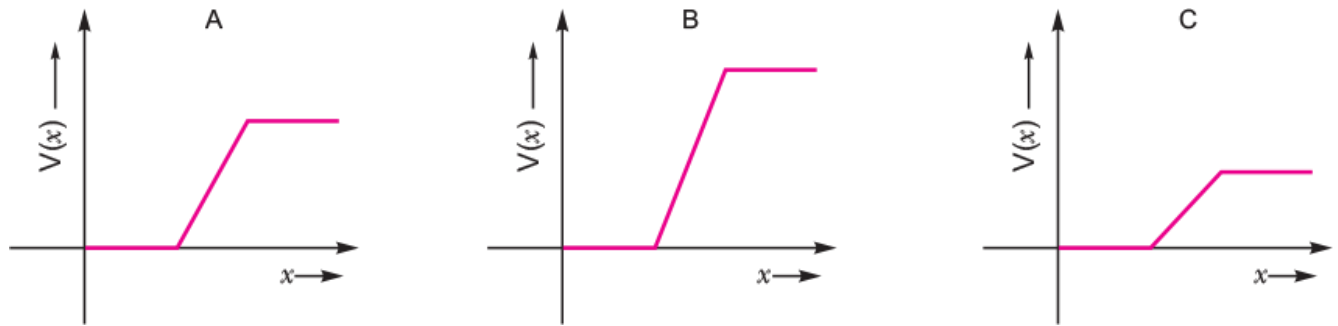
Ans. B : Reverse biased

Justification: When an external voltage V is applied across the semiconductor diode such that n-side is positive and p-side is negative, the direction of applied voltage is same as the direction of barrier potential. As a result, the barrier height increases and the depletion region widens due to the change in the electric field. The effective barrier height under reverse bias is $(V_0 + V)$.

C : Forward biased

Justification: When an external voltage V is applied across a diode such that p-side is positive and n-side is negative, the direction of applied voltage (V) is opposite to the barrier potential (V_0). As a result, the depletion layer width decreases and the barrier height is reduced. The effective barrier height under forward bias is $(V_0 - V)$.

Q. 3. A semiconductor has equal electron and hole concentration of 2×10^8 / m^3. On doping with a certain impurity, the hole concentration increases to 4×10^{10} / m^3.

(i) What type of semiconductor is obtained on doping?
(ii) Calculate the new electron and hole concentration of the semiconductor.
(iii) How does the energy gap vary with doping?

Ans. (i) Given $n_e = 2 \times 10^8$ / m^3, $n_h = 4 \times 10^{10}$ / m^3

(i) The majority charge carriers in doped semiconductor are holes, so semiconductor obtained is p-type semiconductor.

ii. $n_e n_h = n_i^2 \Rightarrow n_h = \dfrac{n_i^2}{n_h} = \dfrac{(2 \times 10^8)^2}{4 \times 10^{10}} = 10^6 / m^3$

New electron concentration $= 10^6$ / m^3

hole concentration $= 4 \times 10^{10}$ / m^3

iii. Energy gap decreases on doping.

Q. 4. A p-n junction germanium diode when forward biased has a drop of 0.3 V which is assumed to be independent of current. The current in excess of 10 mA

through the diode produces a large Joule-heating which damages (burns) the diode. If we want to use a 1.5 V battery to forward-bias the diode, what should be the value of resistor used in series with the diode, so that the maximum current does not exceed 6 mA?
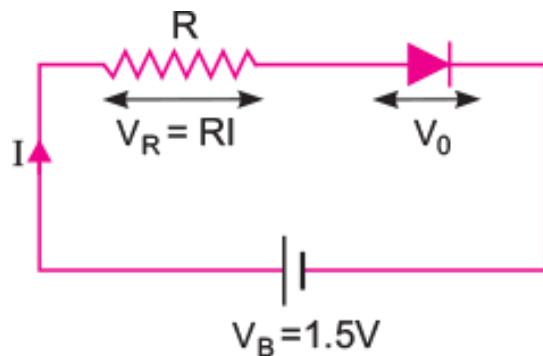

1.5 V
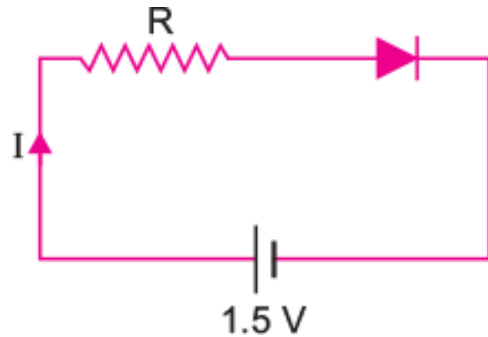
Ans. The basic equation of diode-circuit is

$$RI + V_0 = V_B \quad \Rightarrow \quad R = \frac{V_B - V_0}{I}$$

Here , $V_B = 1.5$ V, $V_0 = 0.3$ V, $I = 5$ mA $= 6 \times 10^{-3}$ A

$$\therefore \quad R = \frac{1.5 - 0.3}{6 \times 10^{-3}} = \frac{1.2 \times 10^3}{6} = 0.2 \times 10^3 \; \Omega = 200 \; \Omega$$

$V_B = 1.5V$

Q. 5. A change of 0.2 mA in the base current causes a change of 5 mA in the collector current for a common emitter amplifier.

(i) Find the ac current gain of the transistor.

(ii) If the input resistance is 2 kΩ and its voltage gain is 75, calculate the load resistor used in the circuit.

Ans. (i)

ac current gain, $\beta = \dfrac{\Delta I_C}{\Delta I_B} = \dfrac{5 \text{ mA}}{0.2 \text{ mA}} = 25$

(ii)

Voltage gain, $A_v = \beta \dfrac{R_L}{R_i}$

Load resistance $R_L = \dfrac{A_v R_i}{\beta} = \dfrac{75 \times 2 \times 10^3}{25} = 60 \times 10^3 \,\Omega = 6 \, k\Omega$

Q. 6. In a silicon transistor, the base current is changed by 20 µA. This results in a change of 0.02 V in base to emitter voltage and a change of 2 mA in the collector current.

(a) Find the input resistance, β_{ac} and trans conductance of the transistor.

(b) This transistor is used as an amplifier in CE configuration with a load resistance 5 kΩ. What is the voltage gain of the amplifier?

Ans. Given $\Delta I_B = 20$ µA $= 20 \times 10^{-3}$ mA $= 0.020$ mA,

$\Delta V_{BE} = 0.02$ V, $\Delta I_C = 2$ mA

a. Input resistance, $R_i = \dfrac{\Delta V_{BE}}{\Delta I_B} = \dfrac{0.02}{20 \times 10^{-6}} \Omega = 10^3 \Omega = 1 k\Omega$

Current gain, $\beta_{ac} = \dfrac{\Delta I_C}{\Delta I_B} = \dfrac{2 \text{ mA}}{0.020 \text{ mA}} = 100$

Trans conductance of a transistor is defined as the ratio of change in collector current to the change in base to emitter voltage at constant collector to emitter voltage, i.e.,

$g_m = \left(\dfrac{\Delta I_C}{\Delta V_{BE}} \right)_{V_{CE}=\text{cons}\tan t} = \dfrac{2 \times 10^{-3}}{0.02} = 0.1 W^{-1}$
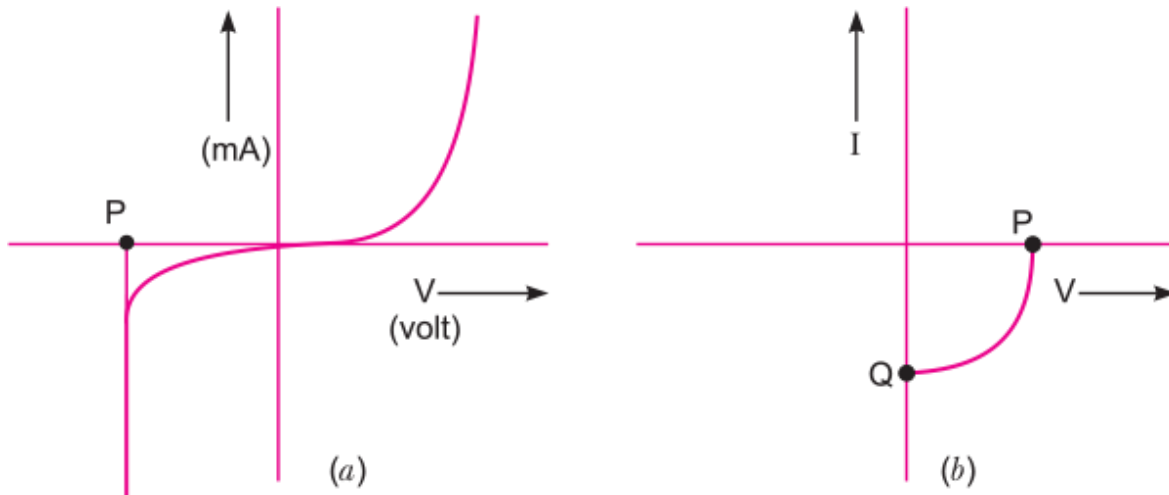
b. Voltage gain $A_v = \dfrac{R_L}{R_i} \times \beta$

Given RL = 5 kΩ = 5 × 103 Ω,

∴ $A_v = \dfrac{5 \times 10^3}{1000} \times 1000 = 500$

As CE amplifier causes a phase shift of 180° between input and output voltages, so voltage gain, $A_v = -500$.

Q. 7. Answer the following question :

(a)

(b)

(i) Name the type of a diode whose characteristics are shown in fig (a) and (b).

(ii) What does the points P in fig. (a) represent?

(iii) What does the points P and Q in fig (b) represent?
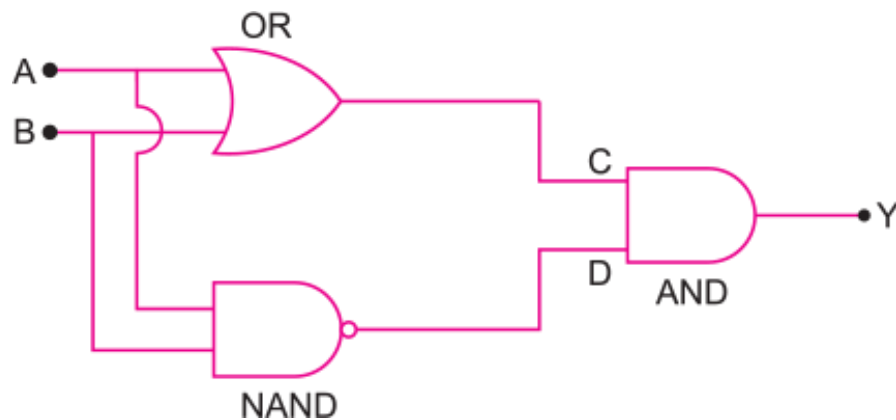**[HOTS][NCERT Exemplar]**

Ans. (i) ZENER junction diode and solar cell.

(ii) Zener breakdown voltage.

(iii) Q-short circuit current

P-open circuit voltage.

Q. 8. Identify the logic gate represented by the following circuit by writing its truth table:

Ans.

The output of OR gate, $C = A + B$

The output of NAND gate, $D = \overline{AB}$

The inputs of AND gate are C and D, so its output is $Y = C \cdot D = (A + B)\,\overline{AB}$

When $A = 0$, $B = 0$, $Y = (0 + 0)\,(\overline{0 \cdot 0}) = 0 \cdot \overline{0} = 0 \cdot 1 = 0$

When $A = 1$, $B = 0$, $Y = (1 + 0)\,(\overline{1 \cdot 0}) = 1 \cdot \overline{0} = 1 \cdot 1 = 1$

When $A = 0$, $B = 1$, $Y = (0 + 1)\,(\overline{0 \cdot 1}) = 1 \cdot \overline{0} = 1 \cdot 1 = 1$

When $A = 1$, $B = 1$, $Y = (1 + 1)\,(\overline{1 \cdot 1}) = 1 \cdot \overline{1} = 1 \cdot 0 = 0$

Thus, truth table of given circuit is:

A	B	Y
0	0	0
1	0	1
0	1	1
1	1	0

This is the truth table of XOR gate, hence the given circuit represents **XOR gate.**

Q. 9. Give reasons for the following:

(i) The Zener diode is fabricated by heavily doping both the p and n sides of the junction.

(ii) A photodiode, when used as a detector of optical signals is operated under reverse bias.

(iii) The band gap of the semiconductor used for fabrication of visible LED's must at least be 1.8 eV.   [HOTS]

Ans. (i) Heavy doping makes the depletion region very thin. This makes the electric field of the junction very high, even for a small reverse bias voltage. This in turn helps the Zener diode to act as a 'voltage regulator'.

(ii) When operated under reverse bias, the photodiode can detect changes in current with changes in light intensity more easily.

(iii) The photon energy, of visible light photons varies about 1.8 eV to 3 eV. Hence, for visible LED's, the semiconductor must have a band gap of 1.8 eV.

Q. 10. In the circuit shown in figure, when the input voltage of the base resistance is 10 V, V$_{BE}$ is zero and V$_{CE}$ is also zero. Find the values of I$_B$, I$_C$ and β. [HOTS][NCERT Exemplar]
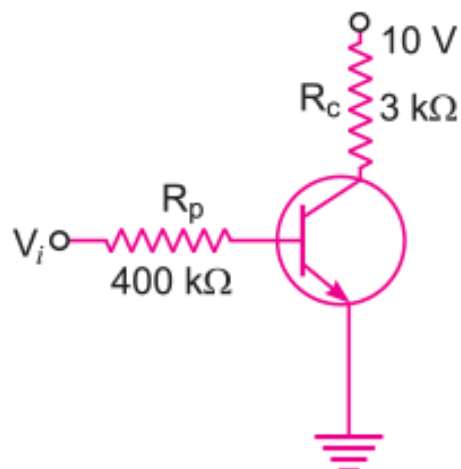
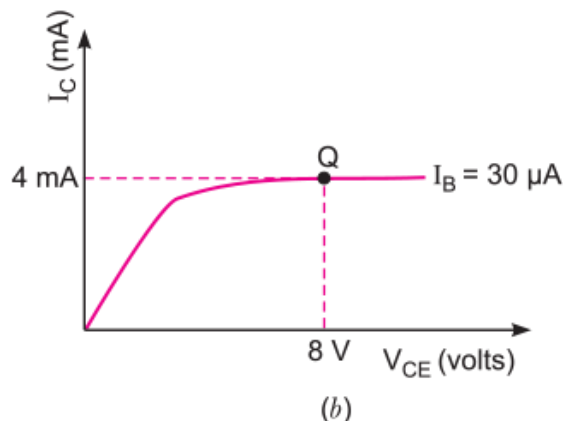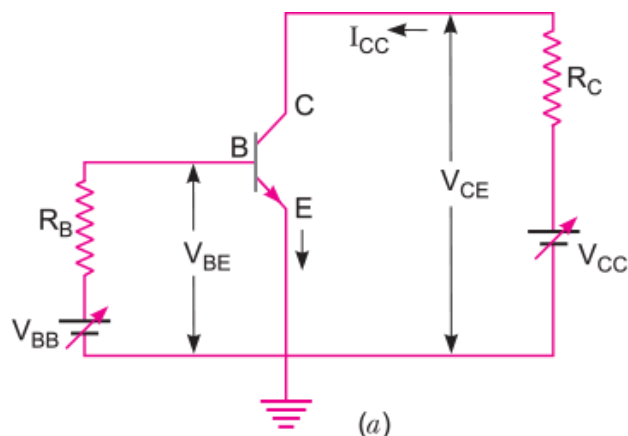**Ans.**

As $V_{BE} = 0$, potential drop across R_B is 10 V.

$$\therefore \quad I_B = \frac{10}{400\times10^3} = 25\mu A \qquad\qquad (\because V_i - V_{BE} = R_B I_B)$$

Since $V_{CE} = 0$, potential drop across R_C i.e., $I_C R_C$ is 10 V.

$$\therefore \quad I_C = \frac{10}{3\times10^3} = 3.33 \times 10^{-3} = 3.33 \text{ mA} \qquad\qquad (\because V_{CC} - V_{CE} = I_C R_C)$$

$$\therefore \quad \beta = \frac{I_C}{I_B} = \frac{333\times10^{-3}}{25\times10^{-6}} = 1.33 \times 10^2 = 133.$$

Q. 11. Consider the circuit arrangement shown in Fig. (a) for studying input and output characteristics of npn transistor in CE configuration.   **[HOTS]**

(a)   (b)

Select the values of R_B and R_C for a transistor whose V_{BE} = 0.7 V, so that the transistor is operating at point Q as shown in the characteristics shown in Fig. (b).

Given that the input impedance of the transistor is very small and V_{CC} = V_{BB} = 16V, also find the voltage gain and power gain of circuit making appropriate assumptions.
[*NCERT Exemplar*]

Ans. From the output characteristics at point Q, V_{CE} = 8 V and I_C = 4 mA

$V_{CC} = I_C R_C + V_{CE}$

$$R_C = \frac{V_{CC} - V_{CE}}{I_C} = \frac{16 - 8}{4 \times 10^{-3}} = 2\,k\Omega$$

Since, $V_{BB} = I_B R_B + V_{BE}$ or $R_B = \frac{V_{BB} - V_{BE}}{I_B}$ $\Rightarrow$

$$R_B = \frac{16 - 0.7}{30 \times 10^{-6}} = 510\,k\Omega$$

Now, $\beta = \frac{I_C}{I_B} = \frac{4 \times 10^{-3}}{30 \times 10^{-6}} = 133$

Voltage gain $= A_v = -\,\beta\frac{R_C}{R_B} = -\,133 \times \frac{2 \times 10^3}{510 \times 10^3} = -\,0.52$

Power gain $= A_p = \beta \times A_V = 133 \times 0.52 = 69$

Q. 12. Explain the following:

(i) In the active state of the transistor, the emitter base junction acts as a low resistance while base collection region acts as high resistance.

(ii) Output characteristics are controlled by the input characteristics in common emitter transistor amplifier.

(iii) LEDs are made of compound semiconductor and not by elemental semiconductors.

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Ans. (i) Emitter base junction is forward biased whereas collector base junction is reverse biased.

(ii) Small change in the current I_B in the base circuit controls the large current I_C in the collector circuit $I_C = \beta I_B$

(iii) Elemental semiconductor's band gap is such that the emitted wavelength lies in I_R region. Hence cannot be used for making LED.