Architecture of 8085

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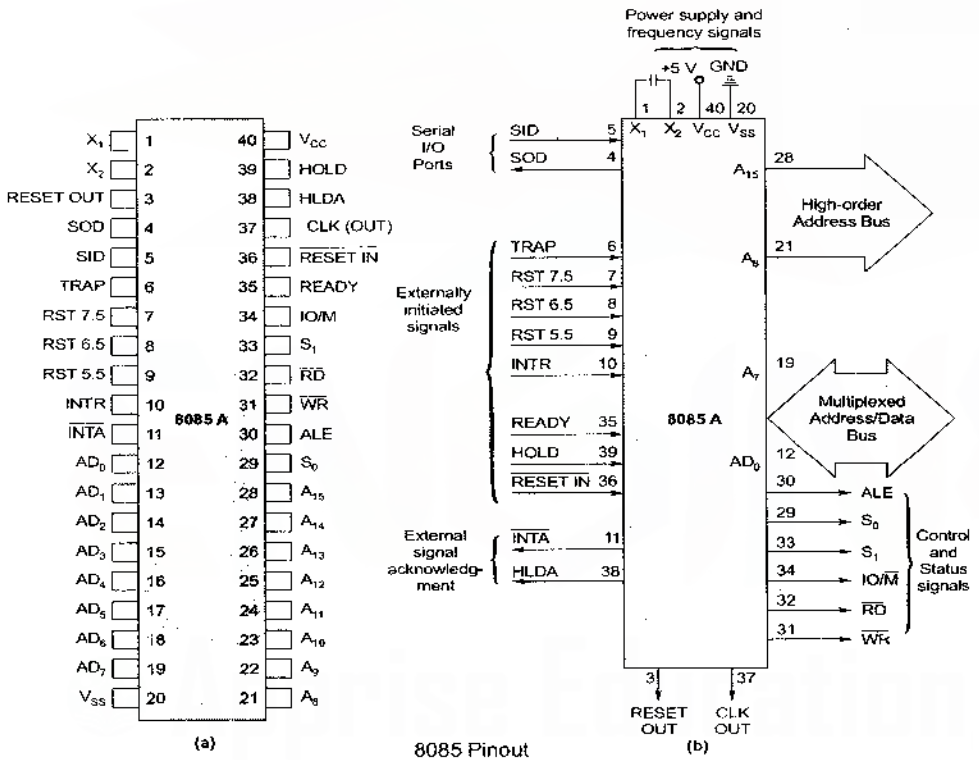
There are two types of architecture depending upon storage of program and data in memory

(i) Von Neumann architecture of computers : Intel 8085 Intel 8086

(ii) Harvard architecture of computer : TMS 32010, Intel 8051, Intel's Pentium etc.

Pin outs of 8085



8085 Pinout

Key features of 8085

(i) It is a 8-bit processor.

(ii) It has 8 data bus lines, which is the bit capacity of the microprocessor.

(iii) It has total 16 address lines with addressing capacity of 64 kB.

(iv) The crystal frequency of processor is 6 MHz and the clock frequency is 3.07 MHz (= 3 MHz), which is approximately half the crystal frequency.

(v) Low order address bus ($AD_0 - AD_7$) is multiplexed with data bus in order to reduce the number of pins.

(vi) To de-multiplex address from data, ALE (Address Latch Enable) signal is used.

ALE = 1, Address transfer to bus

ALE = 0, data transfer to bus.

(vii) Disadvantage of multiplexing is that speed will be reduced.

(viii) There are 5 hardware interrupts available for 8085.

(ix) 8085 has 74 basic instructions with 246 Opcodes.

Sr. No.	Signals	Pins
1.	Power supply signals	V_{CC}, V_{SS}
2.	Clock signals	X_1 X_2, CLK OUT
3.	Reset signals	RESETIN, RESET OUT
4.	Interrupt signals	TRAP, Restart interrupts (RST 7.5, REST 6.5 and RST 5.5), INTR, INTA
5.	Address bus and data bus	Address bus ($A_8 - A_{15}$) Multiplexed address/data bus ($AD_0 - AD_7$)
6.	Status signals and control signals	Address latch enable (ALE), Input output/ memory (IO/$\overline{M}$), Status signals (S_1 and S_0), Read ($\overline{RD}$), Write ($\overline{WR}$), READY
7.	Serial input/output signals	HOLD, HLDA
8.	DMA request signals	SID, (Serial input data), SOD (Serial output data)

Address bus ($A_8 - A_{16}$)

Higher order 8 bit of 16 bit address. The address bus is always unidirectional.

Multiplexed address/data bus ($AD_0 - AD_7$)

It is a bidirectional bus. The data bus is multiplexed with lower order address bus.

Control and status signal

(i) $\overline{RD}$ (Read) : When the signal is low on this pin, the microprocessor performs memory reading or I/O reading operation.

(ii) $\overline{WR}$ (Write) : When the signal is low on this pin, the microprocessor performs memory writing or I/O writing operation.

(iii) IO/$\overline{M}$: This status signal is used to give information of operation to be performed with memory or I/O device.

IO/M	$\overline{RD}$	$\overline{WR}$	Description
0	0	1	Memory read ($\overline{MEMR}$)
0	1	0	Memory write ($\overline{MEMW}$)
1	0	1	IO Read ($\overline{IOR}$)
1	1	0	IO Write ($\overline{IOW}$)

S_1 and S_0 : These two status signal used to indicate the status of the operation.

S_1	S_0	Microprocessor operation
0	0	Halt (No operation)
0	1	Write operation
1	0	Read operation
1	1	Opcode fetch (reading instruction)

Power supply and frequency signals

V_{CC} : Power supply pin of +5V

X_1 and X_2 : A crystal is connected across these pins. The frequency is internally divided by two.

CLK (out) : This pin, there will be synchronization between the different peripherals and microprocessor.

Serial I/O Port

(i) SID (Serial Input Data) : This pin is used for receiving the data into microprocessor serially.

(ii) SOD (Serial output data) : This pin is used for sending the data from the microprocessor serially.

Externally initiated signals

1. **Hardware interrupts**

   TRAP, RST-7.5, RST-6.5, RST-5.5, INTR are called Hardware interrupts.

   It is also used to accepts external interrupts to provide acknowledgment (Ack) to the external device.

Remember:

In priority order, interrupts are as TRAP > RST-7.5 > RST-6.5 > RST-5.5 > INTR.

2. **READY**

   It is used to interface with the slow peripheral devices (Memory or I/O devices) to the microprocessor.

3. **Reset**

   (a) $\overline{RESET\ IN}$: It is an active low signal, when this signal gets activated and microprocessor is reset.

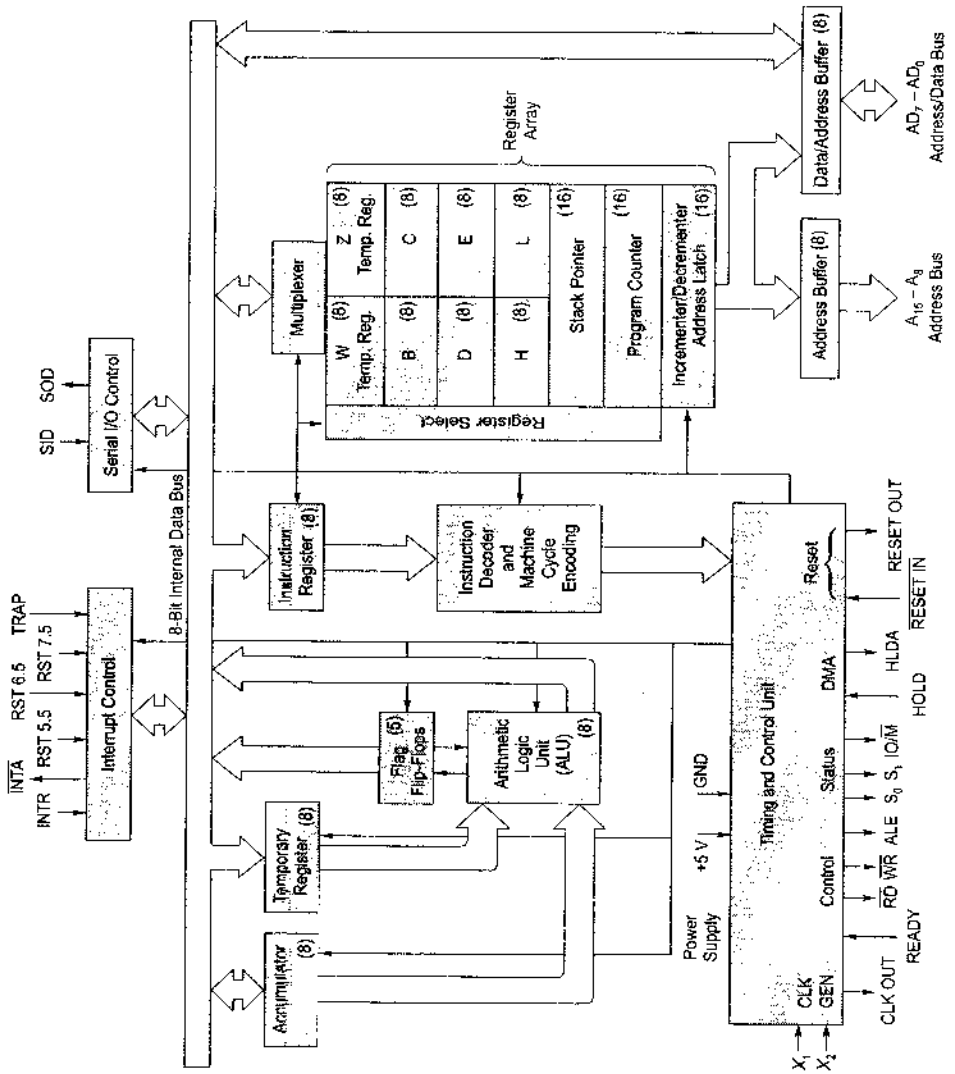
   (b) RESET OUT : This signal is used to reset the other peripheral devices.

4. **HOLD and HLDA**

   (a) HOLD : A peripheral like DMA controller sends the HOLD request to the microprocessor through this pin to leave the data bus which where also used by microprocessor.

   (b) HLDA : HOLD acknowledge

Internal Architecture of 8085 Microprocessor



The architecture is divided into following blocks:

1. Arithmetic and Logical Unit (ALU)

The ALU performs arithmetical and logical operations. It includes

(a) Accumulator : It is a 8 bit programmable register. All the arithmetic and logical operations performed with contents of accumulator and the results are store in accumulator only.

(b) Temporary Register : It is an 8 bit non-programmable register used to hold data during an arithmetics and logic operation.

(c) Arithmetic and logic circuits : This unit performs the actual numerical and logical operation.

(d) Flags : The flags generally reflect the status of arithmetic or logical operation.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
S	Z	×	AC	×	P	×	CY

- **Carry flag (CY):** If an arithmetic operation results in a carry, the CY flag is **set** otherwise it is **reset.**
- **Parity flag (P):**
  - ⇒ If the result has an even number of 1's, the flag is **set.**
  - ⇒ If the result has an odd number of 1's the flag is **reset.**
- **Auxiliary Carry (AC):** In an arithmetic operation.
  - ⇒ If carry is generated by bit D_3 and passed to D_4, flag is **set.**
  - ⇒ Otherwise it is **reset.**
- **Zero Flag (Z):**
  - ⇒ Zero flag is **set** to 1, when the result is zero.
  - ⇒ Otherwise it is **reset.**
- **Sign Flag (S):**
  - ⇒ Sign flag is **set** if bit D_7 of the result is 1.
  - ⇒ Otherwise it is **reset.**

Remember:

- Among the five flags, the AC flags is used internally for BCD arithmetic; the instruction set does not include any conditional Jump instruction based on the AC flag.
- 'x' in the flag register indicate the unused flip-flops.
- The values of D_1, D_3 and D_5 bits should be taken as '0' in programs while using PSW instruction.

2. Register array

The architecture of 8085 consist of following registers.

(a) Temporary registers :

(i) Temporary data register : It is also called as operand register (8-bit). It provides operands to the ALU.

(ii) Temporary registers (W and Z) : This registers are not available to the user.

Remember:

W and Z registers are used by 8085 for swap instruction.

(b) General purpose registers :

The 8085 microprocessor consists 6 general purpose registers i.e. B, C, D, E, H, and L of 8 bits each. These registers are available to the user.

Remember:

- The general purpose registers put together is called scratch and memory.
- The valid register pairs available are BC, DE and HL to store 16-bit of data.
- The HL register pair functions as default data pointer. If used as memory pointer it holds the address of a 16 bit address at a memory location.
- Accumulator can also be used along with status register to form a 16 bit programmable register called program status word (PSW).

(c) Special purpose registers

There are two 16-bit special purpose register i.e. program counter (PC) and stack pointer (SP).

(i) Program counter : It is a 16 bit register used to hold memory addresses.

(ii) Stack pointer : It is a 16 bit register used as a memory pointer.

Remember:

- When the microprocessor is reset, the PC sets to zero.
- Stack grows from bottom to top following last in first out (LIFO) structure and the SP contents keep decreasing as stack grows.

3. Increment and Decrement Latch

It is used for increment or decrement of 16 bit address, always increment and decrement by '1'.

4. Timing and control unit

It controls all internal and external circuits in the microprocessor system.

Remember: .....

The microprocessor uses a quartz crystal (LC or RC circuits) to determine the clock frequency, so that other timing and control signals are developed.

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5. Instruction Register and Decoder

It is the part of ALU and not Assessible to the user.

(a) **Instruction register** :– The instruction register holds the opcode of the instruction that is decoded and executed.

(b) **Instruction decoder** : – The output of instruction register connected to the decoder. The decoder decodes the instruction and establishes the sequence of events to follow.

6. Interrupt Control Unit

The interrupt control units job is to service the interrupt and after completing the interrupt service routine return back the control to the main program where it was interrupted.

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