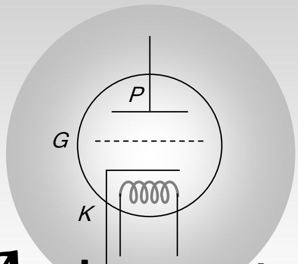


Assignment

Vacuum tubes (Diode and Triode)

1. Thermionic emission from a heated filament varies with its temperature *T* as **[CBSE 1990; RPMT 2000; CPMT 2002]**

   (a) T^{-1} (b) T (c) T^2 (d) $T^{3/2}$

2. Number of secondary electrons emitted per number of primary electrons depends on **[RPET 2000]**

   (a) Material of target (b) Frequency of primary electrons
   (c) Intensity (d) None of the above

3. Due to S.C.R in vacuum tube **[RPET 2000]**

   (a) $I_p \rightarrow$ Decrease (b) $I_p -$ Increase (c) $V_p =$ Increase (d) $V_g =$ Increase

4. In diode, when there is saturation current, the plate resistance (r_p) is **[AIIMS 1997; Haryana PMT 2000]**

   (a) Zero (b) Infinite (c) Some finite quantity (d) Data is insufficient

5. The grid voltage of any triode valve is changed from -1 volt to - 3 *volt* and the mutual conductance is 3×10^{-4} *mho*. The change in plate circuit current will be **[MNR 1999]**

   (a) 0.8 *mA* (b) 0.6 *mA* (c) 0.4 *mA* (d) 1 *mA*

6. In a triode, $g_m = 2 \times 10^{-3} ohm^{-1}; \mu = 42$, resistance load, $R = 50$ kilo ohm. The voltage amplification obtained from this triode will be **[MNR 1999]**

   (a) 30.42 (b) 29.57 (c) 28.18 (d) 27.15

7. In an amplifier the load resistance R_L is equal to the plate resistance (r_p). The voltage amplification is equal to **[CPMT 1995]**

   (a) μ (b) 2μ (c) $\mu / 2$ (d) $\mu / 4$

8. For a given plate-voltage, the plate current in a triode is maximum when the potential of **[IIT-JEE 1985; CPMT 1995; AFMC 1999]**

   (a) The grid is positive and plate is negative (b) The grid is positive and plate is positive
   (c) The grid is zero and plate is positive (d) The grid is negative and plate is positive

9. If $R_p = 7K\Omega, g_m = 2.5$ *millimho*, then on increasing plate voltage by $50V$, how much the grid voltage is changed so that plate current remains the same **[RPET 1996]**

   (a) - 2.86 *V* (b) - 4 *V* (c) + 4 *V* (d) + 2 *V*

10. The amplification factor of a triode is 20 and trans-conductance is 3 *milli mho* and load resistance $3 \times 10^4 \Omega$, then the voltage gain is **[RPMT 1996]**

    (a) 16.36 (b) 28 (c) 78 (d) 108

11. In a triode amplifier, $\mu = 25, r_p = 40$ kilo ohm and load resistance $R_L = 10$ kilo ohm. If the input signal voltage is 0.5 volt, then output signal voltage will be **[RPMT 1995]**

    (a) 1.25 *volt* (b) 5 *volt* (c) 2.5 *volt* (d) 10 *volt*

12. The amplification factor of a triode is 20. If the grid potential is reduced by 0.2 *volt* then to keep the plate current constant its plate voltage is to be increased by **[RPMT 1993, 95]**
(a) 10 *volt* (b) 4 *volt* (c) 40 *volt* (d) 100 *volt*

13. For a triode $r_p = 10$ *kilo ohm* and $g_m = 3$ *milli mho*. If the load resistance is double of plate resistance, then the value of voltage gain will be **[RPMT 1994]**
(a) 10 (b) 20 (c) 15 (d) 30

14. The amplification produced by a triode is due to the action of **[AFMC 1994]**
(a) Filament (b) Cathode (c) Grid (d) Plate

15. In an experiment, the saturation in the plate current in a diode is observed at 240 *V*. But a student still wants to increase the plate current. It can be done, if **[MNR 1994]**
(a) The plate voltage is increased further (b) The plate voltage is decreased
(c) The filament current is decreased (d) The filament current is increased

16. In a triode amplifier, the value of maximum gain is equal to **[MP PMT 1992]**
(a) Half the amplification factor (b) Amplification factor
(c) Twice the amplification factor (d) Infinity

17. For a given triode $\mu = 20$. The load resistance is 1.5 times the anode resistance. The maximum gain will be **[CPMT 1992]**
(a) 16 (b) 12 (c) 10 (d) None of the above

18. The amplification factor of a triode is 20. Its plate resistance is 10 kilo ohms. Mutual conductance is
(a) 2×10^5 *mhos* (b) 2×10^4 *mhos* (c) 500 *mhos* (d) 2×10^{-3} *mhos*

19. The voltage gain of a triode depends upon **[CPMT 1992]**
(a) Filament voltage (b) Plate voltage (c) Plate resistance (d) Plate current

20. In a triode valve **[MP PET 1992]**
(a) If the grid voltage is zero then plate current will be zero
(b) If the temperature of filament is doubled, then the thermionic current will also be doubled
(c) If the temperature of filament is doubled, then the thermionic current will nearly be four times
(d) At a definite grid voltage the plate current varies with plate voltage according to Ohm's law

21. The plate current i_p in a triode valve is given $i_p = K(V_p + \mu V_g)^{3/2}$ where i_p is in milliampere and V_p and V_g are in *volt*. If r_p = 10^4 *ohm*, and $g_m = 5 \times 10^{-3} mho$, then for $i_p = 8\,mA$ and $V_p = 300\ volt$, what is the value of *K* and grid cut off voltage **[Roorkee 1992]**
(a) - 6 *V*, $(30)^{3/2}$ (b) $-6V, (1/30)^{3/2}$ (c) + 6 *V*, $(30)^{3/2}$ (d) + 6 *V*, $(1/30)^{3/2}$

22. The amplification factor of a triode valve is 15. If the grid voltage is changed by 0.3 *volt* the change in plate voltage in order to keep the plate current constant (in volt) is
(a) 0.02 (b) 0.002 (c) 4.5 (d) 5.0

23. The slopes of anode and mutual characteristics of a triode are 0.02 *mA* V^{-1} and 1 *mA* V^{-1} respectively. What is the amplification factor of the valve **[MP PMT 1990]**
(a) 5 (b) 50 (c) 500 (d) 0.5

24. The slope of plate characteristic of a vacuum tube diode for certain operating point on the curve is $10^{-3}\frac{mA}{V}$. The plate resistance of the diode and its nature respectively
(a) 100 kilo-ohms static (b) 1000 *kilo-ohms* static (c) 1000 *kilo-ohms* dynamic (d) 100 *kilo-ohms* dynamic

25. A triode has a mutual conductance of $2 \times 10^{-3} mho$ and an amplification factor of 50. The anode is connected through a resistance of 25×10^3 *ohms* to a 250 *volts* supply. The voltage gain of this amplifier is **[MP PMT 1989]**
(a) 50 (b) 25 (c) 100 (d) 12.5

26. 14×10^{15} electrons reach the anode per second. If the power consumed is 448 *milliwatts*, then the plate (anode) voltage is **[MP PMT 1989]**

(a) 150 *V* (b) 200 *V* (c) $14 \times 448\,V$ (d) 448/14 *V*

27. A valve oscillator is **[MP PMT 1988]**

(a) Simple diode (b) Double diode (c) Triode (d) *L-C* circuit

28. Amplification factor of a triode is 20. If the grid voltage is reduced by one volt, how much should the plate voltage be increased so that plate current remains constant

(a) 10 *V* (b) 1/10 *V* (c) 1/20 *V* (d) 20 *V*

29. If the amplification factor of a triode valve is 100, then at plate potential of 250 *volt* the cutoff voltage of its grid will be **[MP PET 1989]**

(a) 0 *V* (b) - 0.4 *V* (c) - 2.5 *V* (d) - 150 *V*

30. In the circuit of a triode valve, there is no change in the plate current, when the plate potential is increased from 200 *volt* to 220 *volt* and the grid potential is decreased from - 0.5 *volt* to -1.3 *volt*. The amplification factor of this valve is

(a) 15 (b) 20 (c) 25 (d) 35

31. If the amplification factor of a triode (μ) is 22 and its plate resistance is 6600 *ohm*, then the mutual conductance of this valve is mho is

[MP PMT 1989]

(a) $\frac{1}{300}$ (b) 25×10^{-2} (c) 2.5×10^{-2} (d) 0.25×10^{-2}

32. For a triode, at $V_g = -1$ *volt*, the following observations were taken $V_p = 75\,V, I_p = 2mA$, $V_p = 100\,V, I_p = 4mA$. The value of plate resistance will be **[MP PMT 1989]**

(a) 25 KΩ (b) 20.8 KΩ (c) 12.5 KΩ (d) 100 KΩ

33. The triode constant is out of the following **[RPMT 1989]**

(a) Plate resistance (b) Amplification factor (c) Mutual conductance (d) All the above

34. The unit of mutual conductance of a triode valve is **[MP PMT 1988]**

(a) Siemen (b) *Ohm* (c) *Ohm metre* (d) *Joule Coulomb*$^{-1}$

35. With a change of load resistance of a triode, used as an amplifier, from 50 *kilo ohms* to 100 *kilo ohms*, its voltage amplification changes from 25 to 30. Plate resistance of the triode is **[MP PET 1986]**

(a) 25 *Kilo ohms* (b) 75 *Kilo ohms* (c) 7.5 *Kilo ohms* (d) 2.5 *Kilo ohms*

36. The linear portions of the characteristic curves of a triode valve give the following readings **[Roorkee 1985]**

V_g (*volt*)	0	- 2	- 4	- 6
$I_p(mA)$ for $V_p = 150$ *volts*	15	12.5	10	7.5
$I_p(mA)$ for $V_p = 120$ *volts*	10	7.5	5	2.5

The plate resistance is

(a) 2000 *ohms* (b) 4000 *ohms* (c) 8000 *ohms* (d) 6000 *ohms*

37. The amplification factors of a triode is 10. If the grid potential is reduced by 0.4 *volt* then what should be the increase in plate potential, so that the current remains constant **[RPET 1984]**

(a) 0.4 *V* (b) 40 *V* (c) 4 *V* (d) 14 *V*

38. Select the correct statements from the following **[IIT-JEE 1984]**

(a) A diode can be used as a rectifier

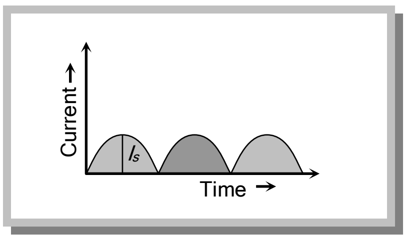
(b) A triode cannot be used as a rectifier

(c) The current in a diode is always proportional to the applied voltage

(d) The linear portion of the I-V characteristic of a triode is used for amplification without distortion

39. The output current versus time curve of a rectifier is shown in the figure. The average value of the output current in this case is **[AIIMS 1982]**

(a) 0



(b) $\frac{i_0}{\pi}$

(c) $\frac{2i_0}{\pi}$

(d) i_0

40. The introduction of a grid in a triode valve affects plate current by **[CPMT 1975, 90]**

(a) Making the thermionic emission easier at low temperature (b) Releasing more electrons from the plate

(c) By increasing plate voltage (d) By neutralising space charge

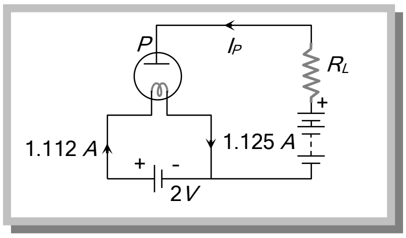
41. Before the saturation state of a diode at the plate voltages of 400 *V* and 200 *V* respectively the currents are i_1 and i_2 respectively. The ratio i_1/i_2 will be

(a) $\sqrt{2}/4$ (b) $2\sqrt{2}$ (c) 2 (d) 1/2

42. The value of constant *A* in Richardson-Dushman equation in $A/m^2/K^2$ is

(a) $\frac{4\pi me}{h^3}$ (b) $\frac{4\pi me^2}{h^3}$ (c) $\frac{4\pi me^2k}{h^3}$ (d) $\frac{4\pi mk^2e}{h^3}$

43. The value of plate current in the given circuit diagram will be



(a) 3 *mA*

(b) 8 *mA*

(c) 13 *mA*

(d) 18 *mA*

44. The plate resistance of a diode valve is 5000 Ω. If the value of plate current is 4.5 *mA* at a plate potential of 70 *V*, then what will be the plate potential at plate current of 6.5 *mA*

(a) 60 *V* (b) 70 *V* (c) 80 *V* (d) 90 *V*

45. A certain triode shows the following readings

V_p	V_g	I_p
150 *V*	-2 *V*	5 *mA*
150 *V*	-3.5 *V*	3.2 *mA*
195 *V*	-3.5 *V*	5 *mA*

The amplification factor of the triode is

(a) 22.5 (b) 45 (c) 30 (d) 60

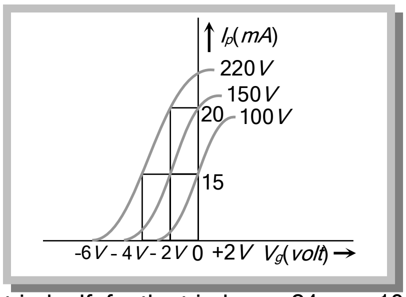
46. The relation between dynamic plate resistance (r_p) of a vacuum diode and plate current in the space charge limited region, is

(a) $r_p \propto I_p$ (b) $r_p \propto I_p^{3/2}$ (c) $r_p \propto \frac{1}{I_p}$ (d) $r_p \propto \frac{1}{(I_p)^{1/3}}$

47. The voltage gain of a triode amplifier is 50. An input signal of $V_g = 20 \sin \omega t \, mV$ is applied in the grid circuit. The output voltage will be

(a) $-1000 \sin \omega t$ *V* (b) $-50 \sin \omega t$ *V* (c) $-20 \sin \omega t$ *V* (d) $-\sin \omega t$ *V*

48. The mutual characteristic curves of a triode are shown in the following figure. The ac mutual conductance of triode will be



(a) 2.5 *m mho*

(b) 5.0 *m mho*

(c) 7.5 *m mho*

(d) 10.0 *m mho*

49. An a.c. signal of IV (*r.m.s.*) and frequency 1 *KHz* is applied to the grid of a triode. If, for the triode μ = 24, r_p = 10 *k*Ω and R_L = 10 *K*Ω, then the voltage gain of the amplifier will be

(a) 4 (b) 8 (c) 12 (d) 16

50. Mutual characteristic curves in working field of triode are parallel lines.

When $V_p = 200\ V$ value of plate current $i_p = (3V_g + 10)mA$ and when $V_p = 150,\ V$ value of plate current $i_p = (3V_g + 6)mA$

Application factor of triode value is

(a) 12.5 (b) 4.33 (c) 15.5 (d) 37.5

Logic gates

51. How many NAND gates are used to form an AND gate **[MP PET 2004]**

(a) 1 (b) 2 (c) 3 (d) 4

52. A gate has the following truth table **[CBSE PMT 2000]**

P	1	1	0	0
Q	1	0	1	0
R	1	0	0	0

The gate is

(a) NOR (b) OR (c) NAND (d) AND

53. A logic gate is an electronic circuit which **[BHU 2000]**

(a) Makes logic decisions

(b) Allows electrons flow only in one direction

(c) Works binary algebra

(d) Alternates between 0 and 1 values

54. The logic behind 'NOR' gate is that it gives **[CPMT 1999, AFMC 1999]**

(a) High output when both the inputs are low

(b) Low output when both the inputs are low

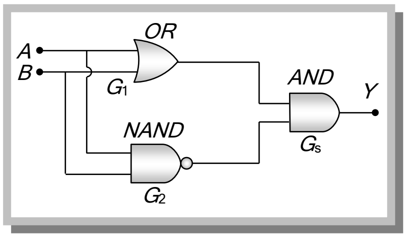
(c) High output when both the inputs are high

(d) None of these

55. Boolean algebra is essentially based on **[AIIMS 1999]**

(a) Truth (b) Logic (c) Symbol (d) Numbers

56. The following configuration of gate is equivalent to **[AMU 1999]**



(a) NAND

(b) XOR

(c) OR

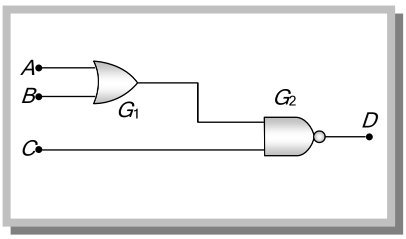
(d) None of these

57. The truth-table given below is for which gate **[CBSE PMT 1998]**

A	0	0	1	1
B	0	1	0	1
C	1	1	1	0

(a) XOR (b) OR (c) AND (d) NAND

58. For the given combination of gates, if the logic states of inputs A, B, C are as follows $A = B = C = 0$ and $A = B = 1$, $C = 0$ then the logic states of output D are **[AMU 1998]**



(a) 0, 0

(b) 0, 1

(c) 1, 0

(d) 1, 1

59. The truth table shown in figure is for **[Pb. CET 1998]**

A	0	0	1	1
B	0	1	0	1
Y	1	0	0	1

(a) XOR (b) AND (c) XNOR (d) OR

60. Which one of the following gates can be served as a building block for any digital circuit **[CPMT 1996]**

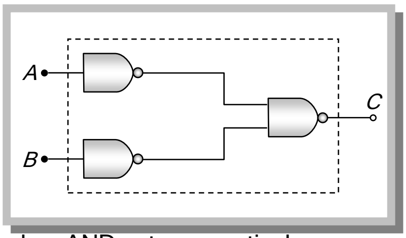
(a) OR (b) AND (c) NOT (d) NAND

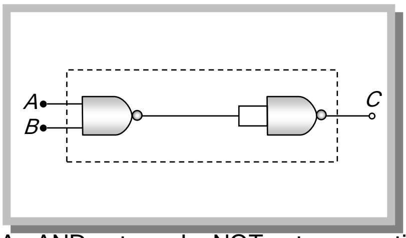
61. A truth table is given below. Which of the following has this type of truth table **[CBSE PMT 1996]**

A	0	1	0	1
B	0	0	1	1
y	1	0	0	0

(a) XOR gate (b) NOR gate (c) AND gate (d) OR gate

62. The combination of 'NAND' gates shown here under (figure) are equivalent to **[Haryana CEET 1996]**





(a) An OR gate and an AND gate respectively (b) An AND gate and a NOT gate respectively

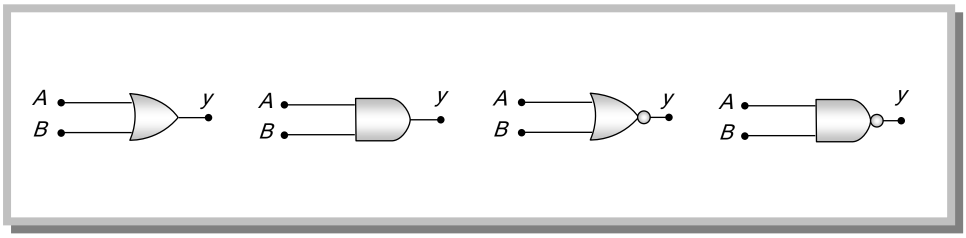
(c) An AND gate and an OR gate respectively (d) An OR gate and a NOT gate respectively.

63. The following truth table corresponds to the logic gate **[BHU 1994]**

A	0	0	1	1
B	0	1	0	1
X	0	1	1	1

(a) NAND (b) OR (c) AND (d) XOR

64. Given below are four logic gate symbol (figure). Those for OR, NOR and NAND are respectively **[NSEP 1994]**



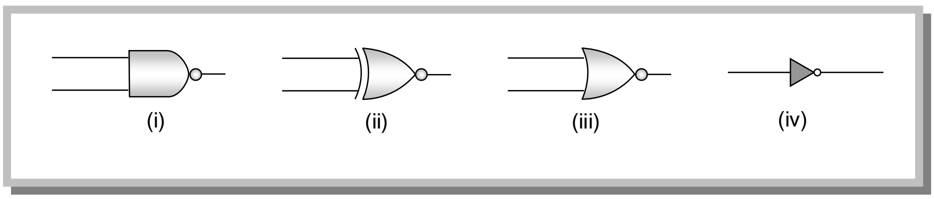
(a) 1, 4, 3

(b) 4, 1, 2

(c) 1, 3, 4

(d) 4, 2, 1

65. Given below are symbols for some logic gates



The XOR gate and NOR gate respectively are **[AFMC 1994]**

(a) 1 and 2 (b) 2 and 3 (c) 3 and 4 (d) 1 and 4

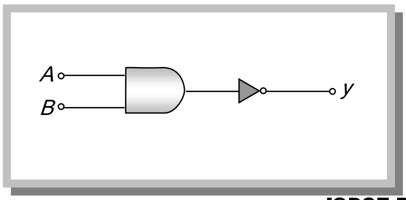
66. What is the name of the gate obtained by the combination shown in figure

(a) NAND

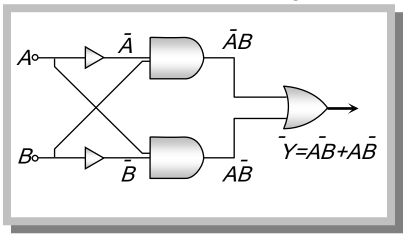
(b) NOR

(c) NOT

(d) XOR



67. Which of the following represent correctly the truth table in of the configuration **[CBSE PMT 1979]**



(a)

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

(b)

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

(c)

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

(d)

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

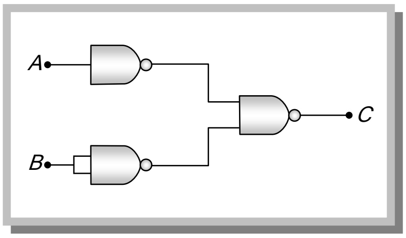
68. The combination of the gates shown in the fig. produces

(a) OR gate

(b) AND gate

(c) NOR gate

(d) XOR gate



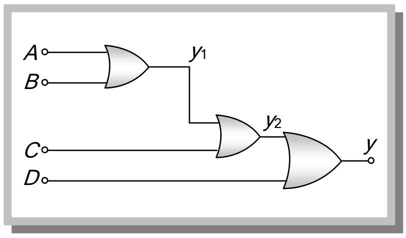
69. The expression *y* in the following circuit is

(a) *ABCD*

(b) *B* + *ACD*

(c) *AB* + *CD*

(d) *A* + *B* + *C* + *D*



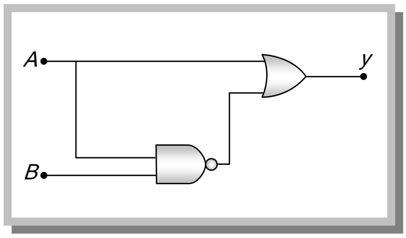
70. What is the output of the combination of the gates shown in the fig.

(a) $A+\overline{A.B}$

(b) $(A.B)+(\bar{A}.\bar{B})$

(c) $(A+B).(\overline{A.B})$

(d) $(A+B)(\bar{A}+\bar{B})$



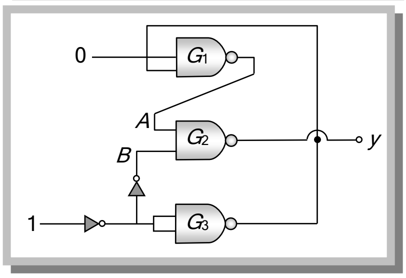
71. In circuit in following fig. the value of *Y* is

(a) 0

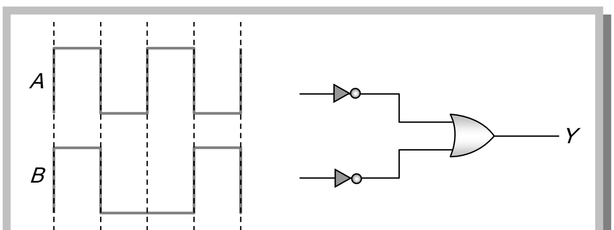
(b) 1

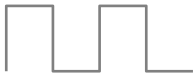
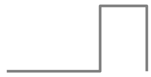
(c) Fluctuates between 0 and 1

(d) Indeterminate as the circuit can't be realised

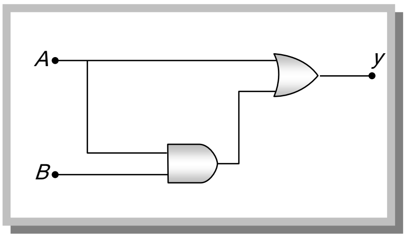


72. In a given circuit as shown the two input waveform *A* and *B* are applied simultaneously. The resultant waveform *Y* is



(a)  (b)  (c)  (d) 

73. What is the output of the combination of the gates shown in the fig. below



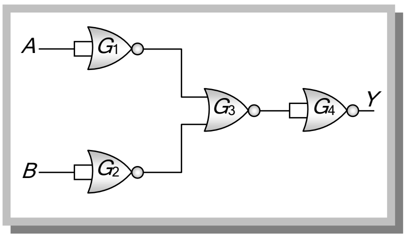
(a) $A + A.B$

(b) $(A+B)\overline{A+B}$

(c) $(A.B)+(\overline{A}.\overline{B})$

(d) $(A+B).(\overline{A.B})$

74. The combination of gates shown below produces



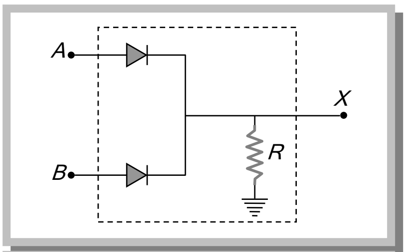
(a) AND gate

(b) XOR gate

(c) NOR gate

(d) NAND gate

75. The circuit shown in figure is used to realise a logic gate. The gate is



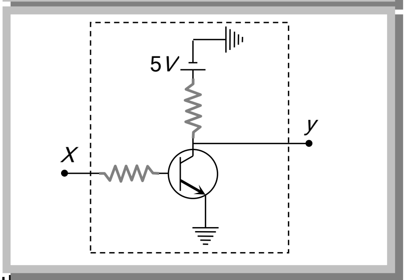
(a) OR

(b) NOT

(c) AND

(d) None of these

76. The circuit shown in fig. is used to realise a logic gate. The gate is



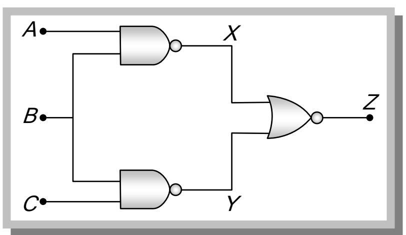
(a) OR

(b) NOT

(c) AND

(d) None of the above

77. The shows two NAND gates followed by a NOR gate. The system is equivalent to the following logic gate



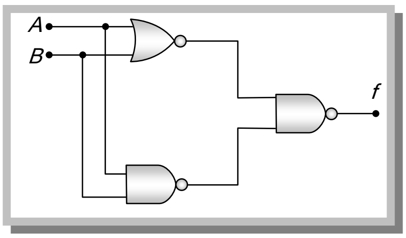
(a) OR

(b) AND

(c) NAND

(d) None of these

78. The Boolean expression for the output *f* of the combination of logic gates shown in fig. is



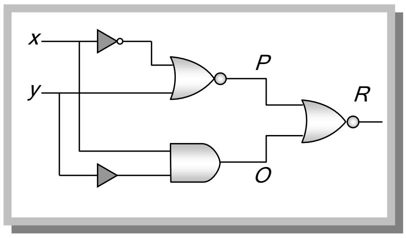
(a) $A.B+\overline{A}.\overline{B}$

(b) $A..\overline{B}+\overline{A}.B$

(c) $A+B..\overline{A}+\overline{B}$

(d) None of these

79. Figure gives a system of logic gates. From the study of truth table it can be found that to produce a high output (1) at *R*, we must have

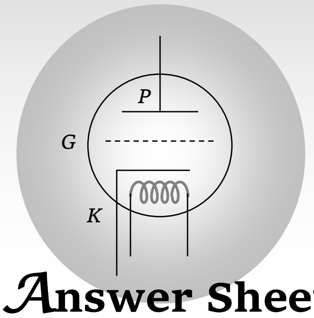


(a) $X = 0,\ Y = 1$

(b) $X = 1,\ Y = 1$

(c) $X = 1,\ Y = 0$

(d) $X = 0,\ Y = 0$



Answer Sheet

Assignments

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
c	c	a	b	b	b	c	b	a	a	c	b	b	c	d	b	b	d	c	c
21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
b	c	b	b	b	b	d	d	c	c	a	c	d	a	a	d	c	a, d	c	d
41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60
c	d	c	c	c	d	d	a	c	d	b	d	a	a	b	b	d	d	c	d
61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	
b	a	b	c	b	a	b	a	d	a	a	a	a	d	a	b	b	c	c	