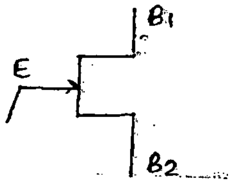
UJT

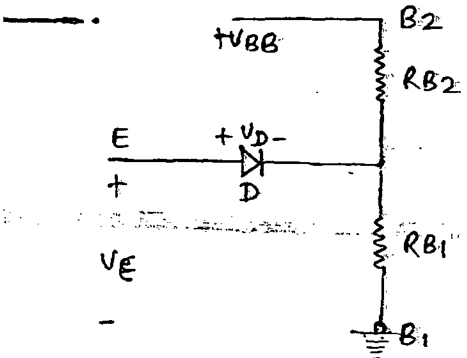


B_1 & B_2 are Base terminal

E – Emitter terminal.

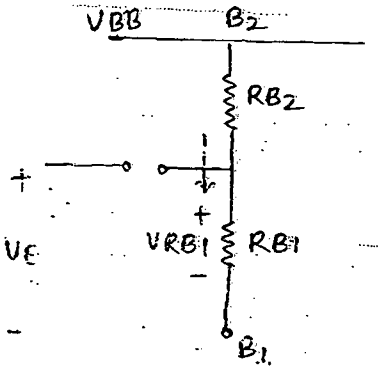
UJT – unijunction transistor.

Equivalent circuit of UJT →



* R_{B1} & R_{B2} → High value (UJT off state)
* Diode is on then UJT on
  diode is OFF then UJT OFF

Suppose diode is OFF;



$$V_{RB1} = \left(\frac{R_{B1}}{R_{B1}+R_{B2}}\right) V_{BB}$$

$$V_{RB1} = \eta V_{BB}$$

$$\boxed{\eta = \frac{R_{B1}}{R_{B1}+R_{B2}}}$$ Intrinsic stand off Ratio.

η = Intrinsic stand off ratio

Let; $V_P = V_{RB1} + V_D$

$V_P = \eta V_{BB} + V_D$

(V_P → Peak point voltage)

↑ V_E & when is reaches to V_P then the UJT will turn on

↑ $V_E \Rightarrow V_P$, UJT → ON

* UJT exibits -ve resistance character.
  Therefore when UJT starts conducting the base resistance R_{B1} starts decreasing.

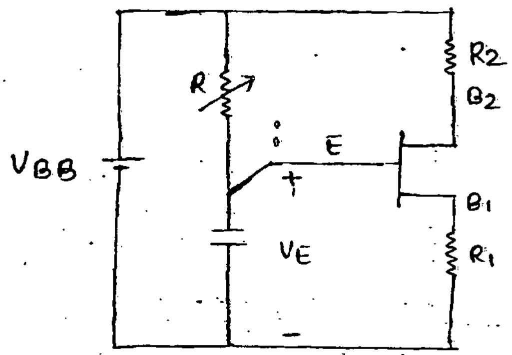
Therefore emitter vol. starts decreasing when UJT starts conducting.

$$\downarrow V_E \Rightarrow V_V,\ UJT \rightarrow OFF$$

$$V_V = \text{Value voltage}$$

* When emitter vol. starts decreasing & reaches to V_V then <u>UJT→OFF</u>

* UJT working as Relaxation oscillator →



UJT→OFF, $V_{B1} = 0$
UJT→OFF, base vol. will charge the capacitor.

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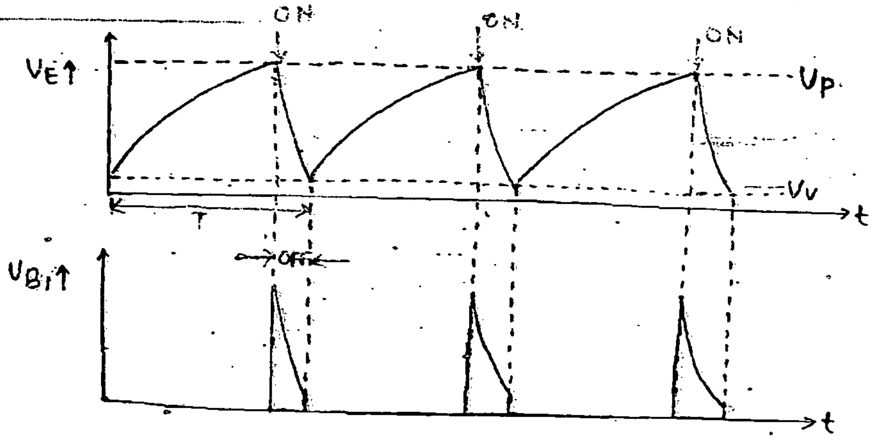
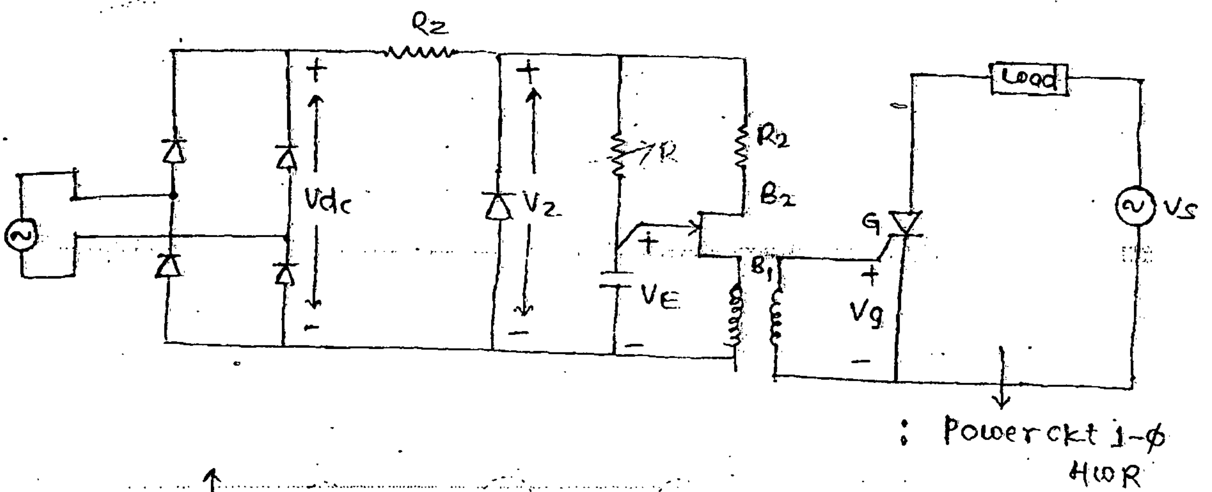


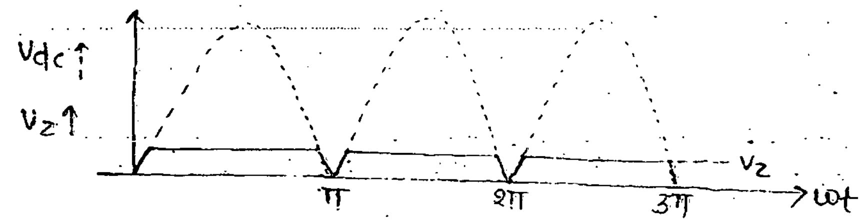
$$T = RC\ln\left(\frac{1}{1-\eta}\right)$$

$$\boxed{f = \frac{1}{RC\ln\left(\frac{1}{1-\eta}\right)}}$$

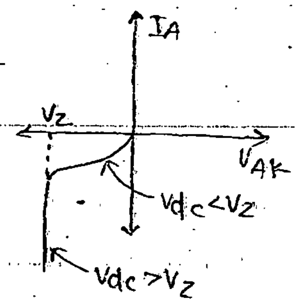
* Synchronised UJT firing ckt →

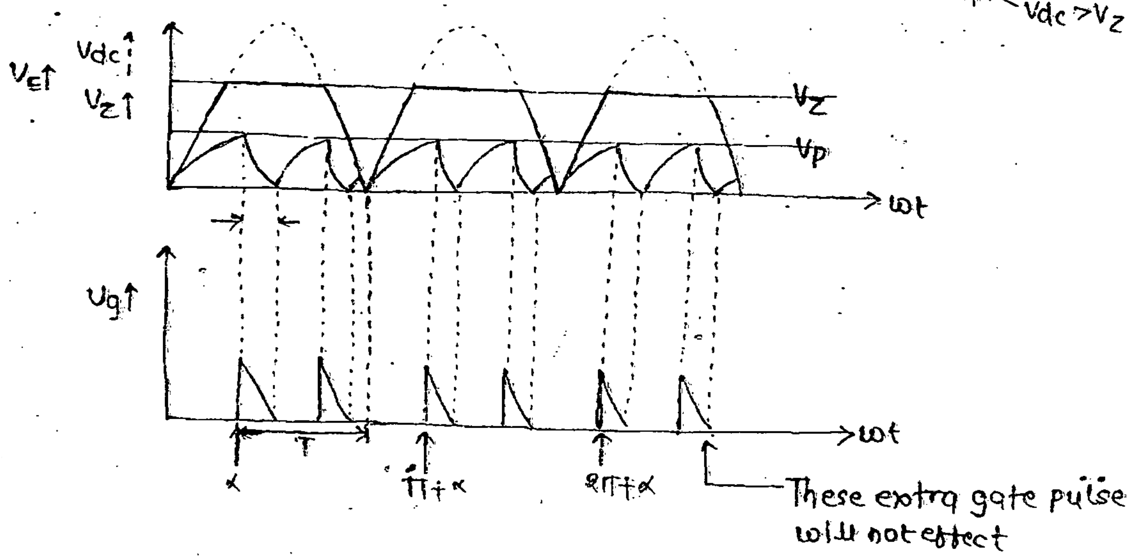
* We must synchronised the firing ckt wrt to the main ckt power supply to match the timings of gate pulse in both the ckt.
* Therefore we must use same power supply in both the ckts for the purpose of synchronisation.





(Still we are not getting the pure dc in 2% variation)

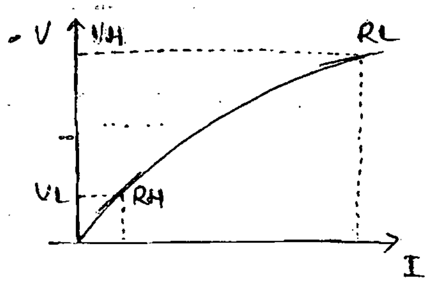




Protection OF Thyristor

(1.) Over current Protection → * We must connect either Fuse (or) CB in series with thy. for Oc protection.

(2.) Over Voltage Protection →



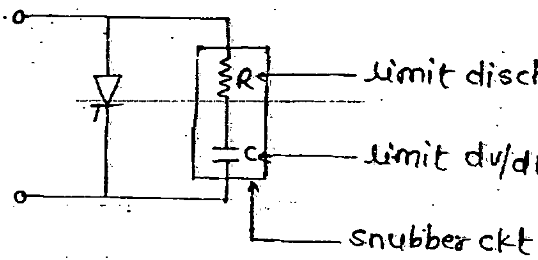
* We must connect a variastor across the thy.
* Variastor is a non-linear restiotor
* All metal oxide resistor behave as non-linear resistor.

eg:- ZnO(zink oxide)

(3.) $\frac{dv}{dt}$ protection →

$$\uparrow I_c = C_j \frac{dv}{dt} \uparrow \quad \& \uparrow I_c \text{ then SCR ON}$$

* At high $\frac{dv}{dt}$ the SCR may turn ON before the gate pulse is given.
* This is an accidental turn-ON.
* This unwanted turn-ON is known as False turn-ON.
* dv/dt protection is needed to avoid the False turn ON.



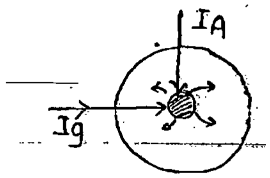
* This ckt is known as Vol. snubber because of dv/dt.

Que→ What is a snubber ckt?

Ans→ When SCR is undergoing switching operation (ON ⇄ OFF) it is subjected to high ele. stress ($\frac{dv}{dt}$ stress, di/dt stress, overvoltage etc)

* The snubber ckt will limit the ele. stress & protect the SCR during switching operations.

(iv) di/dt Protection →



↑ $\frac{di_A}{dt}$ > spread velocity of charge carrier

Effect of high di/dt → * If di/dt > spread velocity of charge carriers then the charge density increases cumulatively in a small cond^n area & this results in the formation of local hotspots damaging the device

* We must connect an inductor in series with SCR for di/dt protection