3 Memory and I/O Interfacing

Multiple Choice Questions

Q.1 RAM and ROM, both are
(a) Sequentially accessed memory
(b) Randomly accessed memory
(c) Either (a) or (b)
(d) RAM: Randomly accessed, ROM sequentially accessed

Q.2 Memory chips of four different sizes as below are available :
1. 32 K × 4
2. 32 K × 16
3. 8 K × 8
4. 16 K × 4

All the memory chips as mentioned in the above list are Read/Write memory. What minimal combination of chips alone can map full address space of 8085 microprocessor?
(a) 1 and 2 (b) 1 only
(c) 2 only (d) 4 only

[IES-2005]

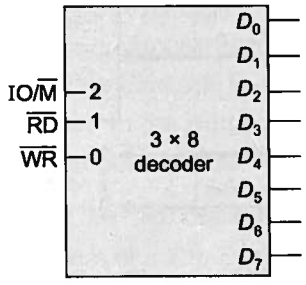
Q.3 A memory of 8 KB is designed using 2048 × 8 RAM chips. The number of chips required are
(a) 4 (b) 6
(c) 8 (d) 16

Q.4 In a 512 × 4 ROM chip, the number of address lines are
(a) 512 (b) 4
(c) 9 (d) 11

Q.5 Which of the following components are used in interfacing memory with microprocessor
(a) Tristate buffer (b) Encoder
(c) Latch (d) All of the above

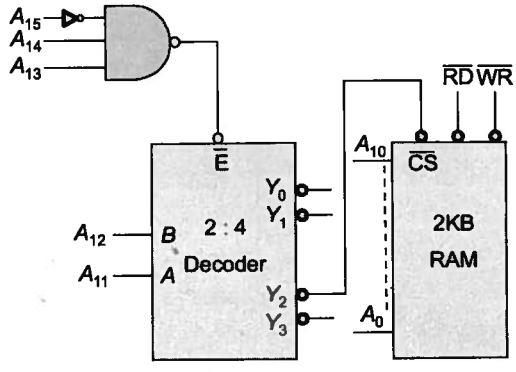
Q.6 Ending address of an 8 KB ROM is B72E H find starting address
(a) D72D H (b) 972F H
(c) 6543 H (d) None

Q.7 Consider the 3 × 8 decoder given below



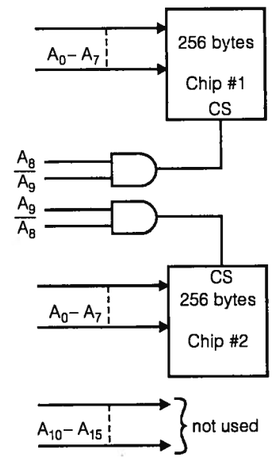
If this to be used with 8085 to generate read and write control signals then valid outputs are
(a) $D_0, D_1, D_2, D_3, D_4, D_5, D_6, D_7$
(b) $D_0, D_1, D_2, D_4, D_5, D_6$
(c) D_1, D_2, D_5, D_6
(d) D_0, D_3, D_4, D_7

Q.8 Memory map of given interfacing logic is



(a) 6800 H - 6FFF H
(b) 7800 H - 7FFF H
(c) 7000 H - 77FF H
(d) None

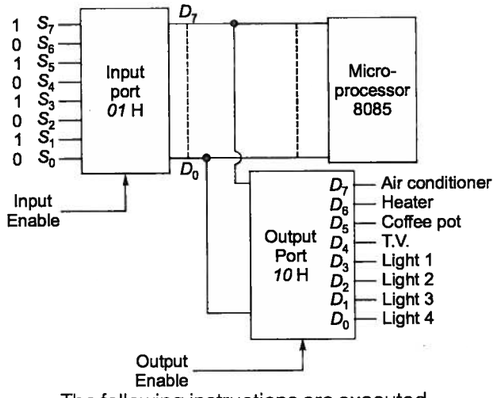
Q.9 What memory address range is NOT represented by chip#1 and chip #2 in the figure. A_0 to A_{15} in this figure are the address lines and CS means Chip select.



(a) 0100-02FF (b) 1500-16FF
(c) F900-FAFF (d) F800-F9FF

[GATE-2005]

Q.10 Consider the figure given below.



The following instructions are executed.

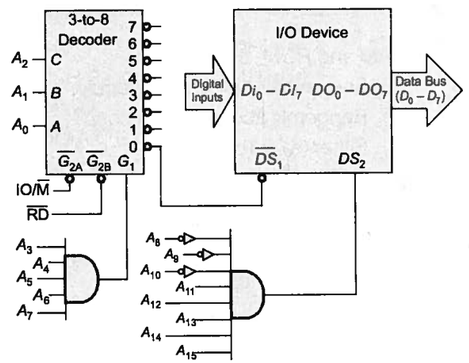
IN 01 H
XRI C2 H
RAL
OUT 10 H

Which of the following statements is/are true.

(*i*) Air conditioner and coffee pot are ON.
(*ii*) Heater and T.V. are ON.
(*iii*) Only 2 Lights are ON.
(*iv*) T.V. and only Light 4 are ON.

(a) (*ii*) and (*i*) (b) (*ii*) only
(c) (*iii*) and (*iv*) (d) (*ii*) and (*iv*)

Q.11 For the 8085 microprocessor, the interfacing circuit to input 8-bit digital data ($DI_0 - DI_7$) from an external device is shown in the figure. The instruction for correct data transfer is



(a) MVI A, F8 H (b) IN F8 H
(c) OUT F8 H (d) LDA F8F8 H

[2014 : 2 Marks, Set-2]

Q.12 The following is not true for RS232 standards

(a) It establishes the way data is coded
(b) It defines signal voltage levels
(c) Does not decide data transmission rate
(d) It defines standard connector configurations

Q.13 The interfacing device used to generate accurate time delay in a microcomputer system is

(a) INTEL 8251 (b) INTEL 8253
(c) INTEL 8257 (d) INTEL 8259

Q.14 What is the maximum memory that can be interfaced with INTEL 8086?

(a) 64 KB (b) 1 MB
(c) 8 KB (d) 2 MB

Numerical Data Type Questions

Q.15 The internal memory of INTEL 8085 is_____byte.

Q.16 Maximum number of 256 × 4 memory chips that can be interfaced with INTEL 8085 microprocessor are _____.

Q.17 A read write memory chip has a capacity of 32 kb. If the memory chip is having equal number address lines and data lines, then minimum number of data lines are _____.

Q.18 A memory system of 128 K bytes needs to be designed with RAM chips of 2 K bytes each and a decoder circuitry constructed with 1 × 2 decoder chips with "enable" input. The minimum number of decoder chips required in design are _____.

Q.19 In INTEL 8085, suppose the peripheral mapped I/O has address length of M and memory mapped I/O has address length of N. Then M + N = _____.

Conventional Questions

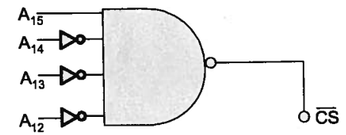
Q.20 Describe various interfacing components.

Q.21 Design a memory of 8 KB using 2048 × 8 RAM chips such that the memory map is 2000 H to 3 FFFH.

Q.22 What are the differences between memory mapped I/O and I/O mapped I/O?

Q.23 Write an ALP to access a data byte from port address 60 H and send it to port address 70 H where a display is connected. Draw the required interfacing logic circuit.

Q.24 If the output of the NAND gate is connected to a memory chip $\overline{CS}$ line then find the capacity and memory map of the memory chip.

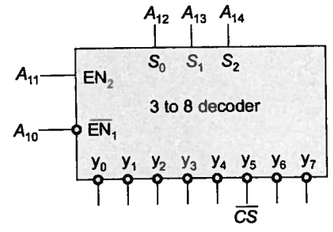


Try Yourself

T1. If a page of memory is assumed to be 256 bytes then in how many pages total memory of 8085 can be treated ?

[Ans: 256]

T2. A 1 Kbyte memory module has to be interfaced with an 8-bit microprocessor that has 16 address lines. The address lines A_0 to A_9 of the processor are connected to the corresponding address lines of the memory module. The active low chip select $\overline{CS}$ of the memory module is connected to the y_5 output of a 3 to 8 decoder with active low outputs. S_0, S_1, and S_2 are the input lines to the decoder, with S_2 as the MSB. The decoder has one active low $\overline{EN_1}$ and one active high EN_2 enable lines as shown below. The address range(s) that gets mapped onto this memory module is (are)



(a) 3000_H to $33FF_H$ and $E000_H$ to $E3FF_H$
(b) 1400_H to $17FF_H$
(c) 5300_H to $53FF_H$ and $A300_H$ to $A3FF_H$
(d) 5800_H to $5BFF_H$ and $D800_H$ to $DBFF_H$

[Ans: (d)]