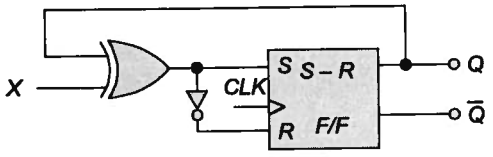
4 Sequential Circuits

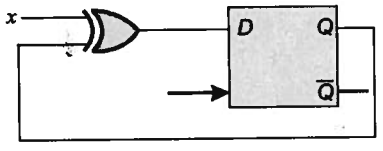
Multiple Choice Questions

Q.1 Identify the type of the flip-flop



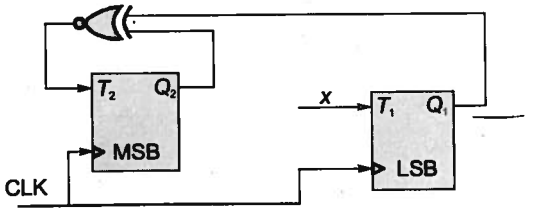
(a) R-S flip-flop (b) J-K flip-flop
(c) D flip-flop (d) T-flip-flop

Q.2 The circuit acts as



(a) D-Flip Flop (b) T-Flip Flop
(c) Both A and B (d) None

Q.3 Consider the partial implementation of a 2-bi counter using T flip-flops following the sequenc 0-2-3-1-0, as shown below

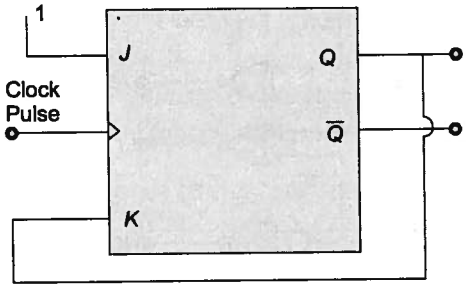


To complete the circuit, the input X should be

(a) Q_2' (b) $Q_2 + Q_1$
(c) $(Q_1 \oplus Q_2)'$ (d) $Q_1 \oplus Q_2$

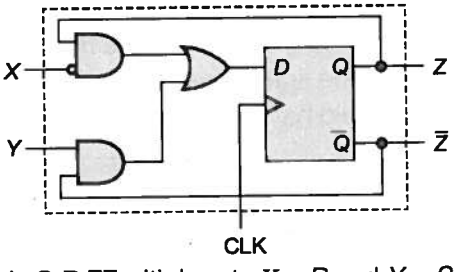
[GATE-2004]

Q.4 In figure, assume that initially $Q = 1$. With clock pulses being given, the subsequent states of Q will be



(a) 1, 0, 1, 0, 1, 0, 1
(b) 0, 0, 1, 0, 0, 1, 0....
(c) 1, 1, 0, 1,1, 0,1
(d) 0,1, 0, 1, 0, 1, 0....

Q.5 A sequential circuit using D flip-flop and logic gates is shown in figure where X and Y are the inputs and Z is the output. The circuit is



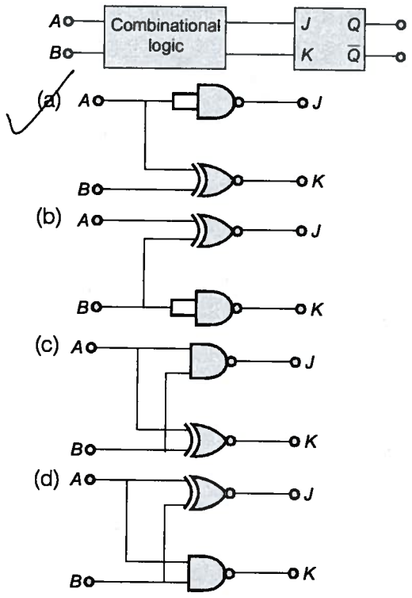
(a) S-R FF with inputs $X = R$ and $Y = S$
(b) S-R FF with inputs $X = S$ and $Y = R$
(c) J-K FF with inputs $X = J$ and $Y = K$
(d) J-K FF with inputs $X = K$ and $Y = J$

Q.6 The characteristic equation of the T-FF is given by

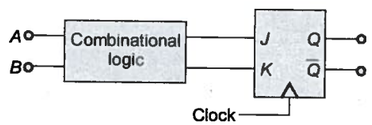
(a) $Q^+ = T\overline{Q} + Q\overline{T}$ (b) $Q^+ = \overline{T}Q + TQ$
(c) $Q^+ = TQ$ (d) $Q^+ = T\overline{Q}$

Q.7 The circuit realization of the combination logic block shown in figure to obtain the following truth table will be,

A	B	Q_{n+1}
0	0	$\overline{Q}_n$
0	1	1
1	0	Q_n
1	1	0



Q.8 To realize the given truth table from the circuit shown in the figure, the input to J in terms of A and B would have to be



Truth Table

A	B	Q_{n+1}
0	0	Q_n
0	1	1
1	0	Q_n
1	1	0

(a) $\overline{A}$ (b) B
(c) $\overline{A}\overline{B}$ (d) $\overline{A}B$

Q.9 X-Y flip flop, whose Characteristic Table is given below is to be implement using a J-K flip flop

X	Y	Q_{n+1}
0	0	1
0	1	$\overline{Q_n}$
1	0	Q_n
1	1	0

This can be done by making
(a) $J = \overline{Y}, K = X$ (b) $J = \overline{X}, K = Y$
(c) $J = Y, K = \overline{X}$ (d) $J = X, K = \overline{Y}$

Q.10 Match **List-I** with **List-II** and select the correct answer using the codes given below the lists:

List-I
A. Shift register
B. Counter
C. Decoder

List-II
1. Frequency division
2. Addressing in memory chips
3. Serial to parallel data conversion

Codes:

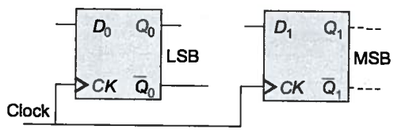
	A	B	C
(a)	3	2	1
(b)	1	2	2
(c)	2	1	3
(d)	3	1	2

[EC : GATE-2004]

Q.11 Two D-flip flops, as shown below are to be connected as a synchronous counter that goes through the following $Q_1\ Q_0$ sequence

$00 \rightarrow 01 \rightarrow 11 \rightarrow 10 \rightarrow 00...$

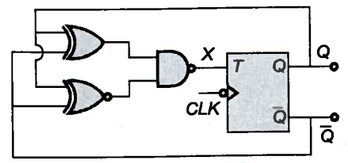
The inputs D_0 and D_1 respectively should be connected as



(a) $\overline{Q_1}\ \overline{Q_0}$ and $Q_1\ Q_0$ (b) $\overline{Q_0}$ and Q_1
(c) $\overline{Q_1}Q_0$ and $\overline{Q_1}\ Q_0$ (d) $\overline{Q_1}$ and Q_0

[EC : GATE-2006]

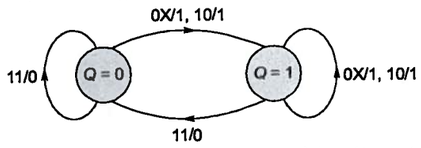
Q.12 The clock frequency applied to the digital circuit shown in figure below is 1 kHz. If the initial state of the output Q of the flip-flop is '0', then the frequency of the output waveform Q in kHz is



(a) 0.25 (b) 0.5
(c) 1 (d) 2

[GATE-2013]

Q.13 A state diagram of a logic which exhibits a delay in the output is shown in the figure, where X is the do not care condition, and Q is the output representing the state.



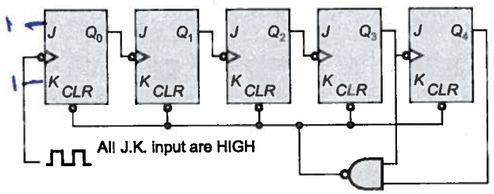
The logic gate represented by the state diagram is
(a) XOR (b) OR
(c) AND (d) NAND **[GATE-2014]**

Q.14 Latches constructed with NOR and NAND gates tend to remain in the latched condition due to which configuration feature?
(a) Asynchronous operation
(b) Low input voltage
(c) Gate impedance
(d) Cross coupling **[ESE-2013]**

Q.15 Synchronous counters eliminate the delay problems encountered with asynchronous (ripple) counter because the
(a) input clock pulses are applied only to the first and the last stages
(b) input clock pulses are applied only to the last stage
(c) input clock pulses are not used to activate any of the counter stages
(d) input clock pulses are applied simultaneously

[ESE-2013]

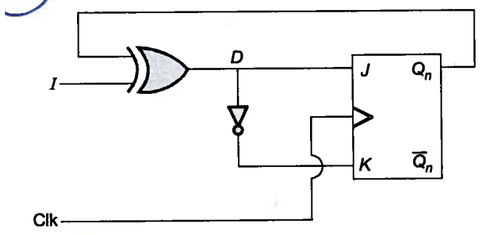
Q.16 The mod-number of the asynchronous counter shown in figure



(a) 24 (b) 48
(c) 25 (d) 36

Q.17 The output of moore sequential machine is a function of
(a) all present states of machine
(b) all inputs
(c) all combination of inputs and present state
(d) few combination of inputs and present state

Q.18 If I is set high is circuit given below then Q_{n+1} is



(a) complementary (b) Q_n
(c) high (d) low

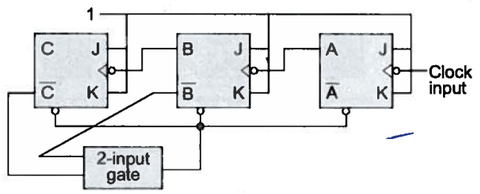
Q.19 The number of unused states in a 4-bit Johnson counter is
(a) 2 (b) 4
(c) 8 (d) 12

[ESE-2003]

Q.20 A 4 bit ripple counter and a 4 bit synchronous counter are made using flip flops having a propagation delay of 10 ns each. If the worst case delay in the ripple counter and the synchronous counter be R and S respectively, then
(a) $R = 10$ ns, $S = 40$ ns
(b) $R = 40$ ns, $S = 10$ ns
(c) $R = 10$ ns, $S = 30$ ns
(d) $R = 30$ ns, $S = 10$ ns

[GATE-2003]

Q.21 In the modulo-6 ripple counter shown in the figure, the output of the 2-input gate is used to clear the *J-K* flip-flops.

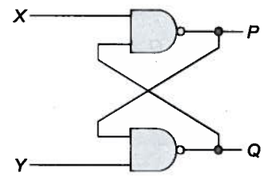


The 2-input gate is

(a) a NAND gate (b) a NOR gate
(c) an OR gate (d) an AND gate

[GATE-2004]

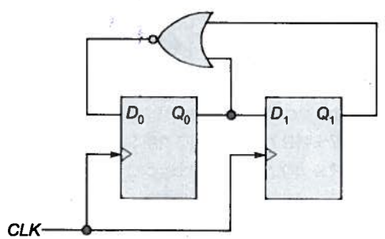
Q.22 The following binary values were applied to the *X* and *Y* inputs of the NAND latch shown in the figure in the sequence indicated below:
$X = 0, Y = 1$; $X = 0, Y = 0$; $X = 1, Y = 1$.
The corresponding stable P, Q outputs will be



(a) $P = 1, Q = 0$; $P = 1, Q = 0$; $P = 1, Q = 0$ or $P = 0, Q = 1$
(b) $P = 1, Q = 0$; $P = 0, Q = 1$ or $P = 0, Q = 1$; $P = 0, Q = 1$
(c) $P = 1, Q = 0$; $P = 1, Q = 1$; $P = 1, Q = 0$ or $P = 0, Q = 1$
(d) $P = 1, Q = 0$; $P = 1, Q = 1$; $P = 1, Q = 1$

[GATE-2007]

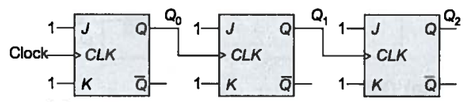
Q.23 For the circuit shown, the counter state $(Q_1 Q_0)$ follows the sequence



(a) 00, 01, 10, 11, 00 ...
(b) 00, 01, 10, 00, 01 ...
(c) 00, 01, 11, 00, 01 ...
(d) 00, 10, 11, 00, 10 ...

[GATE-2007]

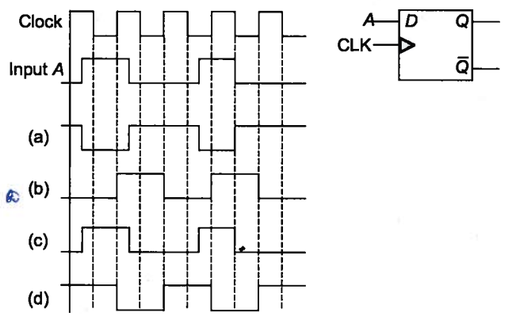
Q.24 The figure below shows a 3-bit ripple counter, with Q_2 as the MSB. The flip-flop are rising-edge triggered. The counting direction is



(a) always down
(b) always up
(c) up or down depending on the initial state of Q_0 only
(d) up or down depending on the initial states of Q_2, Q_1 and Q_0

[GATE-IN:2009]

Q.25 The input *A* and clock applied to the *D* flip-flop are shown in figure below. The output *Q* is,



Q.26 The output Q_n of a J-K flip-flop is zero. It changes to 1 when a clock pulse is applied. The input J_n a K_n are respectively (*X* represents don't care condition):

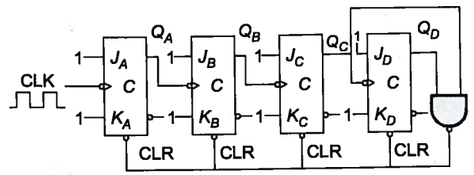
(a) 1 and *X* (b) 0 and *X*
(c) *X* and 0 (d) *X* and 1

[ESE-2013]

Q.27 The Q-output of J-K flip-flop is '1'. The output does not change when a clock-pulse is applied. The input J and K will be respectively (x-don't care state)

(a) 0 and x (b) 0 and 1
(c) 1 and 0 (d) x and 0

Common Data for Questions (28 and 29):
A counter is shown below:



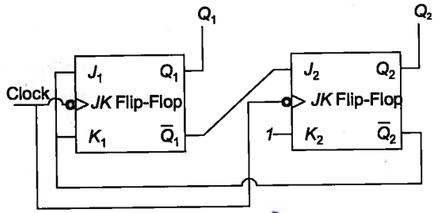
Q.28 The counter shown is

(a) Mod-12 (b) Mod-9
(c) Mod-14 (d) None of these

Q.29 Frequency of output Q_D for 1 MHz clock is

(a) 63.3 kHz (b) 83.3 kHZ
(c) 73.3 kHz (d) None of these

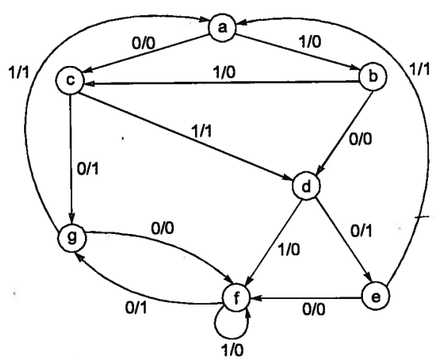
Q.30 What are the counting states (Q_1, Q_2) for the counter shown in the figure below?



(a) 01, 10, 11, 00, 01... (b) 11, 10, 00, 11, 10...
(c) 00, 11, 01, 10, 00... (d) 01, 10, 00, 01, 10...

[EC GATE-2009]

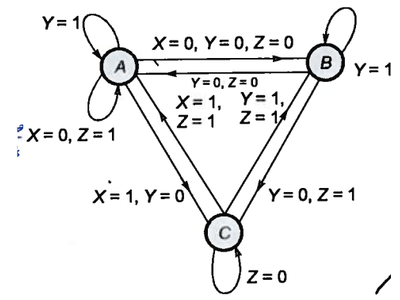
Q.31 Following state diagram shows clocked sequential circuit:



How many minimum number of states the sequential circuit has?

(a) 6 (b) 7
(c) 5 (d) 4

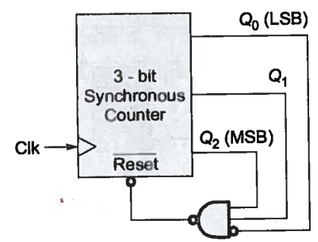
Q.32 The state transition diagram for a finite state machine with states *A*, *B* and *C*, and binary inputs *X*, *Y* and *Z*, is shown in the figure.
Which one of the following statements is correct?



(a) Transitions from State *A* are ambiguously defined.
(b) Transitions from State *B* are ambiguously defined.
(c) Transitions from State *C* are ambiguously defined.
(d) All of the state transitions are defined unambiguously.

[GATE-2016]

Q.33 For the circuit shown in the figure, the delay of the bubbled NAND gate is 2 ns and that of the counter is assumed to be zero.

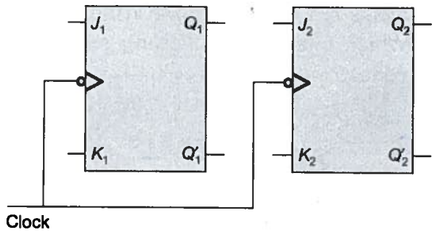


If the clock (Clk) frequency is 1 GHz, then the counter behaves as a

(a) mod-5 counter (b) mod-6 counter
(c) mod-7 counter (d) mod-8 counter

[GATE-2016]

Q.34 A synchronous counter using two J - K flip flops that goes through the sequence of states: $Q_1Q_2 = 00 \rightarrow 10 \rightarrow 01 \rightarrow 11 \rightarrow 00$ ... is required. To achieve this, the inputs to the flip flops are:



(a) $J_1 = Q_2$, $K_1 = 0$; $J_2 = Q_1'$, $K_2 = Q_1$

(b) $J_1 = 1$, $K_1 = 1$; $J_2 = Q_1$, $K_2 = Q_1$

(c) $J_1 = Q_2$, $K_1 = Q_2'$; $J_2 = 1$, $K_2 = 1$

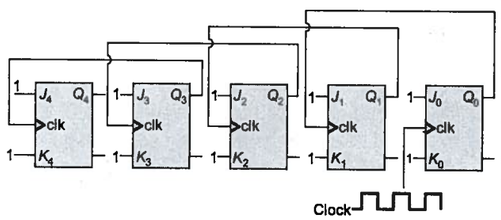
(d) $J_1 = Q_2'$, $K_1 = Q_2$, $J_2 = Q_1$, $K_2 = Q_1'$

[GATE-2016]

Numerical Data Type Questions

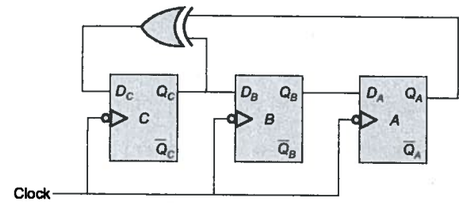
Q.35 The minimum number of flip-flops required by a module-8 counter is 3.

Q.36 Five JK flip-flops are cascaded to form the circuit shown in Figure. Clock pulses at a frequency of 1 MHz are applied as shown. The frequency (in kHz) of the waveform at Q_3 is _____.

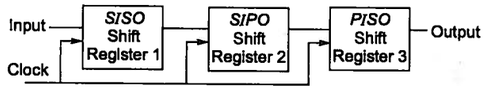


[GATE-2014]

Q.37 A digital circuit is designed with three *D*-flip flops and an Ex-OR gate as shown in below figure. If the initial value of $Q_A\ Q_B\ Q_C$ was 110 then the minimum number of clock pulses required to get $Q_A\ Q_B\ Q_C$ as 011 is _____.



Q.38 Three 4 bit shift registers are connected in cascade as shown in figure below. Each register is applied with a common clock pulse.



A 4 bit data 1011 is applied to the shift register 1.The minimum number of clockpulses required to get same input data at output with same clock are_____.

Common Data for Questions (39 and 40):

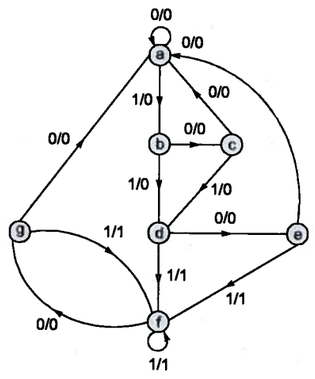
A Mealy system produces a 1 output if the input has been 0 for at least two consecutive clocks followed immediately by two or more consecutive 1's.

Q.39 The minimum number of states for this system is _____.

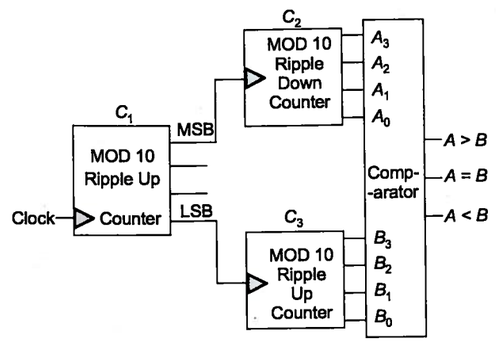
Q.40 The flip-flops required to implement this system are _____.

Try Yourself

T1. Reduce the following state diagram and also write the reduced state table.



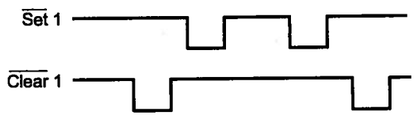
T2. Consider the circuit given below:



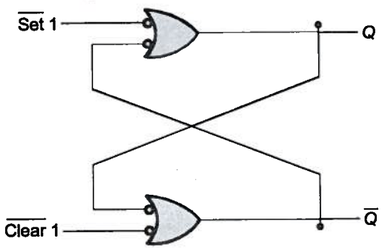
MSB and LSB of MOD 10 ripple up counter acts as clock to 4 bit ripple down and up counter respectively. Initially all the counter were cleared and output of comparator was $A = B$. The clock pulse is applied. Find the minimum number of clock pulses required to make $A = B$ again.

[Ans: 17]

T3. The waveforms.



are applied to the inputs of the latch



Draw the waveform at Q and explain.

[ESE-2006]

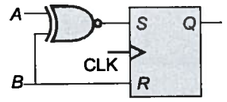
T4. Using J-K flip-flop, design a counter which has the following count sequence:

0	0	0
0	0	1
0	1	0
1	0	0
1	0	1
1	1	0

Draw the excitation table, logic diagram and state diagram.

[ESE-2007]

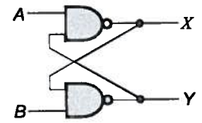
T5. An AB flip-flop is constructed from an SR flip-flop as shown in fig. The expression for next state Q^+ is



(a) $\bar{A}\bar{B} + AQ$ (b) $\bar{A}\bar{B} + \bar{B}Q$

(c) Both A and B (d) None of the above

T6. In figure initially $A = 1$ and $B = 1$, the input B is now replaced by a sequence 1 0 1 0 1 0 ... the outputs X and Y will be



(a) Fixed at 0 and 1 respectively

(b) Fixed at 1 and 0, respectively

(c) X = 1 0 1 0 ... while Y = 1 0 1 0 ...

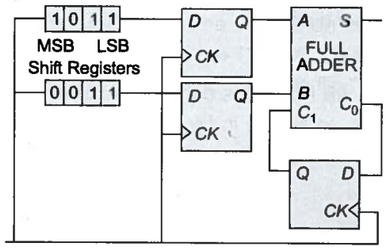
(d) X = 1 0 1 0 ... while Y = 0 1 0 1 ...

T7. A new Flip-Flop is having behaviour as described below. It has two inputs X and Y and when both inputs are same and they are 1,1, the flip-flop is going to set else flip-flop resets. If both inputs are different and they are 0, 1, filp-flop complements itsself otherwise it is going to retain the last state. Which of the following expression is the characteristic expression for the new flip flop?

(a) $xQ + y\bar{Q}$ (b) $x\bar{Q} + yQ$

(c) $x\bar{Q} + y\bar{Q}$ (d) None

T8. For the circuit shown in the figure below, two 4-bit parallel-in-serial-out shift registers loaded with the data shown are used to feed the data to a full adder. Initially, all the flip-flops are in the clear state. After applying two clock pulses, the outputs of the full adder should be



(a) $S = 0$ $C_0 = 1$ (b) $S = 0$ $C_0 = 0$
(c) $S = 1$ $C_0 = 1$ (d) $S = 1$ $C_0 = 0$

[EC GATE-2006]

T9. Design a MOD-10 synchronous counter using J-K flip-flops giving state diagram excitation table, K-maps and circuit diagram.

[ESE-2008]

T10. Design a mod-6 counter to go through the sequence of states as given in the table below using S-R flip-flop:

Sequence No.	Required State Sequence		
0	0	0	0
1	0	1	0
2	0	1	1
3	1	1	0
4	1	0	1
5	0	0	1 → Repeat from 0 0 0

Show the state table indicating the present state, the next state for each present state along with the input requirements of each of the S and R inputs. Show clearly the minimization of logic requirements using K-maps. Write the logical expressions for each excitation input of all the flip-flops. Draw the logic diagram of the counter designed by you.

[ESE-2009]

T11. Using *T* flip-flop and logic gates, design a *L-M* edge triggered flip-flop having a truth table as given below:

L	M	Q_+
0	0	0
0	1	$\overline{Q}$
1	0	1
1	1	$\overline{Q}$

[ESE-2014]

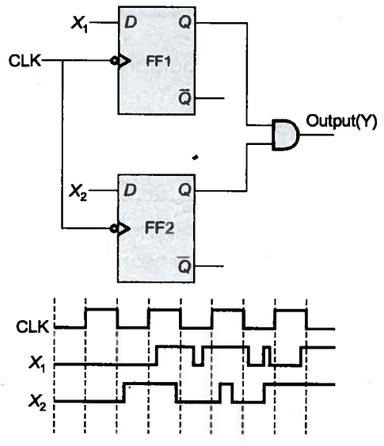
T12. Design a Synchronous BCD Counter using J-K Flip-flops.

T13. Design a counter using D flip-flop that goes through states, 0, 1, 2, 4, 0. The undesired (unused) states must always go to zero (000) on the next clock pulse.

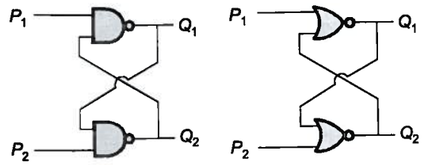
T14. Desigh synchronous counter for given count sequence
$00 \rightarrow 10 \rightarrow 01 \rightarrow 11$.

T15. Consider a mod-1000 ripple up counter. The duty cycle for its MSB is _____%.

T16. Consider the flip-flop circuit diagram shown below. Draw output waveform for the circuit.



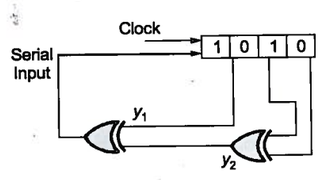
T17. Refer to the NAND and NOR latches shown in the figure. The inputs (P_1, P_2) for both the latches are first made (0, 1) and then after a few second, made (1, 1). The corresponding stable outputs (Q_1, Q_2) are



(a) NAND: first (0, 1) then (0, 1) NOR: first (1, 0) then (0, 0)
(b) NAND: first (1, 0) then (1, 0) NOR: first (1, 0) then (0, 0)
(c) NAND: first (1, 0) then (1, 1) NOR: first (0, 1) then (0, 1)
(d) NAND: first (1, 0) then (1, 0) NOR: first (0, 1) then (0, 0)

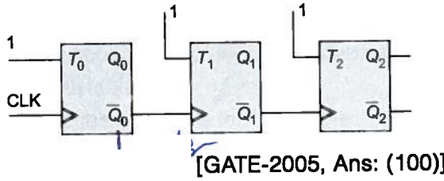
[EC : GATE-2009, Ans: (b)]

T18. The shift register shown in the given figure is initially loaded with the bit pattern 1010. Subsequently the shift register is clocked, and with each clock pulse the pattern gets shifted by one bit position to the right. With each shift, the bit at the serial input is pushed to the left most position (msb). After how many clock pulses will the content of the shift register become 1010 again?



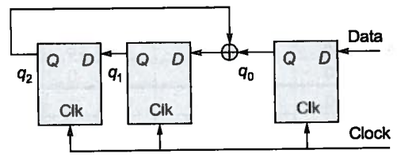
[Ans: (7)]

T19. The given figure shows a ripple counter using positive edge triggered flip-flops.
If the present state of the counter is Q_2 Q_1 Q_0 = 011, then its next state (Q_2 Q_1 Q_0) will be 100



[GATE-2005, Ans: (100)]

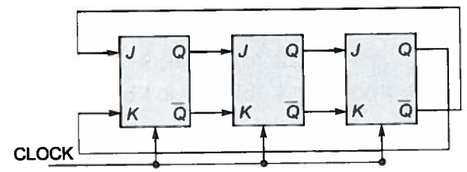
T20. Consider the circuit in the diagram. The ⊕ operator represents Ex-OR. The D flip-flops are initialized to zeroes (cleared).



The following data : 100110000 is supplied to the "data" terminal in nine clock cycles. After that the values of q_2 q_1 q_0 are
(a) 000 (b) 001
(c) 010 (d) 101

[GATE-2006, Ans: (c)]

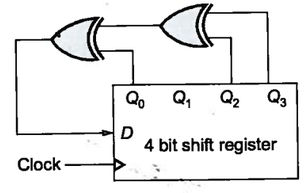
T21. For the initial state of 000, the function performed by the arrangement of the J-K flip flops in the figure



(a) Shift Register (b) Mod-3 counter
(c) Mod-6 counter (d) Mod-2 counter

[EC : GATE-1993]

T22. A 4 bit right shift, shift register is shifting the data to the right for every clock pulse The serial input *D* is derived by using Ex-OR gates as shown in the figure. After three clock pulses the content in the shift register is to be 1010 at $Q_0Q_1Q_2Q_3$, what will be the initial content of the register.



(a) 1100 (b) 1010
(c) 0011 (d) 0101

T23. Consider the following state transition table with two state variables A and B and the input variable x and the output variable y

Present State		Input	Next State		Output
A	B	x	A	B	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	1

If the initial state is $A = 0$ and B = 0, what is the minimum length of an input string which will take the macine to the state $A = 1$ and $B = 1$ with output $y = 1$?

(a) 3 (b) 4

(c) 5 (d) 6

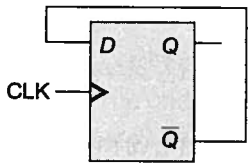
[DRDO-2009]

T24. If a counter having 10 FF's is initially at 0, what count will it hold after 2060 pulses?

(a) 000 000 1100 (b) 000 001 1100

(c) 000 001 1000 (d) 000 000 1110

T25. The frequency of the clock signal applied to the rising edge triggered D-flip flop shown in the following figure is 10 kHz. What is the output frequency at the flip flop output Q? (in kHz)



T26. How many pulses are needed to change the contents of a 8-bit up-counter from 10101100 to 00100111 (right most bit is the LSB)?

[IT GATE-2005]